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Hybrid Inverter Concept for Extreme Bandwidth High-Power AC Source

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Hybrid inverter concept for extreme bandwidth high-power AC source

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A hybrid inverter concept for switch-mode power amplifiers as used, e.g. in power-hardware-in-the-loop testing is proposed. A main converter operating from the supplying DC voltage generates a multilevel output voltage by means of parallel-interleaved operation of several bridge legs and combination of the bridge leg output voltages with coupled inductors into a multilevel waveform. A second, series-connected inverter features a floating DC bus with only a fraction of the main converter's DC voltage, which enables a significantly higher switching frequency. The series inverter compensates the deviation of the main inverter's multilevel output voltage from the reference voltage, whereby pulse-width modulation with sawtooth carriers is employed, and hence defines the effective switching frequency of the hybrid inverter's overall output voltage. This allows for a higher output filter cutoff frequency and ultimately features a significant increase of the full-range system bandwidth, which improves by more than an order of magnitude for the considered 100 kVA example system compared with a conventional approach. Finally, closed-loop circuit simulations verify the high performance of the proposed system.

Introduction: Applications such as power-hardware-in-the-loop testing or grid simulation require controllable voltage or power sources that provide high bandwidth and fast dynamics as well as low total harmonic distortion (THD) of the controlled output voltage and/or current. The inherently high losses of typically employed analogue amplifiers limit their feasible power ratings. Therefore, switch-mode power amplifiers have to be considered for power levels in the hundreds of kVAs. On the other hand, switch-mode power amplifiers require a lowpass output filter to suppress switching harmonics and meet THD limits. The filter's cutoff frequency directly limits the achievable bandwidth, yet it needs to be sufficiently lower than the amplifier's switching frequency for the filter to provide enough attenuation. However, switching losses limit the feasible switching frequencies in hard-switched inverter operation to a few 10 kHz even for modern silicon carbide (SiC) power semicondcutors.

Literature describes various techniques to increase the *effective* switching frequency and possibly also the number of voltage levels at the inverter output, which enables higher filter cutoff frequencies. Multilevel converter structures such as the neutral-point-clamped (NPC) converters, the flying capacitor converters, or, providing full modularity at the cost of high complexity, cascaded H-bridge systems share the total DC voltage among several switches with lower voltage ratings [1], which allows also for higher device switching frequencies in addition to the increased effective switching frequency of the multilevel output voltage.

However, a *hybrid* approach may lead to a better trade-off between output voltage quality (frequency, voltage levels) and system complexity: considering the scaling of power semiconductor switching energies with their rated voltage, slow-switching stages with high DC voltages process the bulk voltage/power whereas fast-switching stages with low DC voltages improve the harmonic quality of the output voltage. Targeting medium-voltage drive applications, the authors in [2, 3] proposed a combination of a slow-switching high-voltage NPC converter with a series-connected low-voltage H-bridge. The DC bus of the series H-bridge can either be actively supplied [2], or, since by generating a voltage that compensates the deviation of the NPC converter's output voltage from the reference, the series H-bridge exchanges only switching frequency reactive power with the load, it can be left floating and be stabilised with appropriate control [3]. Similarly, Manjrekar and Lipo [4] proposed a cascade configuration of converter cells with different DC bus voltages and hence different switching frequencies and power ratings.

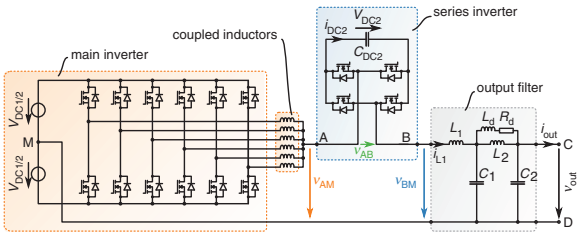

Fig. 1 *Proposed hybrid inverter consisting of main inverter and series inverter rated at fraction of voltage/power only (single phase shown)*

Proposed hybrid inverter concept: Instead of generating a multilevel voltage using either several cascaded converter cells (with high complexity) or, e.g. a NPC converter (limited number of levels), parallel-interleaved operation of several simple two-level bridge legs with their output voltages combined by means of coupled inductors [5] can be used. Fig. 1 shows the proposed hybrid topology [6] for a single phase of an extreme bandwidth power source, Fig. 2 shows the corresponding control block diagram, and Fig. 3 shows key waveforms.

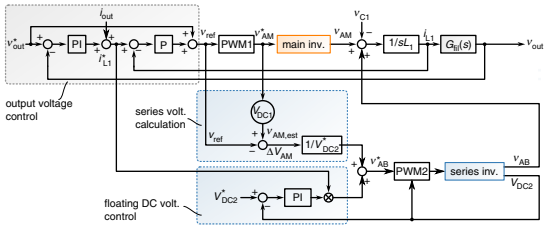

Fig. 2 *Hybrid inverter control system overview*

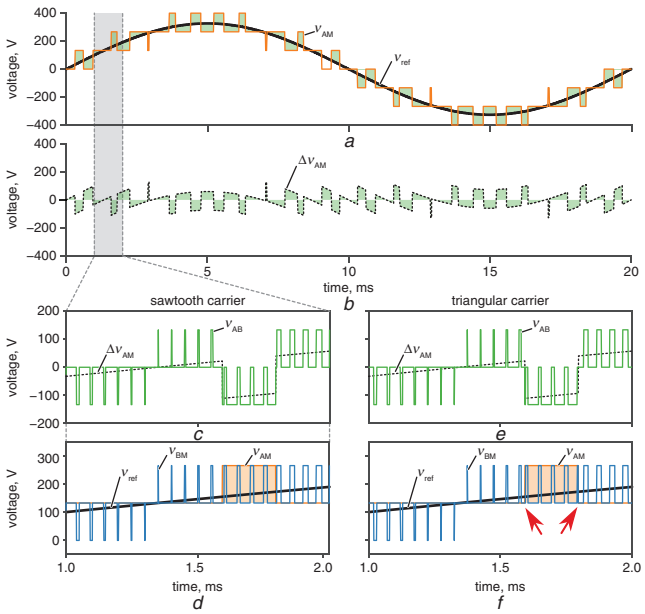

Fig. 3 *Key waveforms of proposed system (low switching frequencies for better visibility)*

a Voltage reference and main inverter output voltage
b Difference between main inverter output voltage and reference
c Series inverter output voltage (sawtooth carrier)
d Combined output voltage (sawtooth carrier)
e Series inverter output voltage (triangular carrier)
f Combined output voltage (triangular carrier)

The main inverter operates from the full DC voltage (e.g. 800 V, cf. Table 1) and uses phase-shifted pulse-width modulation to generate n phase-shifted (by $2\pi/n$) rectangular output voltages of the n bridge legs, each switching at a frequency f_{s1}. These phase-shifted output voltages are combined by means of a coupled inductor to obtain a multilevel output voltage, v_{AM}, with an effective switching frequency of $f_{s1,eff} = n \cdot f_{s1}$ and $n+1$ voltage levels. However, this multilevel voltage is only an approximation of the reference voltage v_{ref} that is, e.g. calculated by a state-of-the art cascaded output voltage controller [7].

Table 1: Parameters of a 100 kVA (three-phase) example system

P_N (1ph)	33.3 kVA	V_N	230 V	I_N	150 A
V_{DC}	800 V	f_{s1}	20 kHz	$f_{s1,eff}$	120 kHz
V_{DC2}	133 V	f_{s2}	1 MHz	$f_{s2,eff}$	2 MHz

The approximation can be improved by adding a corresponding difference voltage $\Delta v_{AM} = v_{ref} - v_{AM}$ to v_{AM}, which could be accomplished by a second inverter stage that is connected in series to the main inverter, provided this series inverter switches at a sufficiently higher switching frequency f_{s2}. As $|\Delta v_{AM}| \leq V_{DC}/n$, the series inverter's DC voltage can be as low as $V_{DC2} = V_{DC}/n$, i.e. the height of one voltage step of

v_{AM}. Since thus V_{DC2} is significantly smaller than V_{DC}, the series inverter's switches can have a lower voltage rating and hence sustain a much higher switching frequency $f_{s2} \gg f_{s1,eff}$. Using Δv_{AM} (e.g. calculated from the main inverter's switching states) as the reference for the PWM of the series inverter causes the local average value of its output voltage to compensate the deviation, i.e. $\bar{v}_{AB} = \Delta v_{AM}$, and the effective switching frequency of the voltage applied to the filter $v_{BM} = v_{AM} + v_{AB}$ increases to $f_{s,eff} = 2f_{s2}$ if unipolar PWM is employed. Therefore, the output filter's cutoff frequency can be significantly increased from f_{c1} to f_{c2} for the same output voltage THD (cf. Figs. 4*a* and *b*).

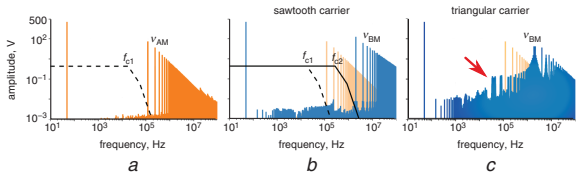

Fig. 4 *Voltage spectra for system specifications according to Table 1*
a Main inverter only
b Main inverter and series inverter with sawtooth carrier
c Main inverter and series inverter with triangular carrier

The asynchronous steps present in Δv_{AM} can cause multiple switching actions per (effective) switching period if the series inverter's PWM employs triangular carriers (cf. Figs. 3*e* and *f*). This translates into low-frequency harmonics in v_{BM} (cf. Fig. 4*c*) that are not compatible with a high output filter cutoff frequency. Therefore, it is imperative to realise the series inverter's PWM with sawtooth carriers, whose constant slope within a pulse interval prevents undesired switching actions (cf. Figs. 3*d* and 4*b*).

As the compensating action of the series inverter does only involve switching frequency reactive power exchange with the load, the series inverter's DC bus can be left floating. A slow proportional–integral controller is used to compensate for losses and stabilise the DC bus voltage V_{DC2} by commanding small components in v_{AB} that are in phase with the load current to create (small) active power contributions (cf. Fig. 2). A remaining fluctuation of V_{DC2} at the output frequency can be compensated in the series inverter's PWM.

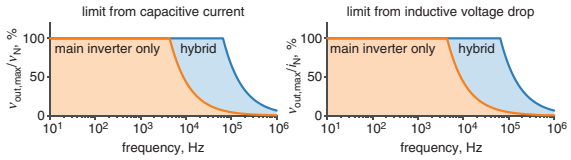

Fig. 5 *Output capabilities over frequency; adding the series inverter ($f_{s2} = 1$ MHz), i.e. implementing the proposed hybrid approach, increases the full-range bandwidth from 4.4 to 65 kHz*

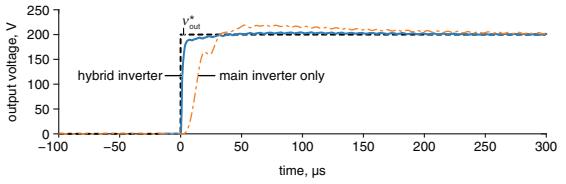

Fig. 6 *Simulated closed-loop response to a reference voltage step for both, system employing only main inverter with corresponding filter or proposed hybrid approach*

Performance evaluation: Considering the topology shown in Fig. 1 and the specifications given in Table 1, the gain in bandwidth that can be realised by complementing the main inverter with a series inverter is evaluated. For both cases, the two-stage LC output filter is designed based on a design space approach [8]. Considering $L_2 = 0.1 \cdot L_1$ and $C_2 = C_1$ [7], a maximum output voltage THD of 0.1% (using an idealised filter characteristic as shown in Figs. 4*a* and *b*) at nominal (resistive) load defines a minimum product L_1C_1, and a maximum output impedance of $< 0.6\,\Omega$ defines a minimum ratio C_1/L_1. The filter capacitors carry a current at the output frequency, which shall sensibly not exceed $0.5 \cdot I_N$ at rated output voltage V_N. Similarly, the inductive voltage drop along $L_1 + L_2$ at the output frequency shall not exceed 85 V at rated output current I_N (corresponding to $|\cos\varphi| = 0.95$). These two conditions set upper bounds for C_1 and L_1, respectively, which depend on the output frequency. The filter design that respects all four conditions for the highest possible output frequency is chosen. For even higher output frequencies, either the output voltage and/or the output current need to be reduced in order not to violate the limits (cf. Fig. 5).

Fig. 5 shows that the full-range bandwidth (i.e. the maximum output frequency) can be increased by more than an order of magnitude if the main inverter is complemented with a series inverter rated at a fraction of the voltage and power only. The significantly higher effective switching frequency of this hybrid inverter system allows for a higher output filter cutoff frequency and hence smaller filter elements. This, in turn, increases the output frequency at which the limits of the capacitive current and/or the inductive voltage drop are reached. Note that the higher effective switching frequency lowers also the effort for EMC filters required by many applications.

Finally, Fig. 6 shows closed-loop simulation results. The response to a step change of the output voltage reference from 0 to 200 V (50%) at nominal (resistive) load is significantly faster for the hybrid inverter system than for the main inverter alone.

Conclusion: In this Letter, we propose a new variant of a hybrid inverter: a main inverter processes the full power and voltage with parallel-interleaved operation of n two-level bridge legs, whose outputs are combined by means of a coupled inductor to generate a multilevel voltage. A series inverter featuring a floating (i.e. without external supply) DC bus with only $1/n$ times the main inverter's DC voltage, which allows for a significantly higher switching frequency, is used to increase the effective switching frequency of the combined output voltage. If the modulation of the series inverter employs sawtooth carriers, this allows for a significantly higher cutoff frequency of the output filter. Considering a 100 kVA, 800 V DC example system, extending the main inverter based on six parallel-interleaved bridge legs switching at 20 kHz with a series inverter operating from a floating 133 V DC bus and switching at 1 MHz (unipolar modulation), allows to increase the full-range output power bandwidth from 4.4 to 65 kHz, which is more than an order of magnitude. Since the series inverter only processes a fraction of the full power and voltage, this improvement comes with relatively little effort and hence cost and only a minor efficiency reduction due to partial power processing. Due to the mostly independent operation of the series inverter, even retrofitting of existing switch-mode amplifiers that generate a multilevel output voltage may be possible. Thus, the proposed hybrid inverter concept is suitable for switch-mode power amplifiers with extreme bandwidth requirements.

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One or more of the Figures in this Letter are available in colour online.

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References

1 Wu, B.: 'High-power converters and AC drives' (John Wiley & Sons, Hoboken, NJ, USA, 2006)
2 Grüning, H.: 'Leistungselektronische Schaltungsanordnung (in German)'. EU Patent EP 0 802 617 A2, 22 October 1997
3 Steimer, P., and Veenstra, M.: 'Converter with additional voltage addition or subtraction at the output'. US Patent 6 621 719 B2, 16 September 2003
4 Manjrekar, M.D., and Lipo, T.A.: 'A hybrid multilevel inverter topology for drive applications'. 13th Annual Applied Power Electronics Conf. and Exposition (APEC), Anaheim, CA, USA, February 1998, pp. 523–529, doi: 10.1109/APEC.1998.653825
5 Stemmler, H.: 'Inverter circuit for supplying current to polyphase motors'. US Patent 3 346 794 A, 10 October 1967
6 Kolar, J.W., Huber, J.E., Krismer, F., Neumayr, D., and Papamanolis, P.: 'Wechselrichter (in German)'. Austrian Patent Appl. A 50231/2017, March 2017
7 Cortes, P., Boillat, D.O., Ertl, H., and Kolar, J.W.: 'Comparative evaluation of multi-loop control schemes for a high-bandwidth AC power source with a two-stage LC output filter'. Int. Renewable Energy Research and Applications Conf. (ICRERA), Nagasaki, Japan, November 2012, pp. 1–10, doi: 10.1109/ICRERA.2012.6477339
8 Boillat, D.O., Krismer, F., and Kolar, J.W.: 'Design space analysis and $\rho - \eta$ Pareto optimization of LC output filters for switch-mode AC power sources', *IEEE Trans. Power Electron.*, 2015, **30**, (12), pp. 6906–6923, doi: 10.1109/TPEL.2015.2393151