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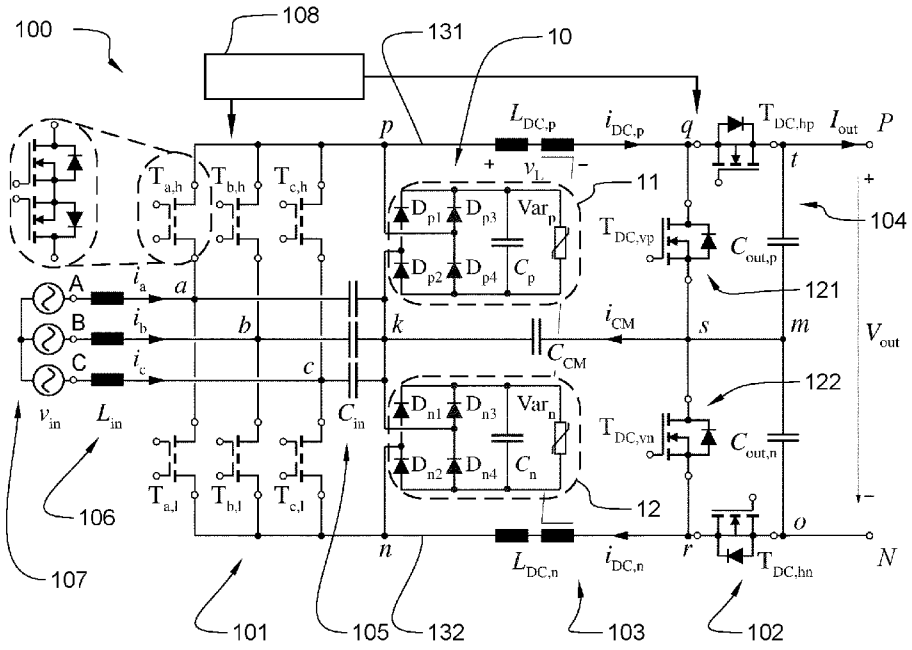

FIG 1

(57) **Abstract:** Current source converter, comprising a first converter stage (101) comprising at least one actively operated switching device ($T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$) configured to switch electric power between at least one first-side node (a, b, c) and at least one switch node (p, n), a DC link (103) comprising an inductive element ($L_{DC,p}$, $L_{DC,n}$) operably coupled to the at least one switch node (p, n), an energy absorbing circuit (10). The energy absorbing circuit (10, 20, 30) and the inductive element form a circulation circuit in which energy stored in the inductive element is configured to circulate when a current path in the first converter stage (101) is interrupted. The current source converter comprises at least one capacitively stabilized voltage node (k, t, o, m) and the energy absorbing circuit comprises a series connection of a clamping diode (D_{p3}, D_{n2}) and

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WO 2022/243423 A1

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an energy absorbing capacitor (C_p, C_n) connected between the at least one switch node (p, n) and the at least one capacitively stabilized voltage node (k, t, o, m).

ELECTRICAL CONVERTER WITH OVERVOLTAGE PROTECTION CIRCUIT

Technical field

[0001] The present invention is related to an electrical converter comprising an overvoltage protection circuit, in particular the present invention is related to a current source converter comprising a passive overvoltage protection circuit for protecting the converter in case of an interruption of the DC-link current.

Background art

[0002] Efficient and robust battery charging power converters are key enablers to accelerate the world's transition to emission-free road transport. Future electric vehicle (EV) chargers are required to cover a wide output voltage range to accommodate different vehicle battery voltages and must allow bidirectional power conversion (i.e., operation as rectifier and as inverter) for the EV batteries to serve as distributed energy storage elements supporting the grid operation. Compared to a conventional boost-type (voltage DC-link) converter approach, the buck-type (current DC-link) converter offers several advantages, e.g., a reduced number of magnetic components, and a sinusoidally varying switched voltage that potentially reduces switching losses. However, due to the current-source behaviour of the buck-type converter's DC-link, the semiconductor switching stage must always be in a configuration that provides a conduction path for the impressed DC-link current. Furthermore, the semiconductor switches of the high-side and low-side commutation cells typically have bi-directional voltage blocking capability which prevents the current to free-wheel when the switches are turned off or fail. When the current path is interrupted, e.g., because of a modulation fault or the loss of a gate driver power supply, significant overvoltages will occur across the affected power semiconductors and lead to failure of these devices.

[0003] Both active and passive protection circuits are known to protect the power semiconductors from destructive overvoltages caused by the interruption of the DC-link current. Active solutions detect a fault situation and then actively turn on an alternative path for the inductive DC-link current. However, it is challenging to realize sufficiently fast-acting detection-reaction timings in a relatively simple way. A fully passive circuit with a short response time is especially crucial in converters realized with SiC MOSFETs, where the overvoltage reaches a breakdown limit in a very short time. In the present disclosure, therefore, passive protection circuits are further considered.

[0004] A first category of passive overvoltage protection circuits involves voltage-limiting devices, such as transient voltage suppression (TVS) diodes and

varistors, or triggered elements, e.g., thyristor-based clamping devices, which are directly connected between the circuit nodes and limit the maximum voltage between them, e.g., between the positive and the negative rail of the DC-link. However, TVS diodes and varistors both add significant parasitic capacitance in parallel to the power semiconductor devices to be protected, which would increase switching losses and lower the converter efficiency. Thyristor-based clamping devices cannot be used to protect fast-switching power semiconductors, such as SiC MOSFETs, due to the risk of parasitic dv/dt-induced triggering.

[0005] A second category of passive overvoltage protection circuits uses diode bridges to clamp the voltages between certain circuit nodes to a capacitively stabilized voltage. During overvoltage clamping, excess energy is transferred from the DC-link inductor into the stabilization capacitor, and ultimately dissipated in a varistor (or some other voltage-limiting device) connected in parallel to that capacitor.

[0006] US 4884182 describes a passive overvoltage protection circuit of the second category employing a clamping mechanism based on a diode bridge. The clamping voltage is defined by the line-to-line voltage. Hence, the voltage rating of the components of the protection circuit, e.g., diodes, capacitors, resistors, are defined by the maximum line-to-line voltage. Furthermore, only the overvoltage generated by the DC-link current in a single flow direction can be limited, and a second circuit is required to limit the overvoltage generated by an opposite flowing DC-link current.

[0007] B. Guo et al., *Overvoltage Protection Scheme for Three- Phase Current Source Converter Built with SiC MOSFETs*, in Proc. of the IEEE Applied Power Electronics Congress and Exposition (APEC), Fort Worth, TX, USA, 16-20 March 2014, pp. 3469-3476, DOI: 10.1109/APEC.2014.6803808 describes an overvoltage protection circuit which again clamps the potential difference between any of the three-phase terminals (a, b, c) and any of the two DC rails (p, n) with a diode bridge consisting of five bridge legs. Furthermore, also in this case the minimum component voltage ratings are defined by the maximum line-to-line voltage. In addition, this specific circuit is not fully passive since it uses triggered elements to clamp the diode bridge's DC-side voltage and to dissipate the excess power, increasing in complexity compared to a fully passive circuit.

Summary

[0008] There is therefore a need in the art to provide passive overvoltage protection circuits for current DC-link converters which are simpler in terms of component count. There is a need in the art to provide overvoltage protection circuits for current DC-link converters having reduced voltage ratings for the components. There is a need in

the art to provide such overvoltage protection circuits which are more reliable, economical, allow faster detection of faulty conditions and/or which can be used for bidirectional power flow.

[0009] According to a first aspect of the invention, there is therefore provided a current source converter as set out in the appended claims. A current source converter as described in the present disclosure comprises a first converter stage coupled to a current DC link. The first converter stage comprises at least one actively operated switching device configured to switch electric power between at least one node at a first side of the converter stage and at least one switch node, e.g. at a second side of the converter stage. The current DC link is operably coupled to the at least one switch node. The at least one actively operated switching device is advantageously configured to have a bidirectional voltage blocking capability and is advantageously a semiconductor switching device. Advantageously, the first converter stage comprises a plurality of actively operated switching devices configured to switch electric power between an AC signal at a plurality of nodes at the first side and a DC signal at a pair of switch nodes. The first converter stage can comprise a pair of commutation cells each having a plurality of actively operated switches to convert between an electric signal, e.g. an AC signal, at a plurality of first-side nodes and an electric signal, e.g. a DC signal, at (at least) two switch nodes to which the DC link is operably coupled. Advantageously, the first converter stage is an AC/DC stage, advantageously a three-phase AC to DC stage configured to convert between an AC signal at three or more phase nodes and a DC signal at a first switch node and a second switch node. In this case, the commutation cells advantageously comprise three actively operated switches each, e.g. arranged in three half-bridge legs.

[0010] The current DC link is one comprising at least one inductive element, e.g. for storing inductive energy, such as an inductor. One terminal of the inductive element can be connected to the respective switch node. The DC link advantageously comprises a first (e.g. positive) DC rail connected to the switch node. The DC link can comprise a second (negative) DC rail connected to a second switch node. Each of the first and possibly second DC rail can comprise a respective inductive element.

[0011] The current source converter comprises at least one capacitively stabilized voltage node, such as a node at a terminal of a filter capacitor, which may be arranged anywhere in the current source converter, e.g. coupled to the first side nodes or at the opposite end of the DC link, e.g. a node of a DC bus.

[0012] The current source converter comprises an energy absorbing circuit which acts as an overvoltage protection mechanism according to aspects as disclosed herein. The energy absorbing circuit and the inductive element form a circulation circuit in which energy stored in the inductive element is configured to circulate when a current path in the first converter stage is interrupted, in particular in case of a fault or a shut down or turn off of the at least one actively operated switching device. The energy absorbing circuit comprises at least one series connection of a clamping diode and an energy absorbing capacitor, connected between a switch node of the second side and one of the capacitively stabilized voltage nodes. A varistor can further be connected in parallel to the capacitor to limit the increase of the capacitor voltage and ultimately dissipate the excess energy.

[0013] The energy absorbing circuit according to the present disclosure is a (completely) passive overvoltage protection circuit, allowing to achieve fast and reliable protection without requiring active devices, such as triggered or thyristor-based devices. A further advantage of the energy absorbing circuit is that it requires a reduced number of components. Particularly only four diodes are required to realize an overvoltage protection both for the upper and lower DC-rail of the DC-link, and for both directions of power flow.

[0014] Furthermore, the energy absorbing capacitor is connected in series with a clamping diode, between a switch node of the converter and the capacitively stabilized voltage node allowing the capacitor to charge to the highest voltage that occurs between the switch node and the capacitively stabilized voltage node during normal operation and to stay charged to this voltage. As a result, the energy absorbing circuit becomes virtually 'invisible' for the switching stage and does not influence the normal operation of the converter. Advantageously, a capacitively stabilized voltage node which is already present in the converter is used. In one particularly advantageous embodiment, a star-point of AC side filter capacitors is used as the capacitively stabilized voltage node, which hence acts as an artificial neutral point further reducing the voltage rating of the components of the energy absorbing circuit.

[0015] In one advantageous embodiment, a single diode full bridge circuit is used with inputs connected between the positive and negative DC rails of the DC link, while the outputs are connected to energy absorbing capacitors which are further connected to a capacitively stabilized voltage node. In particular, the outputs of the diode bridge are connected across a series connection of energy absorbing capacitors. A midpoint of the series connection of energy absorbing capacitors is advantageously connected to the capacitively stabilized voltage node, in particular a star-point of AC-side

filter capacitors or a voltage node of the DC-bus (e.g., a middle voltage node of the DC-bus). This solution features a minimal component count and allows to minimize the voltage rating of the energy absorbing capacitors.

[0016] In an alternative advantageous embodiment, two diode full bridge circuits are used, one for each of the positive and negative DC rails of the DC link. An energy absorbing capacitor is connected across the outputs of each diode bridge circuit to absorb the energy stored in the DC-link inductor during clamping. The inputs of the diode bridge circuit are connected between a respective node of the second side of the converter stage and the capacitively stabilized voltage node, which advantageously is the star-point of the AC side filter capacitors (artificial neutral point). As a result, a symmetrical structure with two diode full-bridges is obtained, limiting the potential differences between the capacitively stabilized voltage node, e.g. the artificial neutral point, and the positive or the negative DC rail, respectively, which reduces the voltage rating for the diodes.

[0017] Even in the case with two symmetrical diode full bridge circuits, the energy absorbing (overvoltage protection) circuit according to aspects of the invention thus features a reduced number of diode bridge legs, i.e., only four diode bridge legs are required compared to at least five as described in the prior art. In addition, the symmetric nature of such a structure, which essentially uses one diode full-bridge for the high-side and one diode full-bridge for the low-side commutation cell, facilitates a fully symmetrical PCB layout with low parasitic loop inductances. A realization using only surface-mounted devices further reduces the construction effort. Finally, the energy absorbing circuits according to aspects of the present disclosure are easy to adapt in high power systems with larger DC-link current amplitudes. Furthermore, the necessary voltage ratings of the diodes, the capacitors, and the varistors are lower, which decreases the cost and volume of the protection circuitry. The energy absorbing circuits as disclosed herein only add little additional capacitive load at the switch node (only the small parasitic capacitances of the diodes), which minimizes any negative influence on the converter switching performance.

[0018] According to a second aspect of the disclosure, there is provided a battery charging system comprising a power supply. The power supply comprises a current source converter according to the present disclosure.

[0019] According to a third aspect of the present disclosure, there is provided an electric motor drive system comprising a power supply. The power supply comprises a current source converter according to the present disclosure.

Brief description of the figures

[0020] Aspects of the invention will now be described in more detail with reference to the appended drawings, wherein same reference numerals illustrate same features and wherein:

[0021] Figure 1 represents a three-phase bidirectional buck-boost current DC-link converter comprising an overvoltage protection circuit according to an aspect of the present disclosure.

[0022] Figure 2 represents in dashed line a possible current path through the converter of Fig. 1 when the upper diode bridge circuit of the overvoltage protection circuit is activated.

[0023] Figure 3 represents plots of simulation results of continuous operation of the converter of Fig. 1 in which $T_{a,h}$ fails to open at t = 5 ms. Characteristic voltages are shown, including the blocking voltages v_{ap}, v_{bp}, v_{cp} of the switches of the high-side commutation cell and blocking voltages v_{an}, v_{bn}, v_{cn} of the switches of the low-side commutation cell, the input voltages v_{pk}, v_{kn} of the upper and lower diode bridge circuits, and the bias voltage v_{bias} derived from the input capacitor voltages v_{ak}, v_{bk}, v_{ck}, the DC-link currents $i_{DC,p}$ and $i_{DC,n}$, and the voltages varp and varn across the varistors var_p and var_n of the overvoltage protection circuit.

[0024] Figure 4 represents plots of simulation results of continuous operation of the converter of Fig. 1 in which $T_{a,h}$ fails to open at t = 10 ms. Characteristic voltages are shown, including the blocking voltages v_{ap}, v_{bp}, v_{cp} of the switches of the high-side commutation cell and blocking voltages v_{an}, v_{bn}, v_{cn} of the switches of the low-side commutation cell, the input voltages v_{pk}, v_{kn} of the upper and lower diode bridge circuits, and the bias voltage v_{bias} derived from the input capacitor voltages v_{ak}, v_{bk}, v_{ck}, the DC-link currents $i_{DC,p}$ and $i_{DC,n}$, and the voltages varp and varn across the varistors var_p and var_n of the overvoltage protection circuit.

[0025] Figure 5 represents plots of simulation results of continuous operation of the converter of Fig. 1 in which all switches are turned off at t = 10 ms. Characteristic voltages are shown, including the blocking voltages v_{ap}, v_{bp}, v_{cp} of the switches of the high-side commutation cell and blocking voltages v_{an}, v_{bn}, v_{cn} of the switches of the low-side commutation cell, the input voltages v_{pk}, v_{kn} of the upper and lower diode bridge circuits, and the bias voltage v_{bias} derived from the input capacitor voltages v_{ak}, v_{bk}, v_{ck}, the DC-link currents $i_{DC,p}$ and $i_{DC,n}$, and the voltages varp and varn across the varistors var_p and var_n of the overvoltage protection circuit.

[0026] Figure 6 represents a diagram of the converter of Fig. 1 further comprising a detection circuit coupled to each of the upper and lower diode bridge

circuits to detect activation of the overvoltage protection circuit and send a signal to the control unit.

[0027] Figure 7 represents a diagram of the converter of Fig. 6 further comprising voltage-limiting devices across the filter capacitors.

[0028] Figure 8 represents a diagram of a current source converter comprising an overvoltage protection circuit according to another embodiment of the present disclosure, including a single diode full bridge circuit.

[0029] Figure 9 represents in dashed line a possible current path through the converter of Fig. 8 when the overvoltage protection circuit is activated.

[0030] Figure 10 represents a diagram of the current source converter of Fig. 8, in which the energy dissipation device in the form of a varistor is connected across both cascaded energy absorbing capacitors of the overvoltage protection circuit.

[0031] Figure 11 represents a diagram of a current source converter comprising an overvoltage protection circuit according to yet another embodiment of the present disclosure, comprising a series connection of a clamping diode and an energy absorbing capacitor.

[0032] Figure 12 represents a diagram of a battery charging system incorporating a current source converter according to the present disclosure.

[0033] Figure 13 represents a diagram of a motor drive system incorporating a current source converter according to the present disclosure.

Detailed Description

[0034] Referring to Fig. 1, a first embodiment of an overvoltage protection circuit 10 according to aspects of the present disclosure is presented in an exemplary current source converter 100. In Fig. 1, the current source converter 100 is shown as a three-phase bidirectional buck-boost current DC-link converter, although it should be noted that overvoltage protection circuits according to aspects as described herein are generally applicable to all kinds of current source converters, particularly converters comprising a first converter stage having an actively operated commutation cell coupled to a current DC link, such as single-stage current source rectifiers/inverters, back-to-back current DC-link AC/AC converters, and two-stage current DC-link AC/DC converters where the buck CSR-stage is implemented as the front-end such as in the example used here.

[0035] Current source converter 100 comprises a first converter stage 101 operable to convert between an AC signal at the three AC nodes *a*, *b*, *c* and a DC signal at switch nodes *p* and *n*. The first converter stage 101 is illustrated in Fig. 1 as a three-phase buck-type current source rectifier (CSR) stage. The CSR stage 101 comprises six

semiconductor switches $T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$ having bidirectional voltage blocking capability, advantageously arranged in three half-bridge legs, e.g. with a high-side commutation cell ($T_{a,h}$, $T_{b,h}$, $T_{c,h}$) and a low-side commutation cell ($T_{a,l}$, $T_{b,l}$, $T_{c,l}$), and operable to switchingly connect the AC nodes *a*, *b*, *c* to the switch nodes *p*, *n*. Each of these semiconductor switches can be formed by anti-series connecting two discrete semiconductor switches having unidirectional voltage blocking capability, e.g. SiC metal oxide semiconductor field effect transistors (MOSFETs) possibly with external anti-parallel diodes. Alternatively, the semiconductor switches of the CSR stage 101 can be formed as monolithic bidirectional transistors, such as GaN field effect transistors, in particular enhanced-mode field effect transistors (e-FET).

[0036] A DC-link 103 connects the CSR stage 101 to any subsequent converter stage of the current source converter 100, or to DC terminals *P*, *N*. In the present illustrative example, the current source converter 100 comprises a second converter stage 102, illustrated in Fig. 1 as a three-level boost-type DC/DC-stage even though other implementations are possible, e.g. as a two-level boost DC/DC stage. Such a boost DC/DC converter stage comprises at least one, advantageously two active semiconductor switches $T_{DC,vp}$ and $T_{DC,vn}$ series connected between nodes *q* and *r* of the second converter stage, where the two semiconductor switches create a common node *s*. An active semiconductor switch $T_{DC,hp}$ and/or $T_{DC,hn}$ advantageously allows for bidirectional power flow between the switch nodes *p*, *n* and the DC terminals *P*, *N* respectively. The DC/DC stage 102 e.g. comprises an upper boost circuit 121 and a lower boost circuit 122 stacked between the DC terminals *P* and *N*. The upper and lower boost circuits 121, 122 comprise the common node *s*. Each of the upper and lower boost circuits can be implemented with semiconductor switches $T_{DC,vp}$ and $T_{DC,hp}$ for the upper boost circuit 121 and semiconductor switches $T_{DC,vn}$ and $T_{DC,hn}$ for the lower boost circuit 122. Other implementations are possible. By way of example, either one or both the upper and lower boost circuits can be implemented as a flying capacitor circuit.

[0037] The DC-link 103 hence connects the CSR stage 101 and the DC/DC stage 102. In particular, the DC-link 103 connects the switch nodes *p*, *n* of the CSR stage 101 to the input nodes *q*, *r* of the DC/DC stage 102. The DC-link 103 comprises an upper (positive) DC rail 131 connected to switch node *p* (connecting *p* to *q*) and a lower DC rail 132 connected to switch node *n* (connecting *n* to *r*). Either one or both of the upper and lower DC rails 131, 132 comprises an inductive element, e.g. provided as a high-frequency filter and/or for storing energy, such as inductor $L_{DC,p}$ and $L_{DC,n}$ respectively operably connected to the respective switch node *p* and *n*. The inductors $L_{DC,p}$ and $L_{DC,n}$ can each comprise a common-mode inductor part, a differential mode inductor part or

both. The DC-link 103 can further comprise a common mode (CM) capacitor C_{CM} connected between the star-point k of the input capacitors C_{in} and the common node s. The common mode capacitor C_{CM} advantageously allows to significantly reduce the high-frequency components of CM noise.

[0038] An input filter 106 is advantageously arranged between the AC terminals A, B, C and the AC voltage nodes *a*, *b*, *c*. The input filter can comprise a network 105 of filter capacitors C_{in} which are star-point-connected to star-point *k*. This star-point *k* advantageously allows to create an artificial neutral point. Additionally, the input filter can comprise filter inductors L_{in}.

[0039] The current source converter 100 further can comprise a DC bus 104 having bus capacitors $C_{out,p}$ and $C_{out,n}$ series connected across the DC terminals *P* and *N*. A middle voltage node *m* (common node) of bus capacitors $C_{out,p}$ and $C_{out,n}$ is advantageously connected to common node *s* of the boost DC/DC stage 102 such that nodes *s* and *m* are at a same electrical potential.

[0040] Converter 100 can be operated by a control unit 108 configured to provide appropriate activation signals to the semiconductor switches of the first converter stage 101 and/or the second converter stage 102, e.g. to operate them by pulse width modulation.

[0041] The overvoltage protection circuit 10 features a symmetrical structure for the positive rail 131 and the negative rail 132 of the DC-link 103. In particular, overvoltage protection circuit 10 comprises two diode full-bridge circuits 11, 12. The upper diode bridge circuit 11 is formed of diodes D_{p1}, D_{p2}, D_{p3}, and D_{p4} arranged in a full-bridge configuration. The inputs of diode bridge circuit 11 are connected between switch node *p* and the star-point *k*. The upper diode bridge circuit limits the potential difference between the positive DC rail 131 and the star-point *k*, which acts here as an artificial neutral point, and therefore allows to provide overvoltage protection for the semiconductor switches of the high-side commutation cell. The lower diode bridge circuit 12 is formed of diodes D_{n1}, D_{n2}, D_{n3}, and D_{n4} arranged in a full-bridge configuration. The inputs of lower diode bridge circuit 12 are connected between star-point *k* and switch node *n*. The lower diode bridge circuit limits the potential difference between the negative DC rail 132 and the star-point *k*, and therefore allows to provide overvoltage protection for the semiconductor switches of the low-side commutation cell.

[0042] A capacitor C_p, C_n is connected across the outputs of the upper and lower diode bridge circuits 11, 12 respectively and is configured to absorb the DC-link inductor energy during clamping. A varistor var_p, var_n is connected in parallel to the capacitors C_p, C_n respectively to limit the corresponding voltage increase and ultimately

to dissipate the excess energy. Any other suitable energy dissipating means can be used instead of a varistor. It will be convenient to note that for safety reasons, an additional discharging resistor (not shown) can be placed in parallel to each capacitor C_p, C_n.

[0043] The mode of operation of the overvoltage protection circuit 10 involves three different states, which are discussed in the following for rectifier operation, i.e., power flow from the AC-side 107 to the DC-side and hence positive DC-link currents $i_{DC,p}$ and $i_{DC,n}$. Because of the full-bridge structure of the protection circuit 10, overvoltage protection also works analogously for inverter operation.

(i) Standby operation

[0044] During normal operation of the converter 100, the overvoltage protection circuit 10 is inactivated and all the diodes of the upper and lower diode bridge circuits 11, 12 are reverse-biased. The capacitors, C_p and C_n, remain charged at the peak value of the phase-to-neutral voltage (i.e., v_{ak}, v_{bk} and v_{ck}), which thus defines the minimum voltage rating of the diodes, capacitors, and varistors. Additional parasitic capacitances at the switch nodes are given by the parasitic capacitances of the diodes, which typically are much smaller than the output capacitances of the converter's main power semiconductors $T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$. Hence, the overvoltage protection circuit 10 advantageously has minimal influence on the switching behaviour and ultimately on the converter efficiency.

(ii) Overvoltage protection in case of a fault in one commutation cell

[0045] During rectifier operation, the DC-link currents, $i_{DC,p}$ and $i_{DC,n}$, are positive to transfer energy from the AC side 107 to the DC side (nodes *P*, *N*). Referring to Fig. 2 and assuming an open-circuit fault (e.g., because of a loss of gate driver power) of at least one of the switches of the high-side commutation cell ($T_{a,h}$, $T_{b,h}$, $T_{c,h}$) of the CSR-stage 101, when $i_{DC,p}$ is commutated to the faulty switch, it will first discharge the output capacitor of the respective transistor to a negative value, thereby pulling node *p* negative with respect to *k*. As a result, diodes D_{p1} and D_{p4} of the diode bridge circuit 11 will conduct once the potential difference of nodes *k* and *p*, i.e. $-v_{pk}$, is larger than the standby voltage of C_p, i.e., the peak value of the phase-to-neutral voltage. This creates a current path from the AC node *a* through the star-point *k* and further through diode D_{p1}, capacitor C_p and diode D_{p4} of the circuit 11, to node *p* and the positive DC-rail 131 as shown by the dashed line in Fig. 2. This current path is further closed by the capacitors $C_{out,p}$ and $C_{out,n}$ of the DC bus 104, the negative DC-rail 132 and one of the switches of the low-side commutation cell ($T_{a,l}$, $T_{b,l}$, $T_{c,l}$) of the CSR stage 101. The current path that is created allows to transfer the DC-link inductive energy (stored in inductor $L_{DC,p}$) into the capacitor C_p. Correspondingly, the capacitor voltage increases until it is clamped by

the varistor var_p, which ultimately dissipates the DC-link energy. The corresponding voltage is applied between the terminals of the protection circuit and contributes to reducing the current in the DC-link inductors towards zero.

[0046] In the above working example, the lower diode bridge circuit 12 is not in operation. It will however be convenient to note that an equivalent discussion applies to the protection in case of open-circuit fault of a switch of the low-side commutation cell ($T_{a,l}$, $T_{b,l}$, $T_{c,l}$) of the CSR stage 101 activating the lower bridge circuit 12 in an analogous manner as above.

[0047] During inverter operation, the DC-link currents, $i_{DC,p}$ and $i_{DC,n}$, are negative to transfer energy from the DC nodes *P*, *N* to the AC side 107. Assuming now a same open-circuit fault (e.g., because of a loss of gate driver power) of at least one of the switches of the high-side commutation cell ($T_{a,h}$, $T_{b,h}$, $T_{c,h}$) of the CSR-stage 101, when $i_{DC,p}$ is commutated to the faulty switch, it will charge the output capacitor of the respective transistor, thereby increasing the potential of node *p*. As a result, diodes D_{p3} and D_{p2} will conduct once the potential difference v_{pk} is larger than the standby voltage of C_p, i.e., the peak value of the phase-to-neutral voltage. A current path is now created for the DC-link current $i_{DC,p}$ from node *p* through diode D_{p3}, capacitor C_p and diode D_{p2} to the star-point *k* and further towards the AC side 107 through nodes *a*, *b*, *c*. Correspondingly, the voltage of capacitor C_p increases until it is clamped by the varistor var_p, which ultimately dissipates the DC-link energy. The operation in case of an open-circuit fault of the switches of the low-side commutation cell ($T_{a,l}$, $T_{b,l}$, $T_{c,l}$) of the CSR-stage 101 is analogous considering the diodes D_{n2}, D_{n3} and capacitor C_n.

(iii) Overvoltage protection in case of faults in both commutation cells

[0048] In case of an open-circuit condition of transistors in both the high-side and the low-side commutation cells, both the upper and lower diode bridge circuits 11, 12 become active. The current path as shown in Fig. 2 (in case of rectifier operation) would in such case pass through node *n*, diode D_{n1}, capacitor C_n and diode D_{n4} of the lower diode bridge circuit 12 rather than passing through the low-side commutation cell ($T_{a,l}$, $T_{b,l}$, $T_{c,l}$) as in Fig. 2. In case of inverter operation, the current flows from node *k* through diode D_{n3}, capacitor C_n and diode D_{n2} of the lower diode bridge circuit 12 to node *n*. Hence, if both diode bridge circuits 11, 12 are active, they form a (closed) conduction path for the DC-link current (through the star-point *k*) that does not involve the filter capacitors C_{in}. It will be convenient to note that such a situation can also occur in case of a converter trip (i.e. shutting down of the converter), if the trip-state is such that all transistors are switched off.

Maximum voltage clamping experiments

[0049] Maximum voltage clamping simulations will now be presented for the latter two modes of operation (ii) and (iii) of the overvoltage protection circuit 10 in case of rectifier operation.

[0050] Referring to operation mode (ii) above, the theoretical maximum voltage V_{max} across a transistor is the sum of the clamp voltage V_{clamp} of the varistor var_p and the voltage V_{in} of the input capacitor C_{in}, i.e., the worst-case peak phase-to-neutral voltage $\hat{V}_{ph}$ during normal operation. However, when either the upper or the lower diode bridge circuit 11, 12 is active, the DC-link current $i_{DC,p}$ is injected into the star-point k, causing an asymmetry of the voltages of the input filter capacitors C_{in}. The corresponding bias can be expressed by the voltage $v_{bias} = v_{ak} + v_{bk} + v_{ck}$, which remains zero during normal operation (assuming symmetrical grid voltages). When either the upper or the lower diode bridge circuit 11, 12 is active, v_{bias} increases and adds on top of one phase-to-neutral voltage exclusively in a worst-case scenario, which would lead to a corresponding increase of the maximum clamping voltage. It will be convenient to note that the bias voltage will not change if both the upper and the lower diode bridge circuits 11, 12 are active, as is the case in operation mode (iii) described above, or when all power semiconductors are turned off, e.g., as a result of a system-level trip.

[0051] When one diode bridge circuit 11, 12 is active, its respective capacitor C_p, C_n is essentially connected in series to one of the filter capacitors C_{in} (which one depends on the switching state of the unaffected commutation cell), i.e., the same DC-link current $i_{DC,p}$, $i_{DC,n}$ respectively flows through either capacitor. The capacitances of the overvoltage protection circuit capacitors (C_p, C_n) are advantageously selected much smaller than the capacitances of the filter capacitors C_{in}, e.g. 75% of the capacitance of C_{in} or less, advantageously 50% or less. Thus, the voltage of the protection circuit capacitor increases much faster than the bias voltage, which facilitates a fast detection of the fault condition.

[0052] To illustrate the corresponding difference in time scales, two scenarios were investigated, showing the behaviour of the converter for the case in which one transistor of the high-side commutation cell fails (and hence the upper diode bridge circuit 11 acts whenever the DC-link current would be commutated to this transistor), but the converter would continue to operate (i.e., no detection and no trip). Figs. 3 and 4 show exemplary simulations for a 10 kW buck-boost CSR system as shown in Fig. 1 connected to a three-phase 400 V AC grid. The circuit component values and simulation parameters are listed in Table 1. A two-stage differential mode (DM) EMI filter between

terminals A, B, C and nodes *a*, *b*, *c*, is considered in the simulation (not shown in schematic).

Table 1: Circuit component values and simulation parameters

Symbol	Description	Value
f_{sw}	Switching frequency (both stages)	100 kHz
C_{in}	Input capacitance	6 µF
$L_{DC,DM}$	DM DC-link inductance	270 µH
$L_{DC,CM}$	CM DC-link inductance	14 mH
C_{CM}	CM filter capacitance	80 nF
$C_{out,p}$, $C_{out,n}$	Output capacitance	15 µF
$L_{EMI,DM}$	DM EMI inductance	15 µH
$C_{EMI,DM}$	DM EMI capacitance	3 µF

[0053] In a first simulation scenario as shown in Fig. 3, failure (open-circuit) of $T_{a,h}$ occurred at t = 5 ms when the (local) conduction time of $T_{a,h}$ is at its maximum during the mains period. The upper diode bridge circuit 11 is activated, and the voltage across its capacitor C_p increases very quickly, as seen by the increase of the voltage over the varistor var_p (shown as varp in Fig. 3). The DC-link currents $i_{DC,p}$ (shown as Idcp) and $i_{DC,n}$ (shown as Idcn) quickly decay to zero and stay at zero due to the comparably small inductance value, and because the overvoltage protection circuit 10 is active for a relatively long time (defined by the failed transistor's would-be conduction time). It can be seen that the bias voltage (vbias) increases on a slower time scale. A significant increase of the DC-link current and of v_{bias} occurs only in the next sector of the mains period, where switching states with shorter conduction intervals of the faulty transistor are used. These simulation results indicate that there is ample time to detect the activation of the overvoltage protection circuit and to trip the converter, long before the bias voltage increases significantly.

[0054] In the second scenario shown in Fig. 4, failure (open-circuit) of $T_{a,h}$ occurred at t = 10 ms when the (local) conduction time of $T_{a,h}$ is at its minimum during the mains period. Again, the upper diode bridge circuit 11 is activated, and the voltage across its capacitor C_p increases very quickly (shown as varp in Fig. 4). However, the DC-link currents $i_{DC,p}$, $i_{DC,n}$ (shown as Idcp and Idcn respectively) are only slightly influenced because switching states involving intact transistors dominate and allow the controller to maintain the DC-link current close to its reference value. On the other hand, v_{bias} increases due to the resulting asymmetrical currents in the filter capacitors C_{in}, but

again on a time scale in the millisecond range, i.e., relatively slowly. Thus, also this simulation indicates that there is ample time to detect the activation of the protection circuit and to trip the converter, long before the bias voltage increases significantly.

[0055] If only one of the upper and lower diode bridge circuits 11, 12 becomes active, the bias voltage increases due to the asymmetric currents in the input filter capacitors C_{in}, which ultimately would lead to the voltage across the power semiconductors exceeding their ratings. Conversely, when both protection circuits are active, the bias voltage does not increase further, as the DC-link current path does not involve any of the filter capacitors C_{in} anymore.

[0056] In case of an open-circuit condition of transistors in both the high-side and the low-side commutation cells, both upper and lower diode bridge circuits 11, 12 become active. Note that such a situation also occurs in case of a converter trip, if the trip-state is such that all transistors are switched off. As already mentioned above, if both protection circuits are active, they form a conduction path for the DC-link current that does not involve the filter capacitors C_{in}. Hence, the bias voltage remains unaffected (i.e., stays at zero). Simulation results of such a situation are shown in Fig. 5 when all switches are turned off at t = 10 ms. From the simulation graphs of Fig. 5 it can be seen that the blocking voltages v_{ap}, v_{bp}, v_{cp} of the switches of the high-side commutation cell and the blocking voltages v_{an}, v_{bn}, v_{cn} of the switches of the low-side commutation cell remain always under the avalanche breakdown limit (1200 V), and no bias voltage is accumulated. The DC-link energy is dissipated in the varistors of both diode bridge circuits 11, 12.

[0057] From the foregoing, it can be derived that the overvoltage protection circuit allows to easily detect a fault situation that leads to one or both protection circuits being triggered. Such a detection allows the converter to be shut down in a safe way (referred to as trip), especially within a few switching cycles and in particular before v_{bias} increases to critical values. Additionally, the energy absorption capability of the varistors (or other voltage-limiting elements) is typically limited, i.e., the fault state cannot persist for too long. In general, the allowed fault state duration is determined by the varistor power dissipation capability if the varistors allow to dissipate the power within a time frame shorter than the time required for a critical increase of the bias voltage.

[0058] Referring to Fig. 6, the converter 100 can be equipped with a detection circuit 13, 14 coupled to a respective diode bridge circuit 11, 12 and coupled to control unit 108. The detection circuit 13, 14 is configured to detect activation of the respective diode bridge circuit 11, 12 and to emit a fault signal 109 upon such detection. The fault signal 109 is sent to the control unit 108. Control unit 108 can be configured to

initiate a shut down (trip) of the converter 100 following receipt of the fault signal 109, e.g. by commanding all (actively operated) switches to the off state. With all switches of the converter turned off and assuming the converter was operating in rectifier mode prior to shut down, the diodes D_{n1} and D_{n4} of the lower diode bridge circuit 12 start conducting to close the DC-link current conduction path. As stated previously, in case of inverter operation, diodes D_{n2} and D_{n3} would start conducting instead. Finally, the DC-link inductive energy will be dissipated in the two varistors of the upper and the lower diode bridge circuits.

[0059] One exemplary embodiment of a detection circuit 13, 14 is configured to measure the voltage over the capacitor C_p, C_n of the respective upper or lower diode bridge circuit 11, 12, and to compare this voltage to a predetermined value. If the measured voltage over C_p or C_n is higher than the predetermined value, for instance 500 V, the detection circuit 13, 14 is configured to emit a fault signal 109 which is sent to the control unit 108.

[0060] Alternative solutions for the detection circuit 13, 14 are to measuring the current through the respective varistor, and comparing it to a reference value expected during normal operation. Alternatively, the fault signal can be derived from already available measurements in the converter 100, e.g. measurements that are required for the closed-loop control of the converter and are already used by control unit 108. In general, various measurements can be used as basis for a fault detection signal. By way of example, the detection circuit can be configured to measure the bias voltage as derived from the measured filter capacitor voltages and/or the DC-link current deviation from a reference value and compare either one or both to a threshold value. A fault signal can be generated by the detection circuit when the threshold value is exceeded. Furthermore, combinations of such characteristics can be used to improve the selectivity and avoid false error detection (considering, for example, that a deviation from the DC-link current reference occurs also during load steps, or that grid voltage asymmetries also lead to a non-zero bias voltage). Processed quantities, such as the rate of change of a signal, may be considered as well.

[0061] As shown in Fig. 6, any other energy dissipation (and voltage clamping) device 15 can be used instead of the varistors var_p and var_n, such as single energy dissipation devices, e.g. resistors, TVS diodes, and thyristor-based triggered devices, or combination of several single devices, e.g., series-connection of varistors with thyristor-based triggered devices to achieve a sharp dynamic performance with low standby leakage current.

[0062] Referring to Fig. 7, voltage-limiting devices 151 (e.g., varistors) can be provided across the input filter capacitors (C_{in}), i.e., across nodes *a-k*, *b-k*, and *c-k*, allowing the maximum clamping voltage across any transistor to be defined as a clamping voltage of these voltage-limiting devices 151 and the clamping voltage of the varistors var_p (or other voltage limiting and energy dissipation devices) used in the protection circuit 10. Thus, the increase of the bias voltage can be limited when the converter 100 would continue operation after one of the diode bridge circuits 11, 12 becomes active. Even though the limited energy absorption capability of the voltage-limiting devices 151 would still require detect-and-trip action, this embodiment advantageously can increase the time available for this, especially in systems with small filter capacitors. Considering a 400 V grid and 1200 V power semiconductors, all voltage-limiting devices (i.e., var_p, var_n of the protection circuit 10 as well as devices 151) require a rated RMS voltage of 230 V and a typical clamping voltage of less than 600 V (i.e., including some margin regarding the semiconductor breakdown voltage rating).

[0063] Referring to Fig. 8, current source converter 200 is identical to current source converter 100 except for the overvoltage protection circuit 20, which is configured as a single diode full-bridge circuit 21 with diodes D_{p1}, D_{p3}, D_{n2}, D_{n4}. The inputs of the diode bridge circuit 21 are now connected between nodes *p* and *n*. The outputs of the diode bridge circuit 21 are connected to capacitors C_p and C_n of the overvoltage protection circuit 20, respectively. Capacitor C_p is connected between one output of the diode bridge circuit 21 and the star-point *k*, while capacitor C_n is connected between the other output of diode bridge circuit 21 and the star-point *k*. Such a configuration allows the overvoltage protection functionality to be realized with a reduced number of diodes. However, a higher voltage rating of the diodes is required in this case. The standby voltage of the capacitors C_p and C_n is defined by the maximum potential difference between the DC-link rails (*p*, *n*) and the star-point *k*, i.e., the peak value of the phase-to-neutral voltage, similar to the overvoltage protection circuit 10 of Fig. 1. However, the minimum diode voltage rating for diode bridge circuit 21 is twice the peak value of the phase-to-neutral voltage, e.g. 650 V diodes are required when considering a 400 V grid. The rated voltage of the varistors var_p and var_n is the same as the voltage rating of the respective capacitors C_p and C_n, and the maximum semiconductor clamping voltage is still the sum of the clamp voltage of the varistor var_p, var_n and the voltage of the filter capacitor C_{in}.

[0064] During normal operation of the converter 200, the overvoltage protection circuit 20 is inactivated and all the diodes of the diode bridge circuit 21 are reverse-biased. The capacitors, C_p and C_n, remain charged at the peak value of the

phase-to-neutral voltage (i.e., v_{ak}, v_{bk} and v_{ck}). During rectifier operation, the DC-link currents, $i_{DC,p}$ and $i_{DC,n}$, are positive to transfer energy from the AC side 107 to the DC side (nodes P, N). Assuming now an open-circuit fault (e.g., because of a loss of gate driver power) of at least one of the switches of the high-side commutation cell ($T_{a,h}$, $T_{b,h}$, $T_{c,h}$) of the CSR-stage 101, when $i_{DC,p}$ is commutated to the faulty switch, it will first discharge the output capacitor of the respective transistor to a negative value, thereby pulling node *p* negative with respect to *k*. As a result, diode D_{p1} will conduct once the potential difference between nodes *k* and *p*, i.e. $-v_{pk}$ is larger than the standby voltage of C_n, i.e., the peak value of the phase-to-neutral voltage. This creates a current path from the AC node *a* through the star-point *k* and capacitor C_n towards node *p* and the positive DC-rail 131 as shown by the dashed line in Fig. 9. This current path is further closed by the capacitors $C_{out,p}$ and $C_{out,n}$ of the DC bus 104, the negative DC-rail 132 and the switches of the low-side commutation cell ($T_{a,l}$, $T_{b,l}$, $T_{c,l}$) of the CSR stage 101. The current path that is created allows to transfer the DC-link inductive energy (stored in inductor $L_{DC,p}$) into the capacitor C_n. Correspondingly, the voltage of capacitor C_n increases until it is clamped by the varistor var_n, which ultimately dissipates the DC-link energy. The corresponding voltage is applied between the terminals of the protection circuit and contributes to reducing the current in the DC-link inductors towards zero.

[0065] In the above working example, the capacitor C_p remains at standby voltage. It will however be convenient to note that an equivalent discussion applies to the protection in case of fault of a switch of the low-side commutation cell ($T_{a,l}$, $T_{b,l}$, $T_{c,l}$) of the CSR stage 101 considering diode D_{n4} and capacitor C_p.

[0066] During inverter operation, the DC-link currents, $i_{DC,p}$ and $i_{DC,n}$, are negative to transfer energy from the DC nodes P, N to the AC side 107. Assuming now an open-circuit fault (e.g., because of a loss of gate driver power) of at least one of the switches of the high-side commutation cell ($T_{a,h}$, $T_{b,h}$, $T_{c,h}$) of the CSR-stage 101, when $i_{DC,p}$ is commutated to the faulty switch, it will charge the output capacitor of the respective transistor, thereby increasing the potential of node *p*. As a result, diode D_{p3} will conduct once the potential difference v_{pk} is larger than the standby voltage of C_p, i.e., the peak value of the phase-to-neutral voltage. A current path is now created for the DC-link current $i_{DC,p}$ from node *p* through diode D_{p3} and capacitor C_p to the star-point *k* and further towards the AC side 107 through nodes *a*, *b*, *c*. Correspondingly, the voltage of capacitor C_p increases until it is clamped by the varistor var_p, which ultimately dissipates the DC-link energy. The operation in case of an open-circuit fault of the switches of the low-side commutation cell ($T_{a,l}$, $T_{b,l}$, $T_{c,l}$) of the CSR-stage 101 is analogous considering the diode D_{n2} and capacitor C_n.

[0067] Referring to Fig. 10, current source converter 300 differs from current source converter 200 in that only one varistor var_{pn} is arranged across both cascaded capacitors C_p and C_n, instead of two separate varistors var_p and var_n across each capacitor as in converter 200. This solution further reduces the number of components. In this case, the rated voltage of the varistor becomes twice the capacitor rating. The maximum semiconductor clamping voltage is determined by the sum of the voltage of the clamping capacitor, instead of the clamping voltage of the varistor, and the voltage of the filter capacitor C_{in}. Needless to say, the varistor var_{pn} can be replaced by any other suitable voltage limiting and energy dissipating device.

[0068] Referring to Fig. 11, current source converter 400 differs from current source converter 200, 300 in that it comprises an overvoltage protection circuit 30 according to another embodiment of the present disclosure. Overvoltage protection circuit 30 does not comprise any diode bridge circuit as the overvoltage protection circuits 10, 20 described above. Instead, overvoltage protection circuit 30 comprises a first circuit 31 formed of a series connection of a clamping diode D_{p3} and a capacitor C_p connected parallel to the positive DC-rail 131 (across nodes *p* and *t*, where *t* is a node of the DC bus 104 and may be equipotential with DC terminal *P*) and a second circuit 32 formed of a series connection of clamping diode D_{n2} and capacitor C_n connected parallel to the negative DC-rail 132 (across nodes *n* and *o*, where *o* is a node of the DC bus 104 and may be equipotential with DC terminal N). Additionally, nodes *p* and *n* are connected to the star-point *k* through a respective diode D_{p1} and D_{n4} respectively which is reverse biased during normal operation of the converter 400.

[0069] By comparing Fig. 8 and Fig. 11 it can be seen that overvoltage protection circuit 30 can be obtained when in overvoltage protection circuit 20, the connection of the negative terminal of capacitor C_p to the star-point *k* is replaced with a connection to node *t* of the DC bus 104, and the connection of the positive terminal of capacitor C_n to the star-point *k* is replaced with a connection to node *o* of the DC bus 104. Hence, nodes *t* and *o* act here as capacitively stabilized voltage nodes, i.e. stabilized by the bus capacitors $C_{out,p}$ and $C_{out,n}$ in alternative to the star-point *k* that was used as capacitively stabilized voltage node in the previous embodiments. It is alternatively possible to connect the circuits 31 and 32 between *p* and *m* and between *n* and *m* respectively, hence using the middle voltage node *m* of the DC bus 104 as a capacitively stabilized voltage node. Yet other connections are possible, e.g. connecting circuit 31 between *p* and *o* (instead of between *p* and *t* as in Fig. 11) and circuit 32 between *n* and *t* (instead of between *n* and *o* as in Fig. 11). Furthermore, it will be

convenient to note that it is possible to swap the position of diode D_{p3} and capacitor C_p in circuit 31 and/or the position of diode D_{n2} and capacitor C_n in circuit 32.

[0070] In normal operation of the converter 400, the overvoltage protection circuit 30 is inactivated and all the diodes D_{p1}, D_{p3}, D_{n2} and D_{n4} are reverse-biased. The capacitors C_p and C_n are only charged during buck operation.The standby voltage of e.g. capacitor C_p is defined by: the mains phase peak voltage $\hat{V}_{pk}$ plus the injected low-frequency common mode voltage V_{mk} minus half of the minimum output voltage V_{tm}. The voltage rating of diode D_{p3} is defined by the capacitor standby voltage plus half of the maximum output voltage V_{tm} plus the injected low-frequency common mode voltage V_{mk}. In case of a fault of a switch in the high-side commutation cell of the CSR stage 101 (e.g., switch $T_{a,h}$) during rectifier operation, node *p* will be pulled negative with respect to star-point *k* due to the DC-link current discharging the output capacitor of the respective transistor as described above. As a result, diode D_{p1} will start conducting creating a current path from the star-point *k* to the DC link inductor $L_{DC,p}$. This current path is further closed as described above in relation to Fig. 2.

[0071] In case of a fault of a switch in the high-side commutation cell of the CSR stage 101 (e.g., switch $T_{a,h}$) during inverter operation, i.e. with a positive DC-link current $i_{DC,p}$ flowing from node *t* to node *p* following the convention of the arrow in Fig. 11, the output capacitor of the transistor of $T_{a,h}$ is further charged to increase the potential at node *p* positive with respect to the potential at node *t*. Diode D_{p3} will conduct once the potential difference v_{pt} between *p* and *t* is larger than the standby voltage of C_p. By so doing, a closed loop current path is created between DC-link inductor $L_{DC,p}$ and capacitor C_p enabling the energy in DC-link inductor $L_{DC,p}$ to be transferred to capacitor C_p. As with the previous embodiments, a voltage limiting and energy dissipation device is placed parallel to capacitors C_p and C_n respectively to clamp the voltage over the capacitor and eventually dissipate it.

[0072] The overvoltage protection circuit 30 is advantageously implemented in converters with a narrow output voltage range, e.g. 400 V – 600 V, to limit the required voltage rating of the diodes D_{p3}, D_{n2} and the trigger voltage.

[0073] Referring to FIG. 12, a battery charging system 700 comprises a power supply unit 704. The power supply unit 704 is coupled on one side to the AC grid through terminals A, B, C, and on the other side (at terminals P', N') to an interface 702, e.g. comprising a switch device, which allows to connect the power supply unit 704 to a battery 703. The power supply unit 704 comprises any one of the electrical converter 100-400 as described hereinabove and can comprise a further converter stage 701, which in the present system is a DC-DC converter, e.g. an LLC resonant converter. The

power supply unit 704, e.g. the third converter stage 701, can comprise a pair of coils which are inductively coupled through air (not shown), such as in the case of wireless power transfer. Alternatively, the DC-DC converter stage 701 can comprise or consist of an isolated DC-DC converter. In some cases, the interface 702 can comprise a plug and socket, e.g. in wired power transfer. Alternatively, the plug and socket can be provided at the input (e.g., at nodes A, B, C).

[0074] While the above overvoltage protection circuits have been illustrated in relation to an exemplary converter 100-400 comprising a three-phase AC-DC buck current source converter stage, a current source DC-link and a three-level boost DC/DC stage, it will be convenient to note that the overvoltage protection circuits can readily be incorporated in any other type of current source converters comprising a current source DC link. Referring to Fig. 13, a converter 800 is shown comprising two three-phase buck AC/DC converter stages in a back to back configuration, connected through a current source DC-link. Converter 800 comprises a first three-phase buck AC/DC converter stage and current source DC link identical to the CSR stage 101 and DC link 103 of Figs. 1-11. Nodes *q* and *r* of the DC link 103 are now connected to a second three-phase buck AC/DC converter stage 802 acting as a current source inverter with the AC nodes connected to e.g. an electric motor 809. Either one, preferably both the converter stages 101, 802 can comprise an overvoltage protection circuit according the present disclosure, e.g. any one of the circuits 10-30.

[0075] Aspects of the present disclosure are described in the following alphanumerically ordered clauses.

A1. A current source converter, comprising:

a first converter stage (101) comprising at least one actively operated switching device ($T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$) configured to switch electric power between at least one first-side node (a, b, c) and at least one switch node (p, n),

a DC link (103) comprising an inductive element ($L_{DC,p}$, $L_{DC,n}$) operably coupled to the at least one switch node (p, n),

an energy absorbing circuit (10, 20, 30), particularly an overvoltage protection circuit,

wherein the energy absorbing circuit (10, 20, 30) and the inductive element form a circulation circuit in which energy stored in the inductive element is configured to circulate when a current path in the first converter stage (101) is interrupted,

characterised in that the current source converter comprises at least one capacitively stabilized voltage node (k, t, o, m) and in that the energy absorbing

circuit comprises a series connection of a clamping diode (D_{p3}, D_{n2}) and an energy absorbing capacitor (C_p, C_n), wherein the series connection is connected between the at least one switch node (p, n) and the at least one capacitively stabilized voltage node (k, t, o, m).

A2. Current source converter of clause A1, comprising a DC bus (104), the DC bus comprising at least one DC bus capacitor ($C_{out,p}$, $C_{out,n}$), wherein the capacitively stabilized voltage node is a voltage node (t, m, o) of the DC bus.

A3. Current source converter of clause A2, wherein the at least one switch node comprises a first switch node (p) and a second switch node (n), wherein the DC link (103) comprises a first rail (131) connected between the first switch node (p) and a first voltage node (t) of the DC bus and a second rail (132) connected between the second switch node (n) and a second voltage node (o) of the DC bus, wherein each of the first rail and the second rail comprises an inductive element ($L_{DC,p}$, $L_{DC,n}$) and wherein the energy absorbing circuit comprises a first one (31) of the series connection (D_{p3}, C_p) connected between the first switch node (p) and a voltage node (t, m, o) of the DC bus (104) and a second one (32) of the series connection (D_{n2}, C_n) connected between the second DC node (n) and a voltage node (t, o, m) of the DC bus.

A4. Current source converter of clause A3, wherein the first series connection (31) is connected between the first switch node (p) and the first voltage node (t) of the DC bus (104), and the second series connection (32) is connected between the second switch node (n) and the second voltage node (o) of the DC bus.

A5. Current source converter of any one of the preceding clauses, comprising at least two of the first-side nodes (a, b, c), and further comprising a filter (105) comprising a plurality of filter capacitors (C_{in}) each connected between a respective one of the at least two first-side nodes (a, b, c) and a star-point (k), wherein the star-point is connected to the at least one switch node (p, n) through a diode (D_{p1}, D_{n4}) configured to be reverse biased under normal operation of the current source converter.

A6. Current source converter of clause A1, comprising at least two of the first-side nodes (a, b, c), and further comprising a filter (105) comprising a plurality of filter capacitors (C_{in}) each connected between a respective one of the at least two first-side nodes (a, b, c) and a star-point (k), wherein the capacitively stabilized voltage node is the star-point (k), wherein the at least one switch node comprises a first switch node (p) and a second switch node (n), wherein the energy absorbing circuit (10, 20) comprises a first diode bridge (11, 12, 21), wherein input nodes of the first diode bridge are connected to the first switch node (p) and the second switch node (n), wherein the clamping diode (D_{p3}, D_{n2}) is a diode of the first diode bridge (11, 12, 21) and wherein a

first terminal of the energy absorbing capacitor (C_p, C_n) is connected to a first output node of the first diode bridge.

A7. Current source converter of clause A6, wherein a second terminal of the energy absorbing capacitor (C_p, C_n) opposite the first terminal is connected to the star-point (k).

A8. Current source converter of clause A7, wherein the energy absorbing circuit (20) comprises a second energy absorbing capacitor (C_p, C_n), wherein a first terminal of the second energy absorbing capacitor is connected to a second output node of the first diode bridge (21) and a second terminal of the second energy absorbing capacitor is connected to the star-point (k).

A9. Current source converter of clause A1, comprising at least two of the first-side nodes (a, b, c), and further comprising a filter (105) comprising a plurality of filter capacitors (C_{in}) each connected between a respective one of the at least two first-side nodes (a, b, c) and a star-point (k), wherein the capacitively stabilized voltage node is the star-point (k), wherein the energy absorbing circuit (10, 20) comprises a first diode bridge (11, 12, 21), wherein input nodes of the first diode bridge are connected between one of the at least one switch node (p, n) and the star-point (k), wherein the clamping diode (D_{p3}, D_{n2}) is a diode of the first diode bridge (11, 12, 21) and wherein a first terminal of the energy absorbing capacitor (C_p, C_n) is connected to a first output node of the first diode bridge.

A10. Current source converter of clause A9, wherein the energy absorbing capacitor (C_p, C_n) is connected across output nodes of the first diode bridge (11, 12).

A11. Current source converter of clause A10, wherein the energy absorbing circuit comprises a second diode bridge (12), wherein the first input node of the first diode bridge is connected to the first switch node (p), wherein a first one of input nodes of the second diode bridge (12) is connected to the star-point (k) and a second one of the input nodes of the second diode bridge is connected to the second switch node (n), and wherein a second energy absorbing capacitor (C_n) is connected across output nodes of the second diode bridge (12).

A12. Current source converter of any one of the clauses A5 to A11, comprising a voltage limiting device (151) connected across each of the plurality of filter capacitors (C_{in}).

A13. Current source converter of any one of the preceding clauses, further comprising an energy dissipation device (15) connected across the energy absorbing capacitor.

A14. Current source converter of clause A13, wherein the energy dissipation device comprises or consists of a varistor (var_p, var_n, var_{pn}), a resistor, a thyristor-based triggered device, a transient voltage suppression diode or a combination thereof.

A15. Current source converter of any one of the preceding clauses, further comprising a detection circuit (13, 14) configured to detect activation of the energy absorbing circuit (10, 20, 30), particularly wherein the detection circuit is configured to output a fault signal (109) when an activation of the energy absorbing circuit is detected.

A16. Current source converter of any one of the preceding clauses, wherein the energy absorbing capacitor is provided as a surface mounted device.

A17. Current source converter of any one of the preceding clauses, wherein the first converter stage is an AC/DC stage comprising at least two of the first-side nodes (a, b, c), wherein the at least one switch node comprises a first switch node (p) and a second switch node (n), wherein the AC/DC stage comprises a first commutation cell between the at least two first-side nodes and the first switch node and a second commutation cell between the at least two first-side nodes and the second switch node configured to convert between an AC signal at the at least two first-side nodes (a, b, c) and a DC signal at the first and the second switch nodes, each of the first and second commutation cells comprising a plurality of actively operated switching devices ($T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$).

A18. Current source converter of any one of the preceding clauses, further comprising a second converter stage (102) coupled to the DC link.

A19. Current source converter of clause A18, wherein the second converter stage is a DC/DC converter stage or a DC/AC converter stage.

A20. Current source converter of any one of the preceding clauses, being a bidirectional converter.

A21. Current source converter according to any one of the preceding clauses, wherein the overvoltage protection circuit, particularly the clamping diode, is connected such that, under normal operation of the current source converter, the energy absorbing capacitor is configured to stay charged to a highest voltage which occurs between the at least one switch node and the capacitively stabilized voltage node.

A22. Current source converter of any one of the preceding claims, wherein the DC link connects the first converter stage to a pair of voltage nodes, wherein a first terminal of the inductive element is connected to a first one of the at least one switch node (p) and a second terminal of the inductive element is connected to one of the pair of voltage nodes (q).

A23. Battery charging system (700), comprising a power supply, the power supply comprising the current source converter of any one of the preceding clauses.

A24. Electric motor drive system (800), comprising a power supply, the power supply comprising the current source converter of any one of the clauses A1 to A22.

CLAIMS

1. A current source converter, comprising:

a first converter stage (101) comprising at least one actively operated switching device ($T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$) configured to switch electric power between at least one first-side node (a, b, c) and at least one switch node (p, n),

a DC link (103) comprising an inductive element ($L_{DC,p}$, $L_{DC,n}$) operably coupled to the at least one switch node (p, n),

an overvoltage protection circuit (10, 20, 30),

wherein the overvoltage protection circuit (10, 20, 30) and the inductive element form a circulation circuit in which energy stored in the inductive element is configured to circulate when a current path in the first converter stage (101) is interrupted,

characterised in that the current source converter comprises at least one capacitively stabilized voltage node (k, t, o, m) and in that the overvoltage protection circuit comprises a series connection of a clamping diode (D_{p3}, D_{n2}) and an energy absorbing capacitor (C_p, C_n), wherein the series connection is connected between the at least one switch node (p, n) and the at least one capacitively stabilized voltage node (k, t, o, m) such that the energy absorbing capacitor is configured to charge to a highest voltage which occurs between the at least one switch node and the capacitively stabilized voltage node and to stay charged to the highest voltage under normal operation of the current source converter.

2. Current source converter of claim 1, comprising a DC bus (104), the DC bus comprising at least one DC bus capacitor ($C_{out,p}$, $C_{out,n}$), wherein the capacitively stabilized voltage node is a voltage node (t, m, o) of the DC bus.

3. Current source converter of claim 2, wherein the at least one switch node comprises a first switch node (p) and a second switch node (n), wherein the DC link (103) comprises a first rail (131) connected between the first switch node (p) and a first voltage node (t) of the DC bus and a second rail (132) connected between the second switch node (n) and a second voltage node (o) of the DC bus, wherein each of the first rail and the second rail comprises an inductive element ($L_{DC,p}$, $L_{DC,n}$) and wherein the overvoltage protection circuit comprises a first one (31) of the series connection (D_{p3}, C_p) connected between the first switch node (p) and a voltage node (t, m, o) of the DC bus (104) and a second one (32) of the series connection (D_{n2}, C_n) connected between the second DC node (n) and a voltage node (t, o, m) of the DC bus.

4. Current source converter of claim 3, wherein the first series connection (31) is connected between the first switch node (p) and the first voltage node

(t) of the DC bus (104), and the second series connection (32) is connected between the second switch node (n) and the second voltage node (o) of the DC bus.

5. Current source converter of any one of the preceding claims, comprising at least two of the first-side nodes (a, b, c), and further comprising a filter (105) comprising a plurality of filter capacitors (C_{in}) each connected between a respective one of the at least two first-side nodes (a, b, c) and a star-point (k), wherein the star-point is connected to the at least one switch node (p, n) through a diode (D_{p1}, D_{n4}) configured to be reverse biased under normal operation of the current source converter.

6. Current source converter of claim 1, comprising at least two of the first-side nodes (a, b, c), and further comprising a filter (105) comprising a plurality of filter capacitors (C_{in}) each connected between a respective one of the at least two first-side nodes (a, b, c) and a star-point (k), wherein the capacitively stabilized voltage node is the star-point (k), wherein the at least one switch node comprises a first switch node (p) and a second switch node (n), wherein the overvoltage protection circuit (10, 20) comprises a first diode bridge (11, 12, 21), wherein input nodes of the first diode bridge are connected to the first switch node (p) and the second switch node (n), wherein the clamping diode (D_{p3}, D_{n2}) is a diode of the first diode bridge (11, 12, 21) and wherein a first terminal of the energy absorbing capacitor (C_p, C_n) is connected to a first output node of the first diode bridge.

7. Current source converter of claim 6, wherein a second terminal of the energy absorbing capacitor (C_p, C_n) opposite the first terminal is connected to the star-point (k).

8. Current source converter of claim 7, wherein the overvoltage protection circuit (20) comprises a second energy absorbing capacitor (C_p, C_n), wherein a first terminal of the second energy absorbing capacitor is connected to a second output node of the first diode bridge (21) and a second terminal of the second energy absorbing capacitor is connected to the star-point (k).

9. Current source converter of claim 1, comprising at least two of the first-side nodes (a, b, c), and further comprising a filter (105) comprising a plurality of filter capacitors (C_{in}) each connected between a respective one of the at least two first-side nodes (a, b, c) and a star-point (k), wherein the capacitively stabilized voltage node is the star-point (k), wherein the overvoltage protection circuit (10, 20) comprises a first diode bridge (11, 12, 21), wherein input nodes of the first diode bridge are connected between one of the at least one switch node (p, n) and the star-point (k), wherein the clamping diode (D_{p3}, D_{n2}) is a diode of the first diode bridge (11, 12, 21) and wherein a

first terminal of the energy absorbing capacitor (C_p, C_n) is connected to a first output node of the first diode bridge.

10. Current source converter of claim 9, wherein the energy absorbing capacitor (C_p, C_n) is connected across output nodes of the first diode bridge (11, 12).

11. Current source converter of claim 10, wherein the overvoltage protection circuit comprises a second diode bridge (12), wherein the first input node of the first diode bridge is connected to the first switch node (p), wherein a first one of input nodes of the second diode bridge (12) is connected to the star-point (k) and a second one of the input nodes of the second diode bridge is connected to the second switch node (n), and wherein a second energy absorbing capacitor (C_n) is connected across output nodes of the second diode bridge (12).

12. Current source converter of any one of the claims 5 to 11, comprising a voltage limiting device (151) connected across each of the plurality of filter capacitors (C_{in}).

13. Current source converter of any one of the preceding claims, further comprising an energy dissipation device (15) connected across the energy absorbing capacitor.

14. Current source converter of claim 13, wherein the energy dissipation device comprises or consists of a varistor (var_p, var_n, var_{pn}), a resistor, a thyristor-based triggered device, a transient voltage suppression diode or a combination thereof.

15. Current source converter of any one of the preceding claims, further comprising a detection circuit (13, 14) configured to detect activation of the overvoltage protection circuit (10, 20, 30), particularly wherein the detection circuit is configured to output a fault signal (109) when an activation of the overvoltage protection circuit is detected.

16. Current source converter of any one of the preceding claims, wherein the energy absorbing capacitor is provided as a surface mounted device.

17. Current source converter of any one of the preceding claims, wherein the first converter stage is an AC/DC stage comprising at least two of the first-side nodes (a, b, c), wherein the at least one switch node comprises a first switch node (p) and a second switch node (n), wherein the AC/DC stage comprises a first commutation cell between the at least two first-side nodes and the first switch node and a second commutation cell between the at least two first-side nodes and the second switch node configured to convert between an AC signal at the at least two first-side

nodes (a, b, c) and a DC signal at the first and the second switch nodes, each of the first and second commutation cells comprising a plurality of actively operated switching devices ($T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$).

18. Current source converter of any one of the preceding claims, further comprising a second converter stage (102) coupled to the DC link.

19. Current source converter of claim 18, wherein the DC link connects the first converter stage to the second converter stage, wherein a first terminal of the inductive element is connected to a first one of the at least one switch node (p) and a second terminal of the inductive element is connected to a node (q) of the second converter stage.

20. Current source converter of claim 18 or 19, wherein the second converter stage is a DC/DC converter stage or a DC/AC converter stage.

21. Current source converter of any one of the preceding claims, wherein the at least one actively operated switching device has bidirectional voltage blocking capability.

22. Current source converter of any one of the preceding claims, being a bidirectional converter.

23. Battery charging system (700), comprising a power supply, the power supply comprising the current source converter of any one of the preceding claims.

24. Electric motor drive system (800), comprising a power supply, the power supply comprising the current source converter of any one of the claims 1 to 22.

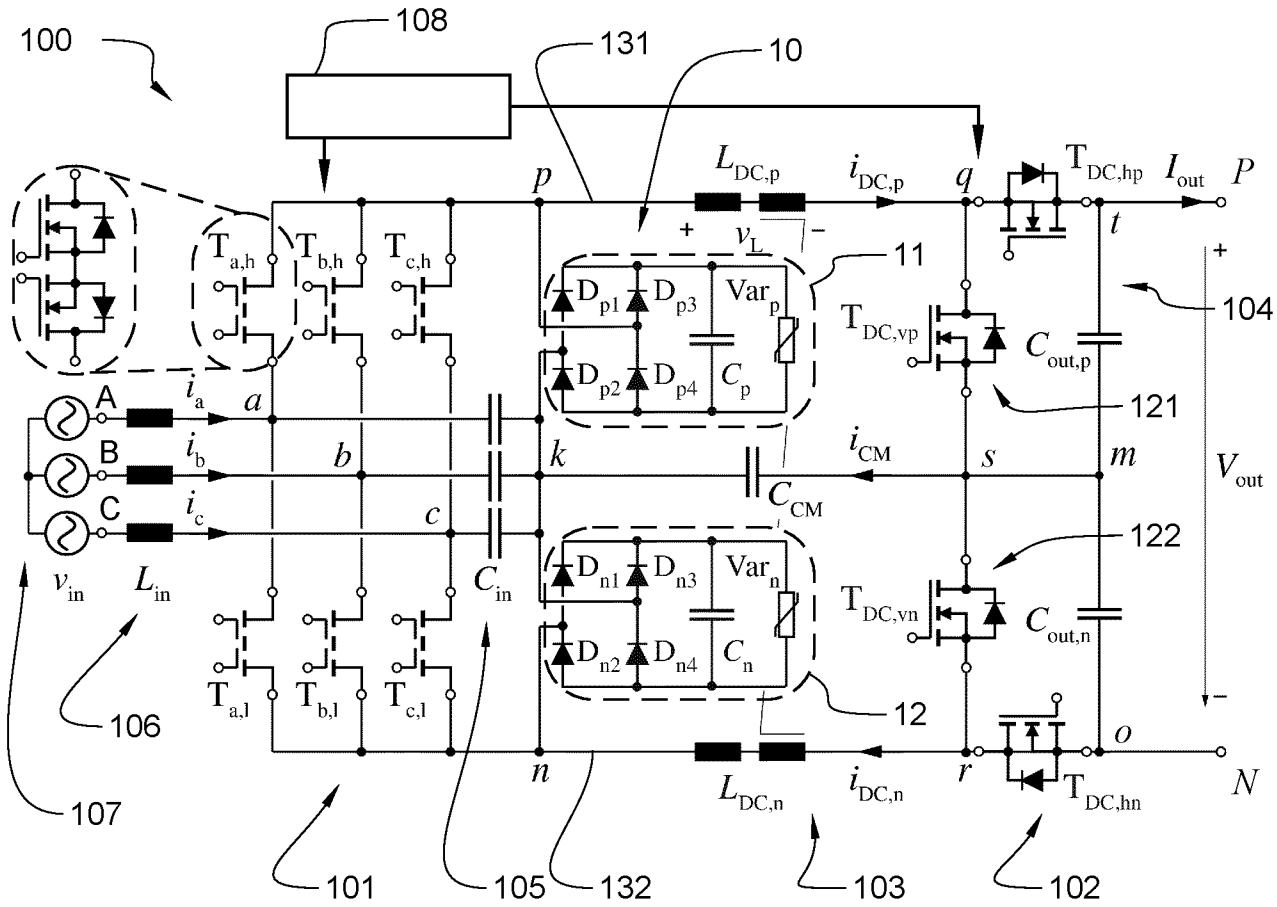

100
108
131
10
$L_{DC,p}$
$i_{DC,p}$
p
q
$T_{DC,hp}$
I_{out}
P
t
$T_{a,h}$
$T_{b,h}$
$T_{c,h}$
v_L
11
D_{p1}
D_{p3}
Var_p
D_{p2}
D_{p4}
C_p
$T_{DC,vp}$
$C_{out,p}$
104
121
A
B
C
i_a
i_b
i_c
a
b
c
k
i_{CM}
s
m
V_{out}
C_{CM}
122
v_{in}
L_{in}
C_{in}
D_{n1}
D_{n3}
Var_n
D_{n2}
D_{n4}
C_n
$T_{DC,vn}$
$C_{out,n}$
$T_{a,l}$
$T_{b,l}$
$T_{c,l}$
12
o
106
n
r
$L_{DC,n}$
$i_{DC,n}$
$T_{DC,hn}$
N
107
101
105
132
103
102

FIG 1

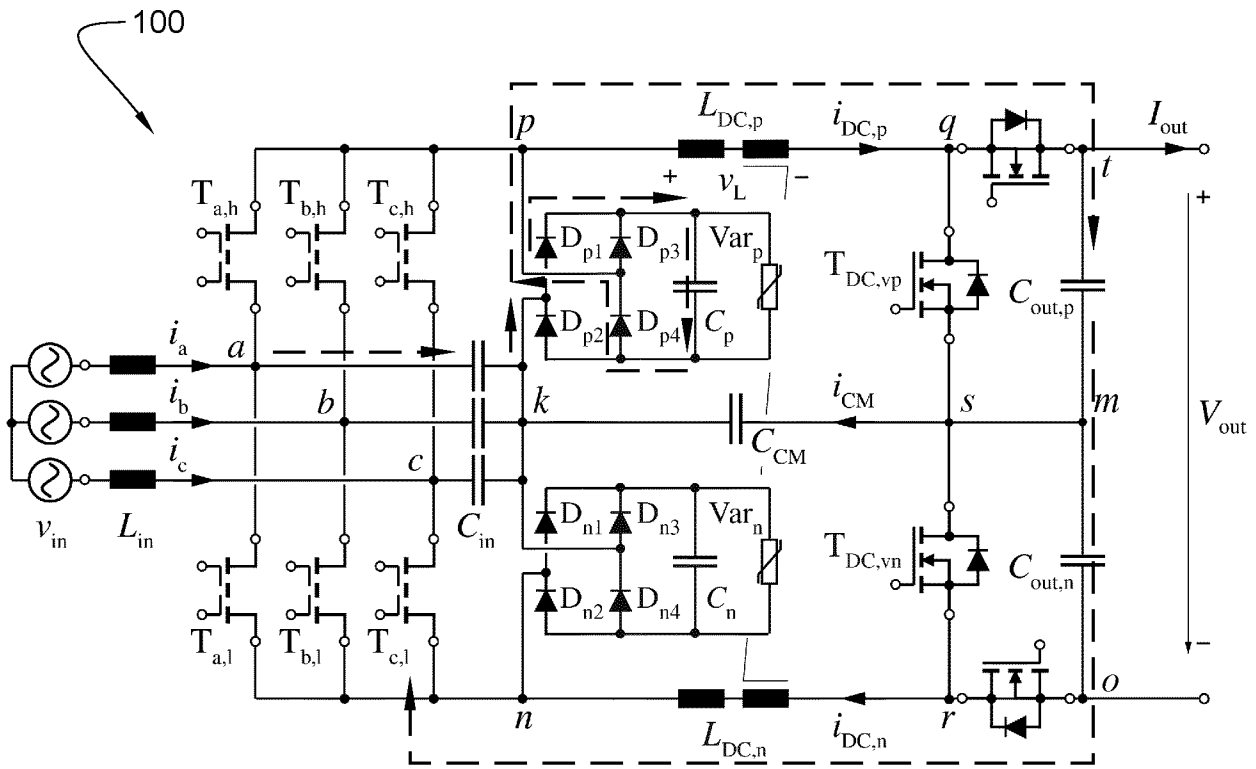

100
p
$L_{DC,p}$
$i_{DC,p}$
q
I_{out}
t
v_L
$T_{a,h}$
$T_{b,h}$
$T_{c,h}$
D_{p1}
D_{p3}
Var_p
D_{p2}
D_{p4}
C_p
$T_{DC,vp}$
$C_{out,p}$
i_a
i_b
i_c
a
b
c
k
i_{CM}
s
m
V_{out}
C_{CM}
v_{in}
L_{in}
C_{in}
D_{n1}
D_{n3}
Var_n
D_{n2}
D_{n4}
C_n
$T_{DC,vn}$
$C_{out,n}$
$T_{a,l}$
$T_{b,l}$
$T_{c,l}$
o
n
r
$L_{DC,n}$
$i_{DC,n}$

FIG 2

FIG 3

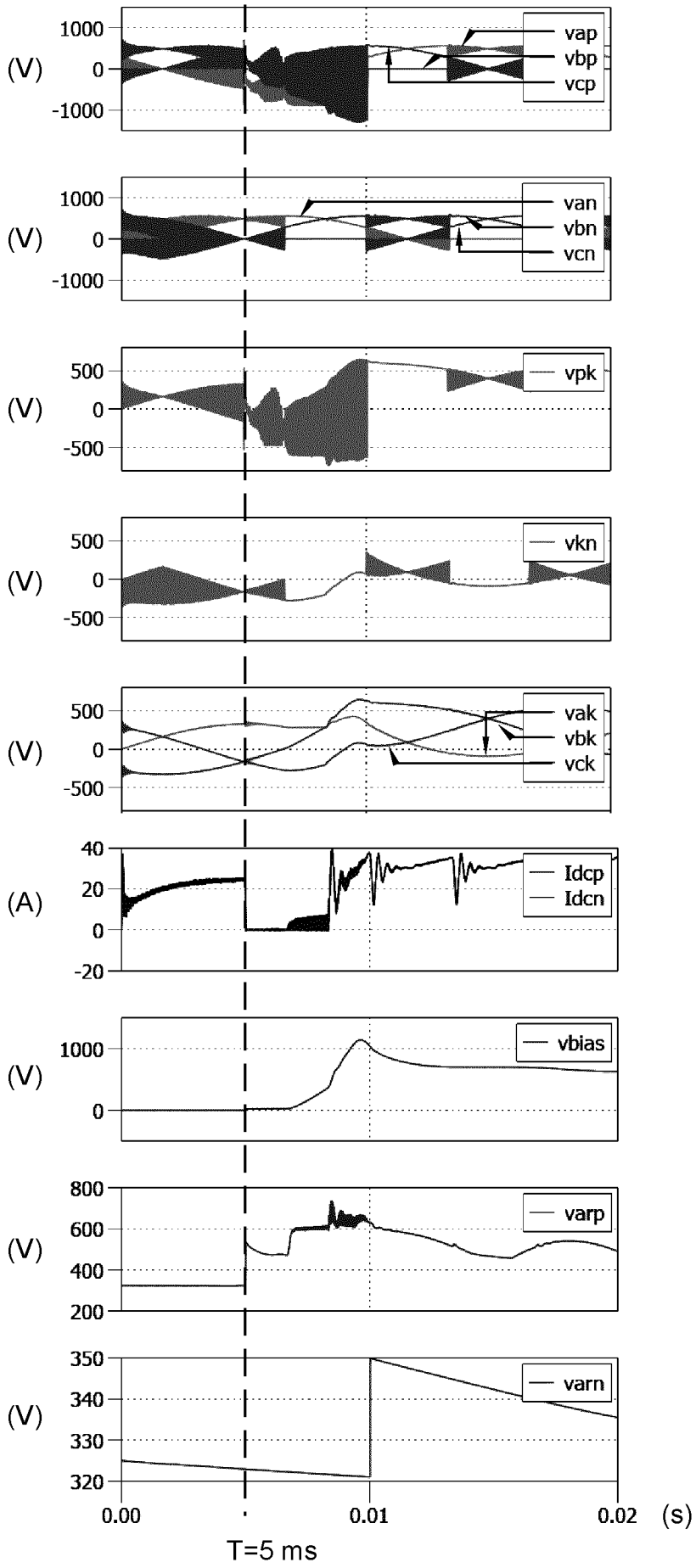

1000
0
-1000
(V)
vap
vbp
vcp
1000
0
-1000
(V)
van
vbn
vcn
500
0
-500
(V)
vpk
500
0
-500
(V)
vkn
500
0
-500
(V)
vak
vbk
vck
40
20
0
-20
(A)
Idcp
Idcn
1000
0
(V)
vbias
800
600
400
200
(V)
varp
350
340
330
320
(V)
varn
0.00
0.01
0.02
(s)
T=5 ms

FIG 4

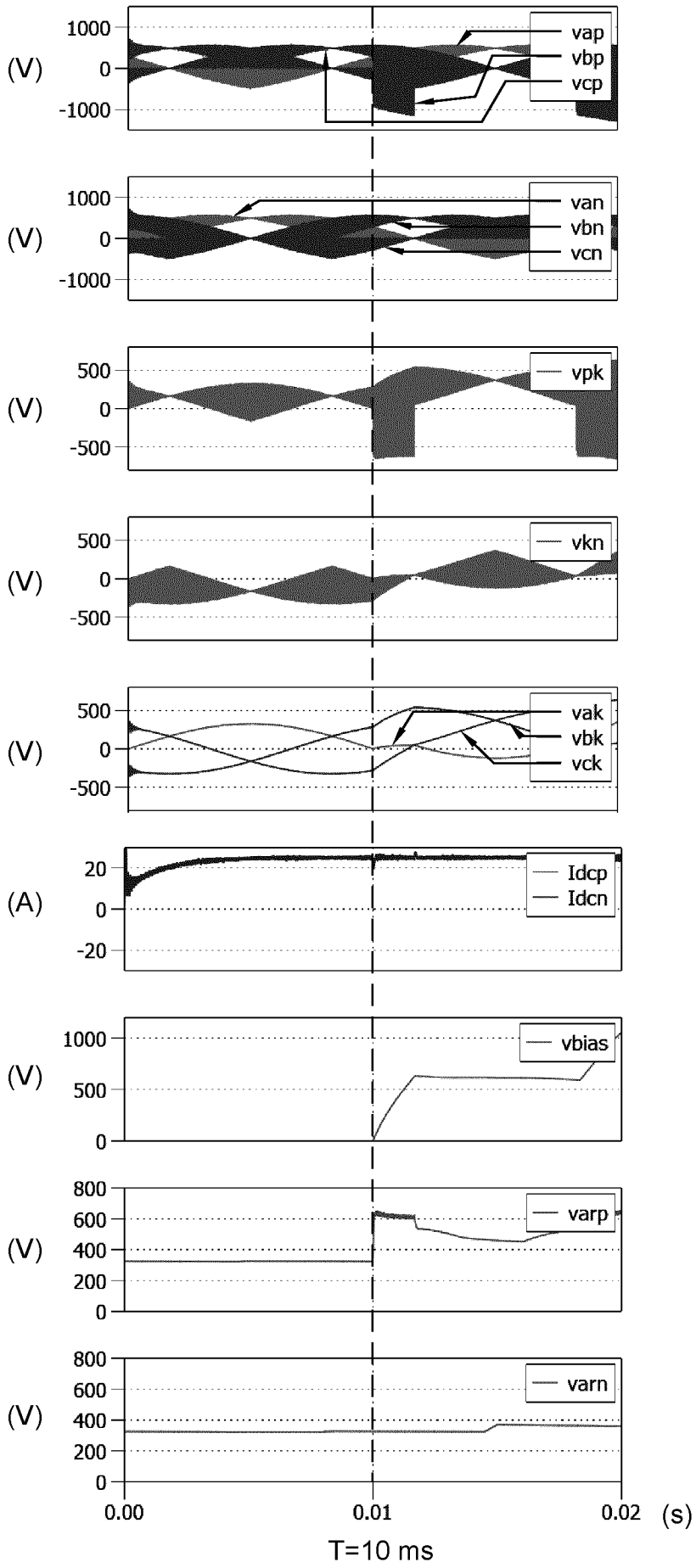
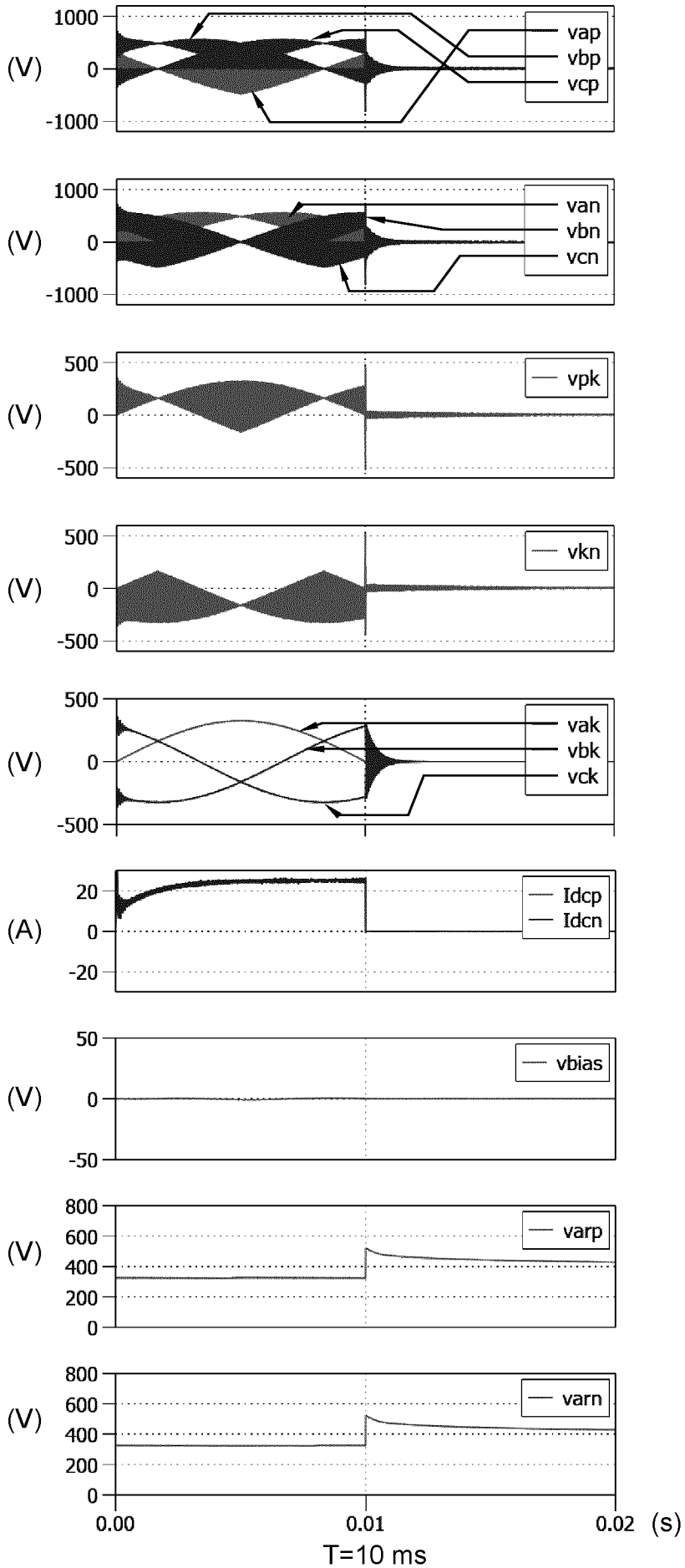

1000
0
-1000
(V)
vap
vbp
vcp
1000
0
-1000
(V)
van
vbn
vcn
500
0
-500
(V)
vpk
500
0
-500
(V)
vkn
500
0
-500
(V)
vak
vbk
vck
20
0
-20
(A)
Idcp
Idcn
1000
500
0
(V)
vbias
800
600
400
200
0
(V)
varp
800
600
400
200
0
(V)
varn
0.00
0.01
0.02
(s)
T=10 ms

FIG 5


1000
(V)
0
-1000
vap
vbp
vcp
1000
(V)
0
-1000
van
vbn
vcn
500
(V)
0
-500
vpk
500
(V)
0
-500
vkn
500
(V)
0
-500
vak
vbk
vck
20
(A)
0
-20
Idcp
Idcn
50
(V)
0
-50
vbias
800
600
(V)
400
200
0
varp
800
600
(V)
400
200
0
varn
0.00
0.01
0.02
(s)
T=10 ms

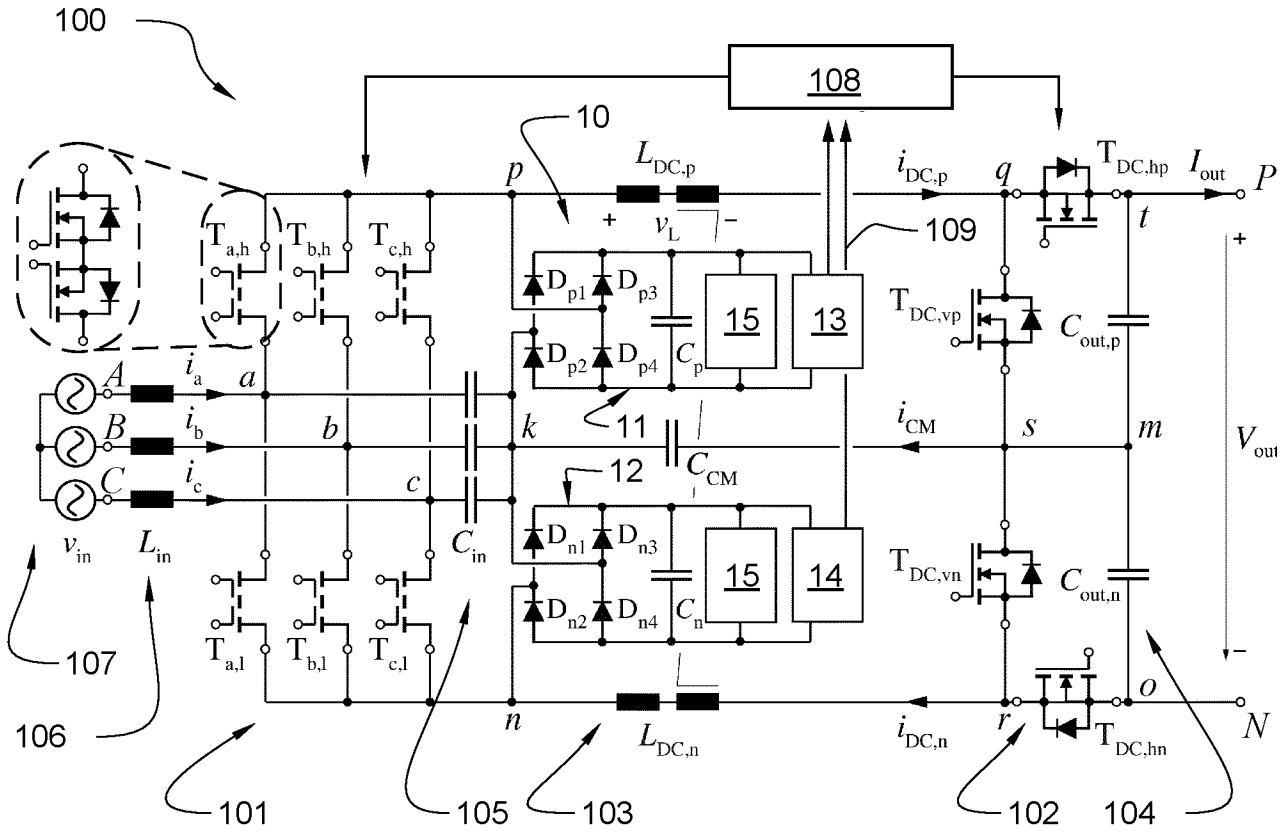

100
108
10
109
11
12
13
14
15
101
102
103
104
105
106
107
A
B
C
a
b
c
k
n
p
q
r
s
t
m
o
$T_{a,h}$ $T_{b,h}$ $T_{c,h}$
$T_{a,l}$ $T_{b,l}$ $T_{c,l}$
i_a i_b i_c
v_{in} L_{in} C_{in}
$L_{DC,p}$ $L_{DC,n}$
v_L
$i_{DC,p}$ $i_{DC,n}$
i_{CM}
D_{p1} D_{p2} D_{p3} D_{p4} C_p
D_{n1} D_{n2} D_{n3} D_{n4} C_n
C_{CM}
$T_{DC,hp}$ $T_{DC,hn}$
$T_{DC,vp}$ $T_{DC,vn}$
$C_{out,p}$ $C_{out,n}$
I_{out} V_{out}
P N

FIG 6

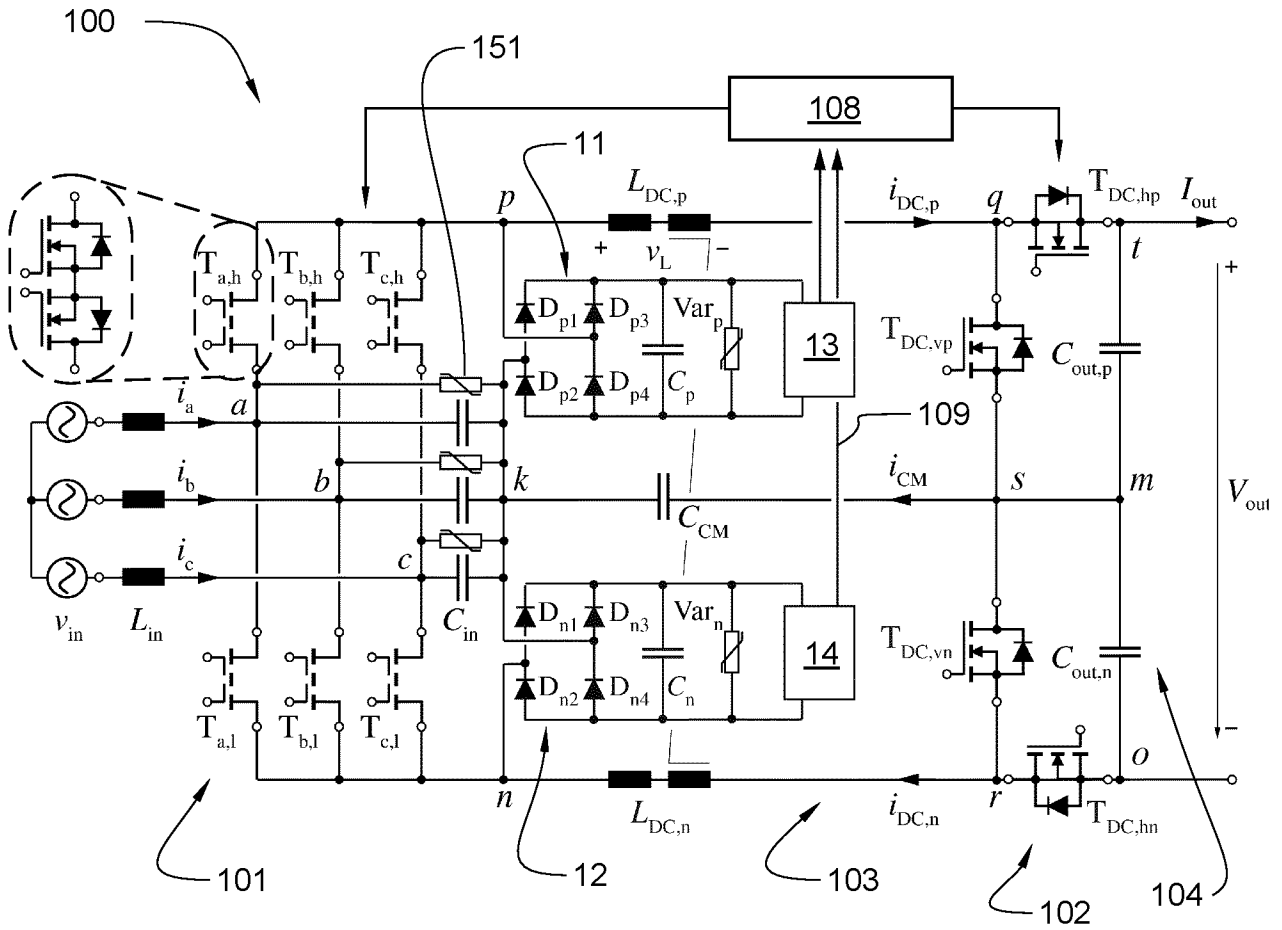

100
151
108
11
12
13
14
101
102
103
104
109
a
b
c
k
n
p
q
r
s
t
m
o
$T_{a,h}$ $T_{b,h}$ $T_{c,h}$
$T_{a,l}$ $T_{b,l}$ $T_{c,l}$
i_a i_b i_c
v_{in} L_{in} C_{in}
$L_{DC,p}$ $L_{DC,n}$
v_L
$i_{DC,p}$ $i_{DC,n}$
i_{CM}
D_{p1} D_{p2} D_{p3} D_{p4} Var_p C_p
D_{n1} D_{n2} D_{n3} D_{n4} Var_n C_n
C_{CM}
$T_{DC,hp}$ $T_{DC,hn}$
$T_{DC,vp}$ $T_{DC,vn}$
$C_{out,p}$ $C_{out,n}$
I_{out} V_{out}

FIG 7

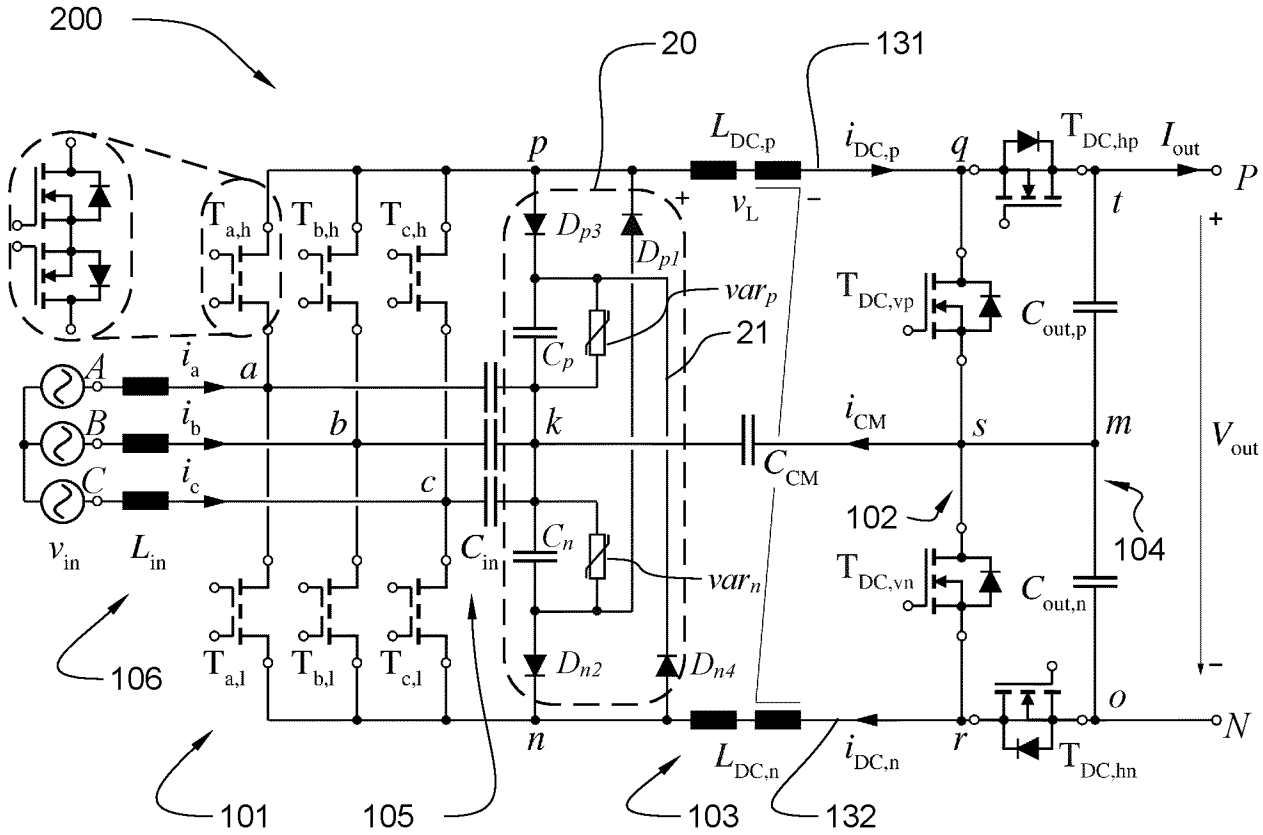

200
20
131
$L_{DC,p}$
$i_{DC,p}$
p
q
$T_{DC,hp}$
I_{out}
P
t
$T_{a,h}$
$T_{b,h}$
$T_{c,h}$
D_{p3}
D_{p1}
v_L
var_p
21
C_p
$T_{DC,vp}$
$C_{out,p}$
A
B
C
i_a
i_b
i_c
a
b
c
k
i_{CM}
s
m
V_{out}
C_{CM}
102
104
v_{in}
L_{in}
C_{in}
C_n
var_n
$T_{DC,vn}$
$C_{out,n}$
$T_{a,l}$
$T_{b,l}$
$T_{c,l}$
D_{n2}
D_{n4}
106
o
N
n
$L_{DC,n}$
$i_{DC,n}$
r
$T_{DC,hn}$
101
105
103
132

FIG 8

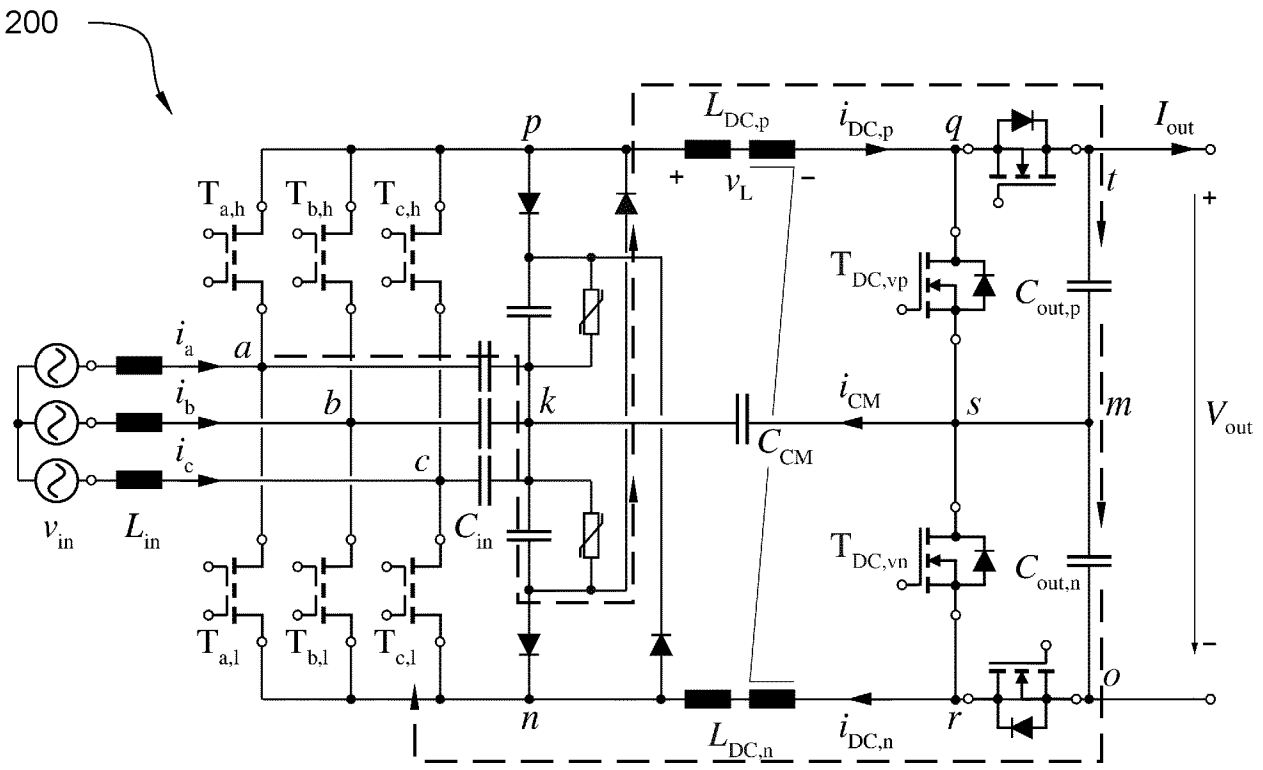

200
$L_{DC,p}$
$i_{DC,p}$
p
q
I_{out}
t
v_L
$T_{a,h}$
$T_{b,h}$
$T_{c,h}$
$T_{DC,vp}$
$C_{out,p}$
i_a
i_b
i_c
a
b
c
k
i_{CM}
s
m
V_{out}
C_{CM}
v_{in}
L_{in}
C_{in}
$T_{DC,vn}$
$C_{out,n}$
$T_{a,l}$
$T_{b,l}$
$T_{c,l}$
o
n
$L_{DC,n}$
$i_{DC,n}$
r

FIG 9

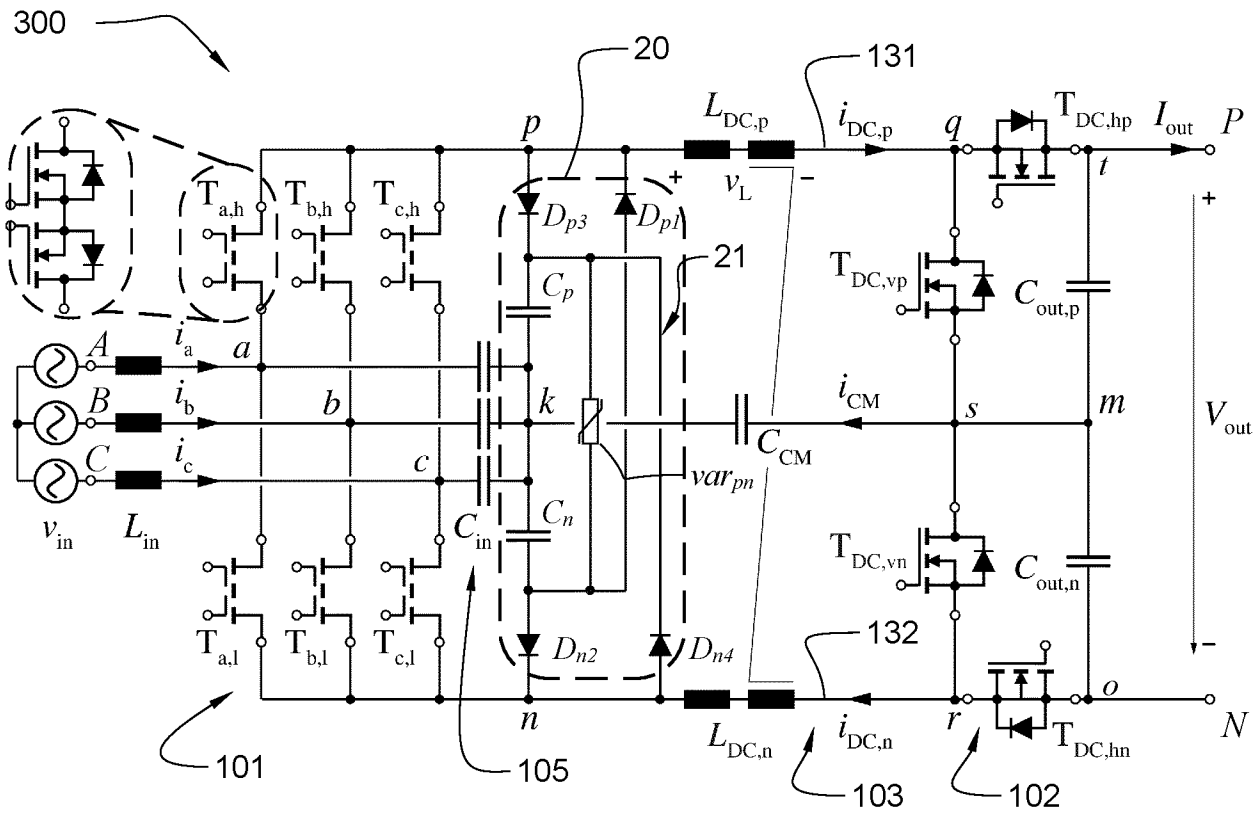

300
20
131
$L_{DC,p}$
$i_{DC,p}$
p
q
$T_{DC,hp}$
I_{out}
P
t
v_L
D_{p3}
D_{p1}
21
$T_{a,h}$
$T_{b,h}$
$T_{c,h}$
C_p
$T_{DC,vp}$
$C_{out,p}$
A
B
C
i_a
i_b
i_c
a
b
c
k
i_{CM}
s
m
V_{out}
C_{CM}
var_{pn}
v_{in}
L_{in}
C_{in}
C_n
$T_{DC,vn}$
$C_{out,n}$
$T_{a,l}$
$T_{b,l}$
$T_{c,l}$
D_{n2}
D_{n4}
132
o
n
$L_{DC,n}$
$i_{DC,n}$
r
$T_{DC,hn}$
N
101
105
103
102

FIG 10

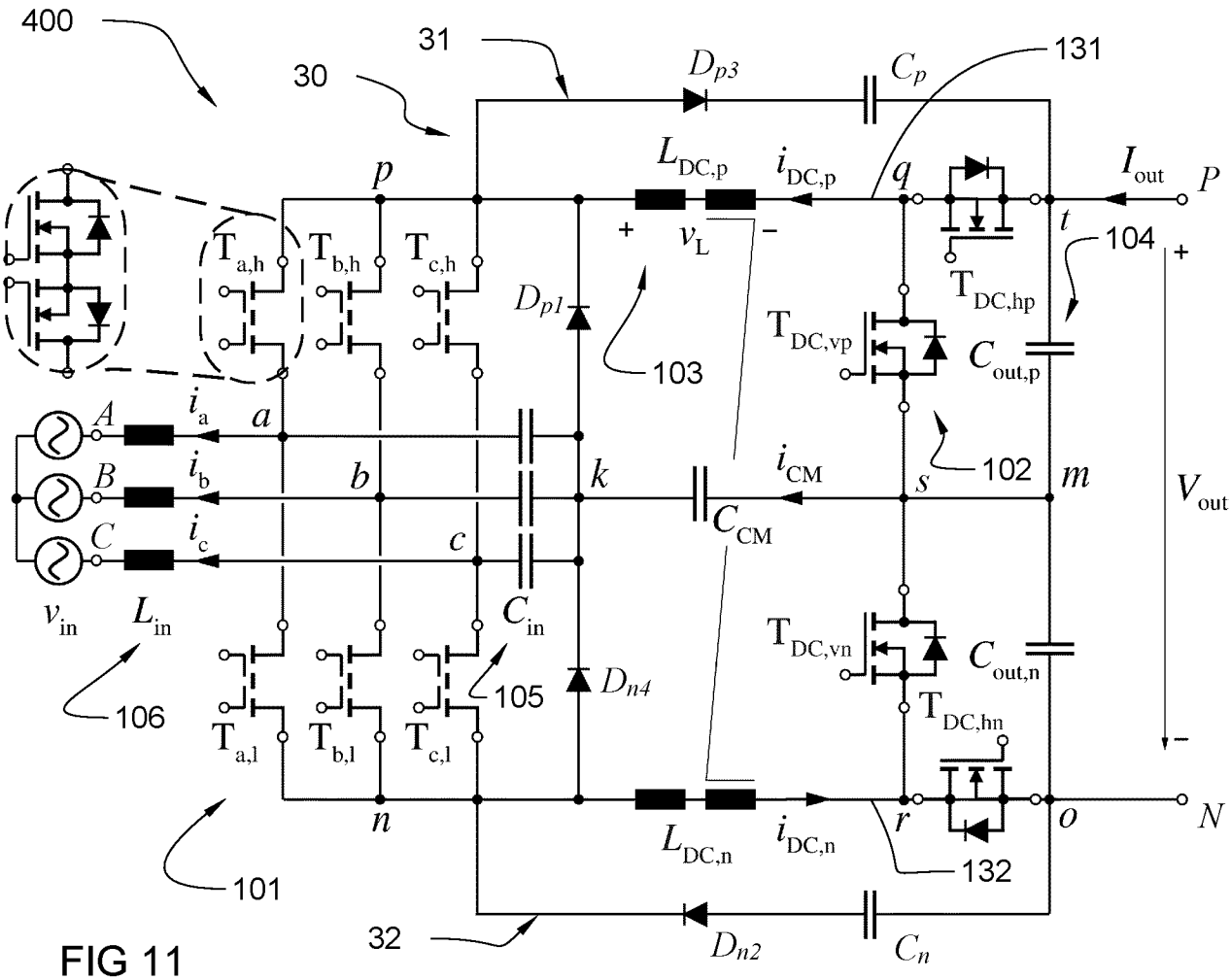

400
31
30
D_{p3}
C_p
131
$L_{DC,p}$
$i_{DC,p}$
p
q
I_{out}
P
v_L
t
104
$T_{a,h}$
$T_{b,h}$
$T_{c,h}$
D_{p1}
103
$T_{DC,hp}$
$T_{DC,vp}$
$C_{out,p}$
A
B
C
i_a
i_b
i_c
a
b
k
i_{CM}
102
s
m
V_{out}
C_{CM}
c
v_{in}
L_{in}
C_{in}
$T_{DC,vn}$
$C_{out,n}$
D_{n4}
105
$T_{DC,hn}$
$T_{a,l}$
$T_{b,l}$
$T_{c,l}$
106
n
$L_{DC,n}$
$i_{DC,n}$
r
o
N
132
101
32
D_{n2}
C_n

FIG 11

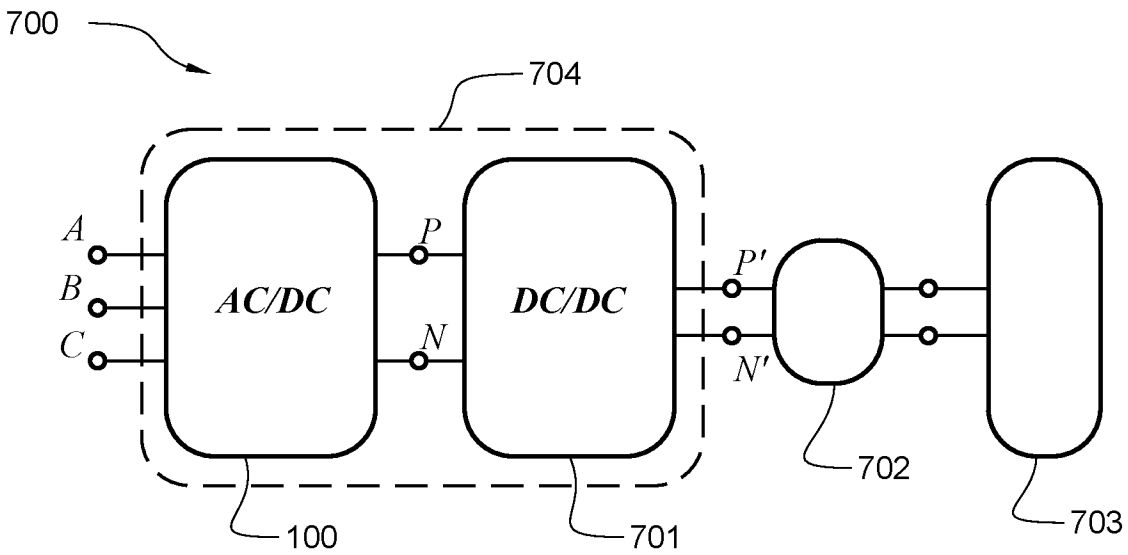

700
704
A
B
C
AC/DC
P
N
DC/DC
P'
N'
100
701
702
703

FIG 12

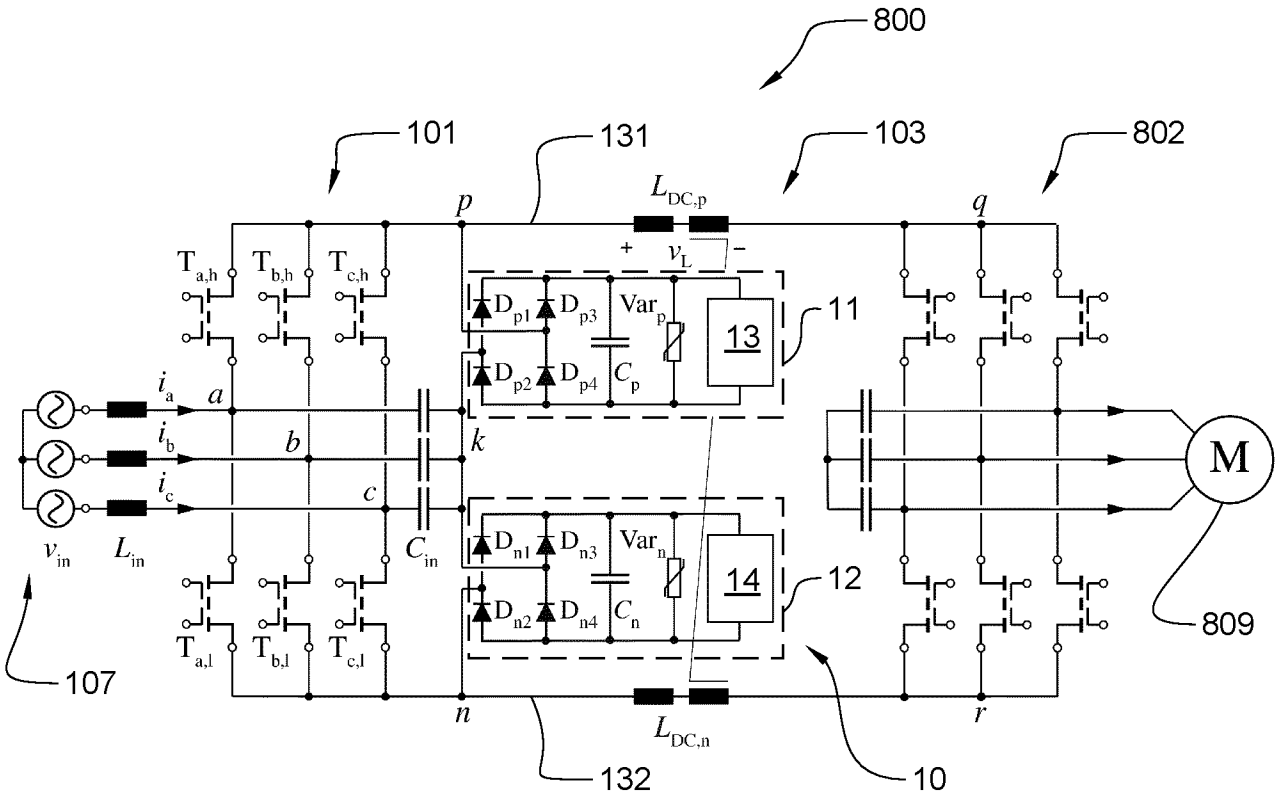

800
101
131
103
802
p
q
$L_{DC,p}$
v_L
$T_{a,h}$ $T_{b,h}$ $T_{c,h}$
D_{p1} D_{p3} Var_p
D_{p2} D_{p4} C_p
13
11
i_a i_b i_c
a
b
c
k
M
v_{in} L_{in} C_{in}
D_{n1} D_{n3} Var_n
D_{n2} D_{n4} C_n
14
12
$T_{a,l}$ $T_{b,l}$ $T_{c,l}$
809
107
n
r
$L_{DC,n}$
132
10

FIG 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2022/063549

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M1/34 H02M7/12 H02M7/797
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 636 114 A (BHAGWAT PRADEEP M [US] ET AL) 3 June 1997 (1997-06-03) figures 3, 4c column 7, line 45 - line 54	1-24
A	US 4 884 182 A (ANDO TAKEKI [JP] ET AL) 28 November 1989 (1989-11-28) cited in the application figure 1	15,17-22
Y	EP 2 662 969 A1 (ABB TECHNOLOGY AG [CH]) 13 November 2013 (2013-11-13) figures 1,2 paragraph [0024] - paragraph [0029] paragraph [0037] paragraph [0053]	1-4, 17-22,24

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[x] Further documents are listed in the continuation of Box C.

[x] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 July 2022	29/07/2022

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	van der Weiden, Ad

1

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2022/063549

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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X	EP 2 698 909 A1 (DAIKIN IND LTD [JP]) 19 February 2014 (2014-02-19)	1-24
Y	figure 20 paragraph [0121] - paragraph [0131]	1-4, 17-22,24

1

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Information on patent family members

International application No
PCT/EP2022/063549

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