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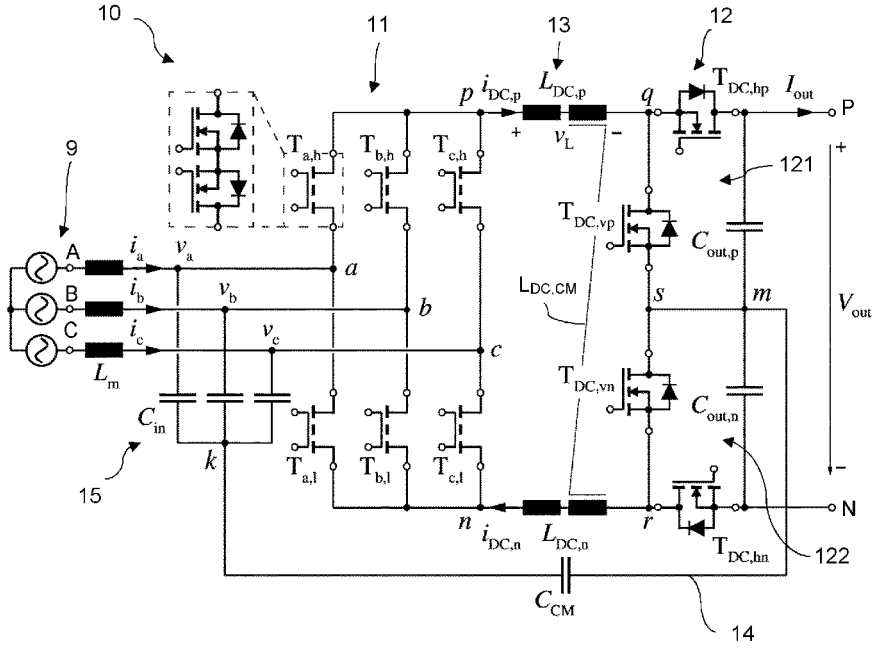

FIG 1

(57) Abstract: Electrical converter for converting between an AC signal having at least three phases and a DC signal, comprising at least three phase terminals, a first DC terminal and a second DC terminal, a first converter stage operable to convert between an AC current at the at least three phase terminals and a first DC current at the first and second intermediate nodes (p, n), a second converter stage operable to convert between a first DC signal at third and fourth intermediate nodes (q, r) and a second DC signal at the first and second DC terminals, a first filter stage comprising a capacitor network (C_{in}) having a star-point (k), a DC link connecting the first intermediate node (p) to the third intermediate node (q) and the second intermediate node (n) to the fourth intermediate node (r). The second converter stage comprises a middle voltage node (m) between the first and

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second DC terminals and a boost circuit having a midpoint node (s) at the same electrical potential as the middle voltage node (m). The DC link comprises a common mode filter, the common mode filter comprising a common mode capacitor (C_{CM}) connecting the middle voltage node (m) to the star- point (k).

Electrical power converter

Technical field

[0001] The present invention is related to electrical converters allowing to convert between a three phase AC signal and a DC signal. The electrical converter comprises an AC/DC stage and a DC/DC stage.

Background art

[0002] High power and high efficiency battery chargers, enabling fast charging of electric vehicles (EVs), are of crucial importance for a fast growth of the EV market. Moreover, in case EV batteries serve as distributed energy storage elements to support the grid operation, EV chargers must allow bidirectional power conversion. The AC/DC front-end is a main element of an EV battery charging system, and must cover a wide output voltage range to adapt to different battery voltages.

[0003] Three-phase buck-boost rectifiers are known. The buck-boost topology is simply a buck rectifier with a boost-stage added at the output end of the inductor, as illustrated in Fig. 6.5 in [3]. The two input switches rectify the AC line into a switched voltage, converted next into a DC current by the high-frequency inductor. The output switch then feeds this current into the load.

[0004] In [4], a three-phase buck-boost current source inverter is described, comprising a buck-type DC/DC converter input stage and a boost-type three-phase current DC-link inverter output stage. The current source inverter is implemented with two different modulation schemes, namely conventional pulse-width modulation and two-third pulse-width modulation (2/3-PWM). The 2/3-PWM reduces conduction and switching losses and can be applied in a subset of the buck-mode operation region. In the remainder of the buck-mode operation region, conventional PWM (3/3-PWM) and 2/3-PWM are alternated depending on the instantaneous value of the output voltage.

[0005] References:

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[3] K. D. T. Ngo, Topology and Analysis in PWM Inversion, Rectification, and Cycloconversion, Ph.D. dissertation, California Institute of Technology, May 1984.

[4] M. Guacci, D. Zhang, M. Tatic, D. Bortis, J. W. Kolar, Y. Kinoshita, H. Ishida, Three-Phase Two-Third-PWM Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs, *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 4, pp. 339-354, December 2019.

[5] M. Baumann, J. W. Kolar, A Novel Control Concept for Reliable Operation of a Three-Phase Three-Switch Buck-Type Unity-Power-Factor Rectifier With Integrated Boost Output Stage Under Heavily Unbalanced Mains Condition, *IEEE Transactions on Industrial Electronics*, vol. 52, no. 2, pp. 399-409, April 2005.

[6] Q. Lei, B. Wang, and F. Z. Peng, Unified Space Vector PWM Control for Current Source Inverter, in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Raleigh, NC, USA, 2012.

[7] D. Menzi, D. Bortis, J. W. Kolar, Three-Phase Two-Phase-Clamped Boost-Buck Unity Power Factor Rectifier Employing Novel Variable DC Link Voltage Input Current Control, *Proceedings of the 2nd IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Shenzhen, China, November 4-7, 2018.

[8] CH 698490, J. W. Kolar, Vorrichtung zur Regelung der Teilausgangsspannungen eines Dreipunkt-Hochsetzstellers.

Summary of the invention

[0006] There is a need in the art to provide a buck-boost electrical converter of the above described kind, allowing an extended converter output voltage range. There is a need in the art to provide such an electrical converter allowing improved suppression of noise at the DC-side.

[0007] According to a first aspect of the invention, there is therefore provided an electrical converter as set out in the appended claims.

[0008] An electrical converter according to the invention comprises at least three phase terminals, a first DC terminal and a second DC terminal, a first converter stage and a second converter stage, and a DC link connecting the first and second converter stages.

[0009] The first converter stage is operably coupled to the at least three phase terminals and comprises a first intermediate node and a second intermediate node, wherein the converter stage is operable to convert between an AC current at the at least three phase terminals and a first DC current at the first and second intermediate nodes. The first converter stage is advantageously implemented as a buck-type bridge converter, advantageously as a current-source converter, in particular a (bidirectional) current-source rectifier.

[0010] The second converter stage is operably coupled to the first DC terminal and the second DC terminal and comprises a third intermediate node and a fourth intermediate node. The second converter stage is operable to convert between a first DC signal, preferably a current signal, at the third and fourth intermediate nodes and a second DC signal, preferably a voltage signal, at the first and second DC terminals, wherein the second converter stage comprises a middle voltage node between the first and second DC terminals. The second converter stage is advantageously implemented as, or comprises, a boost circuit, in particular comprising a first boost circuit and a second boost circuit series stacked between the first DC terminal and the second DC terminal. The second converter stage, e.g. the boost circuit comprises a plurality of first (active) switches series connected between the third intermediate node and the fourth intermediate node. By way of example, the first boost circuit comprises at least a first one of the first switches and the second boost circuit comprises at least a second one of the first switches. Advantageously, the middle voltage node is or acts as a common node of the first and second boost circuits, e.g. the middle voltage node and the common node (midpoint) of the first and second boost circuits are coincident or connected, e.g. through a direct link, so as to be at a same electrical potential. Either one, or both the first boost circuit and the second boost circuit can be a multi-level boost circuit comprising at least three voltage nodes.

[0011] The DC link connects the first intermediate node to the third intermediate node, and the second intermediate node to the fourth intermediate node. The electrical converter further comprises a first filter stage comprising a capacitor network operably coupled to each of the three phase terminals, wherein the capacitor network comprises a star-point. The DC link comprises a common mode filter, the common mode filter comprising a common mode capacitor connecting the middle voltage node to the star-point. Advantageously, the common mode filter comprises a common mode filter choke operably coupled to the first intermediate node and the second intermediate node, the third intermediate node and the fourth intermediate node. Advantageously, the DC link comprises at least one differential mode inductor operably coupled to the first intermediate node and the third intermediate node and/or operably coupled to the second intermediate node and the fourth intermediate node.

[0012] The electrical converter topology according to the present invention combines one or more of the following advantages. First, a three-level second converter stage is employed to extend the converter output voltage range without compromising its performance, but instead reducing the occurring switching losses and/or minimizing the number of magnetic components and the size of the DC-

link inductor. Second, a novel integrated common mode (CM) filter is applied to suppress the CM noise at the DC-side.

[0013] Advantageously, the control structure is capable to seamlessly transition between conventional 3/3-PWM and 2/3-PWM [6].

[0014] As an advantage, the electrical converter according to aspects of the invention can be implemented with a control structure as discussed in this document capable to automatically select the optimal operating modes for different output voltage values. Compared to the conventional voltage source approach, the converter system introduced herein offers several advantages, i.e. a reduction of switching losses enabled by a variable DC-link current control strategy (synergetic control) and by a sinusoidally varying switched voltage.

[0015] Accordingly, in one advantageous aspect, the present disclosure provides a three-phase current DC-link split-output buck-three-level-boost AC/DC converter, formed by a three-phase buck-type current source rectifier (CSR)-stage and a subsequent boost-type DC/DC-stage. This power converter is advantageously bidirectional and can operate under non-ideal three-phase mains conditions, e.g., in case of harmonics distortion, over- or under-voltage events, voltage dips and phase voltage interruptions. Moreover, both stages are advantageously operated synergetically to provide a wide output voltage range. Electrical converters according to the invention are as well applicable in non-isolated on-board chargers protected by an on-board ground fault circuit interrupter [1]. In this case, the switches of the traction inverter and the stator coils of the motor, already present on-board of the EV, can be used as DC/DC-stage and DC-link inductor, respectively, aiming for a compact and low-cost solution [2].

[0016] Furthermore, this invention can also be applied to other areas requiring a three-phase AC/DC PFC rectifier front-end either for providing a widely adjustable DC output/load voltage from a constant three-phase mains or for providing a constant DC output voltage despite a large tolerance of the mains voltage. An example for the latter case would be datacenter power supplies, which (besides wide input voltage range) should feature continuous power supply and sinusoidal input current also in case of a mains phase loss which is possible due to the boost output stage of the proposed system. Moreover, the system could be employed for supplying a non-isolated converter stage supplying a single-side grounded load, as frequently given for envelope tracking power supplies of linear amplifiers, e.g. used for testing purposes.

[0017] Finally, it should be highlighted, that actually two individually controlled DC outputs are generated, which could be different in reference voltage

values and power delivery to the individual loads, i.e. the total power taken from the three-phase can be freely distributed to the two outputs. Accordingly, e.g. two isolated DC/DC load converters could be supplied from the two DC outputs, which would allow a design with power semiconductors of lower voltage rating and the utilization of transformers with lower turns ratio in case a low output voltage needs to be generated like for telecom applications.

[0018] According to a second aspect of the disclosure, there is provided an electric motor drive system as set out in the appended claims.

[0019] According to a third aspect of the disclosure, there is provided a battery charging system as set out in the appended claims.

[0020] According to a fourth aspect of the disclosure, there is provided a method of converting between an AC signal having at least three phases at three or more phase nodes and a DC signal at a high node and a low node. The method comprises switching by pulse width modulation between the at least three phase nodes and the high node and the low node to obtain a switched voltage signal across the high node and low node. A period of the switched voltage signal comprises a zero voltage level portion obtained by connecting the phase node having a smallest absolute instantaneous voltage value of the at least three phases of the AC signal to both the high node and the low node. The method reduces the common mode noise generated by the PWM switching without increasing switching losses or degrading a differential mode performance. Advantageously, the switched voltage signal comprises a second voltage level portion obtained by connecting the phase node having the highest instantaneous voltage value of the at least three phases of the AC signal to the high node, and connecting the phase node having the lowest instantaneous voltage value of the at least three phases of the AC signal to the low node. Advantageously, the switched voltage signal comprises a third voltage level portion obtained by connecting the phase node having the smallest absolute instantaneous voltage value to the high node, and connecting the phase node having the lowest instantaneous voltage value of the at least three phases of the AC signal to the low node, or vice versa.

[0021] According to a fifth aspect of the disclosure, there is provided a method of converting between an AC signal having at least three phases at three or more phase nodes and a DC signal at a high node and a low node. The method comprises switching by pulse width modulation between the at least three phase nodes and the high node and the low node to convert between the AC signal and the DC signal. The switching comprises switching between active states in which a connection is made between two of the at least three phases and the high node and the low node

and zero states in which the high node and the low node are short circuited, in particular in which both high and low node are both connected to only one of the at least three phases. At least one, preferably all the zero states are obtained by connecting a phase of the at least three phases of the AC signal having a smallest absolute instantaneous voltage value to the high and low nodes.

[0022] The fourth and fifth aspects described above can be provided independently of the first to third aspects, or in combination. In particular, the fourth and fifth aspects can be implemented in the electrical converter according to the first aspect.

Brief description of the figures

[0023] Aspects of the disclosure will now be described in more detail with reference to the appended drawings, wherein same reference numerals illustrate same features and wherein:

[0024] **Figure 1** represents a schematic of an exemplary embodiment of an electrical converter according to the invention implemented as a three-level (3-L) three phase (3-Φ) buck-boost (bB) current DC-link AC/DC converter system. To filter the common mode (CM) noise at the DC output port, the artificial 3-Φ neutral point k and the DC midpoint m are connected through a CM filter capacitor C_{CM}.

[0025] **Figure 2** represents Operating regions of the proposed 3-L 3-Φ bB current DC-link AC/DC converter system of Fig. 1. Depending on the required output voltage V_{out}, different operating modes, i.e. Buck-Mode, Transition-Mode, and Boost-Mode (#1 or #2), are applied in order to minimize the switching and conduction losses, and reduce the CM noise emission. Different colour intensity indicate different output power levels.

[0026] **Figure 3a-d** represent simulated waveforms of the converter of Fig. 1 operating in *Buck-Mode* with a capacitive return connection. In particular, in **Fig. 3a** the three-phase mains voltages v_a, v_b, and v_c, in **Fig. 3b** the three-phase mains currents i_a, i_b, and i_c, the DC-link currents $i_{DC,p}$ and $i_{DC,n}$ and the CM current on the return connection i_{CM}, in **Fig. 3c** the output voltage v_{out} and the output capacitor voltages $v_{cout,p}$ and $v_{cout,n}$, and in **Fig. 3d** the three-phase mains line-to-line voltages v_{ab}, v_{bc}, and v_{ca} are shown.

[0027] **Figure 4** represents differential mode (DM) voltages in *Buck-Mode* operation over one 60°-wide sector of the mains period defined by the three-phase mains currents, i.e. in this sector phase *c* has the minimum current value. In particular, v_{pn} is a switched waveform alternately assuming the values of two line-to-line voltages v_{ac} and v_{bc} during the active states, and of 0V during the zero state, and v_{qr} is equal to

V_{out}. The graphs in the upper part offer a zoomed view of typical voltage waveforms within a switching period.

[0028] **Figure 5a** represents the CM voltage of the converter of Fig. 1 operating in the *Buck-Mode* according to an aspect of the invention, with the capacitive return connection as described in the present disclosure.

[0029] **Figure 5b** represents the CM voltage of a converter as in Fig. 1 operating in *Buck-Mode* as described herein without the return connection that is contemplated in the present disclosure (the white dotted line indicates the local average value (within one pulse period) of the switched voltage waveform v_{CM}).

[0030] **Figure 6** represents common mode (CM) voltages in Buck-mode operation of the converter of Fig. 1 over one 60°-wide sector of the mains period defined by the three-phase mains currents, i.e. in this sector phase *c* has the minimum current value. specifically, the CM voltage generated by the CSR-stage $v_{CM,CSR}$ constituted of two active states common mode voltages $v_{CM,bc} = \frac{v_b+v_c}{2}$ and $v_{CM,ac} = \frac{v_a+v_c}{2}$ and one phase voltage v_a or v_b, and low-frequency components of the generated CM voltage $v_{CM,LF}$. The graphs in the upper part offer a zoomed view of typical voltage waveforms during two switching periods.

[0031] **Figure 7** represents space vector diagram of a three-phase current DC-link converter highlighting the nine states of the three-phase rectifier. The 60°-wide sector considered in **Fig. 3d** is shaded.

[0032] **Figure 8a-d** represent simulated waveforms of the converter of Fig. 1 operating in *Boost-Mode* with a capacitive return connection. In particular, in **Fig. 8a** the three-phase mains voltages v_a, v_b, and v_c, in **Fig. 8b** the three-phase mains currents i_a, i_b, and i_c, the DC-link current $i_{DC,p}$ and $i_{DC,n}$ and the CM current in the return connection i_{CM}, in **Fig. 8c** the output voltage v_{out} and the output capacitor voltages $v_{cout,p}$ and $v_{cout,n}$, and in **Fig. 8d** the three-phase mains line-to-line voltages v_{ab}, v_{bc}, and v_{ca} are shown.

[0033] **Figure 9** represents DM voltages in *Boost-Mode #1* operation over one 60°-wide sector defined by the three-phase mains currents, i.e. in this sector phase *c* has the minimum current value. In particular, v_{pn} is a switched waveform alternately assuming the values of two line-to-line voltages v_{ac} and v_{bc} during the active states, while v_{qr} switches between $\frac{V_{out}}{2}$ and V_{out}. The graphs in the upper part offer a zoomed view of typical voltage waveforms within a switching period T_{sw}.

[0034] **Figure 10a** represents the CM voltage v_{CM} of the converter of Fig. 1 operating in *Boost-Mode #1* with the return connection according to the disclosure.

[0035] **Figure 10b** represents the CM voltage v_{CM} of a converter as in Fig. 1 operating in *Boost-Mode #1* without the return connection that is contemplated in the present disclosure (the white dot line indicates the local average value of the switched voltage waveform v_{CM}).

[0036] **Figure 11** represents CM voltages in Boost mode #1 operation over a 60°-wide sector defined by the three-phase mains currents, i.e. in this sector phase *c* has the minimum current value. Specifically, CM voltage generated by the CSR-stage $v_{CM,CSR}$ constituted of the CM voltages of two active states $v_{CM,bc} = \frac{v_b+v_c}{2}$ and $v_{CM,ac} = \frac{v_a+v_c}{2}$ and low-frequency components of the generated CM voltage $v_{CM,LF}$. Furthermore, the CM voltage generated by the DC/DC-stage $v_{CM,DCDC}$ formed by $\pm\frac{1}{4}V_{out}$ and 0V is demonstrated. The graphs in the upper part offer a zoomed view of typical voltage waveforms during two switching periods.

[0037] **Figure 12** represents DM voltages in *Boost-Mode #2* operation over one 60°-wide selected sector defined by the three-phase mains currents, i.e. in this sector phase *c* has the minimum current value. In particular, v_{pn} is a switched waveform alternately assuming the values of two line-to-line voltages v_{ac} and v_{bc} during the active states, while v_{qr} switches between $\frac{V_{out}}{2}$ and V_{out}, or $\frac{V_{out}}{2}$ and 0V depending on the local average value of v_{pn}. The graphs in the upper part offer a zoomed view of typical voltage waveforms within a switching period T_{sw}.

[0038] **Figure 13a** represents the CM voltage of the converter of Fig. 1 operating in *Boost-Mode #2* with the return connection according to the disclosure.

[0039] **Figure 13b** represents the CM voltage of a converter as in Fig. 1 operating in *Boost-Mode #2* without the return connection that is contemplated in the present disclosure (the white dotted line indicates the local average value of the switched voltage waveform v_{CM}).

[0040] **Figure 14** represents CM voltages in Boost mode #2 operation over a 60°-wide selected sector defined by the three-phase mains currents, i.e. in this sector phase *c* has the minimum current value. Specifically, CM voltage generated by the CSR-stage $v_{CM,CSR}$ constituted of the CM voltages of two active states $v_{CM,bc} = \frac{v_b+v_c}{2}$ and $v_{CM,ac} = \frac{v_a+v_c}{2}$ and low-frequency components of the generated CM voltage $v_{CM,LF}$. Furthermore, the CM voltage generated by the DC/DC-stage $v_{CM,DCDC}$ formed by $\pm\frac{1}{4}V_{out}$ and 0V is demonstrated. The graphs in the upper part offer a zoomed view of typical voltage waveforms during two switching periods.

[0041] **Figure 15a-d** represent simulated waveforms of the converter of Fig. 1 operating in *Transition-Mode* with a capacitive return connection. In particular, in **Fig. 15a** the three-phase mains voltages v_a, v_b, and v_c, in **Fig. 15b** the three-phase mains currents i_a, i_b, and i_c, the DC-link current $i_{DC,p}$ and $i_{DC,n}$ and the CM current on the return connection i_{CM}, in **Fig. 15c** the output voltage v_{out} and the output capacitor voltages $v_{cout,p}$ and $v_{cout,n}$, and in **Fig. 15d** the voltage v_{mk} across the CM capacitor C_{CM} are shown.

[0042] **Figure 16** represents a synergetic control structure according to an exemplary embodiment includes three main blocks, i.e. the *Output Voltage Control*, the *DCLink Current Reference Generation* and the *Synergetic DC-Link Current Control*, enabling PFC operation with sinusoidal three-phase mains currents i_a, i_b, and i_c in phase with the sinusoidal three-phase mains voltages $v_{m,a}$, $v_{m,b}$, and $v_{m,c}$, regulation of the output voltage V_{out}, control of the DC-link current i_{DC} with synergetic operation of the three-phase buck CSR-stage and of the boost DC/DC-stage, and seamless transition between the different operating modes, i.e. *Buck-* and *Boost-mode*, and modulation schemes, i.e. 3/3-PWM and 2/3-PWM.

[0043] **Figure 17a** represents a CM/DM equivalent circuit of the electrical converter of Fig. 1, in which the CSR-stage and the DC/DC-stage are replaced by switched voltage sources.

[0044] **Figure 17b** represents a CM/DM equivalent circuit of the electrical converter of Fig. 1, in which the CSR-stage and the DC/DC-stage are replaced by equivalent CM/DM voltage sources.

[0045] **Figure 18** represents another exemplary embodiment of an electrical converter according to the invention, which differs from the converter of Fig. 1 in that the second converter stage (DC/DC stage) is implemented as a flyback capacitor circuit.

[0046] Figure 19 represents a battery charging system according to aspects of the present disclosure.

[0047] Figure 20 represents an electric motor drive system according to aspects of the present disclosure.

Description of embodiments

[0048] Referring to **Fig. 1**, an embodiment of an electrical converter 10 according to aspects of the present invention is implemented as a three-phase (3-Φ) current DC-link split-output buck-three-level-boost current AC/DC converter system, comprising a 3-Φ buck-type current source rectifier (CSR)-stage 11 and a subsequent three-level (3-L) boost-type DC/DC-stage 12. The CSR stage 11 comprises six

semiconductor switches $T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$ having bidirectional voltage blocking capability, advantageously arranged in three bridge legs, and operable to switchingly connect the AC voltage nodes a, b, c to the DC nodes p, n. Each of these semiconductor switches can be formed by anti-series connecting two discrete semiconductor switches having unidirectional voltage blocking capability, possibly with external anti-parallel diodes. Alternatively, the semiconductor switches of the CSR stage 11 can be formed as monolithic bidirectional GaN field effect transistors, in particular enhanced-mode field effect transistors (e-FET).

[0049] The DC/DC stage 12 advantageously comprises an upper boost circuit 121 and a lower boost circuit 122 stacked between the DC terminals P and N. The upper and lower boost circuits 121, 122 comprise a common node s connected to the middle voltage node m such that nodes s and m are at a same electrical potential. Each of the upper and lower boost circuits can be implemented with semiconductor switches $T_{DC,vp}$ and $T_{DC,hp}$ for the upper boost circuit 121 and semiconductor switches $T_{DC,vn}$ and $T_{DC,hn}$ for the lower boost circuit 122. Other implementations are possible. By way of example, either one or both the upper and lower boost circuits can be implemented as a flyback capacitor circuit 123, 124 as shown in Fig. 18. Fig. 18 also shows the possibility of utilizing the middle voltage node m as a third DC terminal 125.

[0050] A DC-link 13 connects the CSR stage 11 and the DC/DC stage 12. In particular, the DC-link 13 connects the DC-nodes p, n of the CSR stage 11 to the input nodes q, r of the DC/DC stage 12. The DC-link 13 is implemented with a novel common mode (CM) filtering concept, comprising a capacitive return connection 14 between the input capacitors C_{in} (star-point k) and the middle voltage node m of the output capacitors $C_{out,p}$ and $C_{out,n}$, possibly in combination with a CM DC-link inductor $L_{DC,CM}$. This common mode filtering concept allows to significantly reduce the high-frequency components of CM noise.

[0051] An input filter 15 is advantageously arranged between the AC terminals A, B, C and the AC voltage nodes a, b, c. The input filter can comprise a network of input capacitors C_{in} which are advantageously star-point-connected to star-point k. Furthermore, the split-output structure advantageously enables an asymmetrical loading capability at the DC output-port. **Figs. 17a** and **b** represent equivalent electrical circuits of the converter of Fig. 1. The DC-link 13 advantageously comprises a common mode inductor $L_{DC,CM}$ and/or a differential mode inductor $L_{DC,DM}$ which are operably coupled to nodes p and q and/or n and r.

[0052] Different possible operating modes employed in the different output voltage regions characteristic of this converter (see **Fig. 2**) are analyzed in the following with the support of simulation results.

[0053] The converter operating modes as described herein advantageously implement two different pulse-width modulation schemes for operating the switches $T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$ of the CSR stage 11, namely conventional pulse-width modulation (3/3-PWM) and two-third pulse-width modulation (2/3-PWM). The electrical converter 10 comprises a control unit configured to automatically select which of the two PWM schemes to use for operating the CSR stage 11 based on a desired or requested output voltage, as will be described in more detail below.

[0054] Referring to Fig. 7, six symmetric π/3-wide sectors of the AC input period are represented with six active states [bc], [ac], [ab], [cb], [ca] and [ba] and three freewheeling or zero states [aa], [bb] and [cc]. The letters 'a', 'b' and 'c' in the above refer to the voltage nodes a, b, c of Fig. 1. E.g., the state [bc] refers to a state in which node b is connected to node p by closing switch $T_{b,h}$ and in which node c is connected to node n by closing switch $T_{c,l}$. Hence, in the active states, the AC input 9 is connected between the DC-link nodes p, n, whereas in the zero states, the nodes p and n are short circuited. Consequently, depending on the selected state, the DC-link input voltage v_{pn} varies between 0V (zero states) and the six input voltages $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ac}$.

[0055] In 3/3-PWM, the six semiconductor switches $T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$ of the CSR stage 11 are operated in order to switch between the two respective active states and the zero state. In the example of the shaded sector of Fig. 2, the switches of the CSR stage 11 are operated to switch between states [bc], [ac] and the zero state. Conventionally, the zero state [cc] is used for this sector. However, in one aspect of the invention, as will be described below in relation to buck-mode operation, the zero state used in this sector is [bb] from $\frac{\pi}{6}$ to $\frac{\pi}{3}$ and [aa] from $\frac{\pi}{3}$ to $\frac{\pi}{2}$, instead of [cc] over the whole sector. This allows to further reduce the common mode noise generated by the CSR stage.

[0056] In 2/3-PWM, a pulse-width modulation scheme is employed that is free of zero states in all sectors, i.e. all zero space vectors are eliminated and only the active states are applied. For the shaded sector of Fig. 2, this results in that only active states [bc] and [ac] are applied, without applying the zero state, e.g. [cc]. Consequently, $T_{c,h}$ is permanently off and only $T_{a,h}$ and $T_{b,h}$ are alternately switched. In this case, $T_{c,l}$ is permanently on and $T_{a,l}$ and $T_{b,l}$ are permanently off. The 2/3-PWM scheme allows to improve efficiency by eliminating switching losses resulting from

transitioning to/from the zero state and possibly conduction losses in the DC-link due to reduced RMS value of the DC-link current. Further details regarding 2/3-PWM scheme can be found in reference [6], section III.B and IV and in [4].

(i) *Buck-Mode* Operation ($V_{out} < \frac{3}{2}\hat{V}_{in}$)

[0057] In buck-mode operation, the most significant waveforms of the CSR-stage and of the DC/DC-stage are reported in **Fig. 3a-d**. In this mode, only the CSR-stage operates to step down the three-phase mains voltages to a DC output voltage lower than $\frac{3}{2}\hat{V}_{in}$ (where $\hat{V}_{in}$ refers to the peak amplitude of the AC input voltage). The two switches $T_{DC,hp}$ and $T_{DC,hn}$ of the DC/DC-stage are permanently on to avoid any switching losses, as shown in **Fig. 4**, where $v_{qr} = V_{out}$.

[0058] The differential mode (DM) output voltage of the CSR-stage v_{pn} is a switched waveform alternately assuming the values of two line-to-line voltages during the active states, and of 0V during the zero state, as shown in **Fig. 4**.

[0059] In **Fig. 5a-b**, $v_{CM,CSR}$ coincides with the CM voltage v_{CM} generated by the converter without the return connection 14, i.e. with an open circuit between *m* and *k*, due to permanently clamping of the DC/DC stage. With a capacitive return connection, i.e. a CM capacitor C_{CM} connected between *m* and *k*, C_{CM}, together with the CM DC-link inductor L_{DC}, forms a CM filter. Accordingly, the low-frequency (LF), i.e. 150Hz, component of v_{CM} appears across C_{CM} (see **Fig. 5a**), while the high-frequency (HF) component, i.e. at the switching frequency, appears across $L_{DC,p}$ and $L_{DC,n}$.

[0060] In buck-mode operation, a 3/3-PWM scheme is advantageously applied. To reduce the CM noise generated by the CSR-stage 11 without increasing switching losses or degrading the DM performance, e.g. the DC-link current ripple, the zero state is advantageously implemented by connecting the AC input voltage node a, b, c having the smallest absolute instantaneous voltage value to the nodes p, n of the DC-link 13. In **Fig. 6**, the sector where phase *c* has the minimum current value is considered as an example (this sector is shaded in Fig. 7). The zero state used in this sector is [bb] from $\frac{\pi}{6}$ to $\frac{\pi}{3}$ and [aa] from $\frac{\pi}{3}$ to $\frac{\pi}{2}$, instead of [cc] as in the PWM schemes described in literature (see **Fig. 7**).

[0061] The aforementioned PWM modulation scheme advantageously allows to have a continuous LF component of v_{CM} at the boundary between different sectors, in turn allowing implementation of the capacitive return connection 14. Thus, advantageously, in each sector, the LF component of v_{CM} should, for example, start from 0V and end at 0V. Otherwise, a current ringing will occur on the return path and also in the DC-link.

(ii) *Boost-Mode* Operation ($V_{out} > \sqrt{3}\hat{V}_{in}$)

[0062] To achieve the boost functionality, both CSR-stage 11 and DC/DC-stage 11 are operated simultaneously. The CSR-stage 11 always operates at the maximum modulation index (equal to one) to minimize the DC-link current i_{DC} and the conduction losses of the whole converter 10. In boost-mode operation, a 2/3-PWM scheme is advantageously applied to the switches of the CSR stage 11. The DC-link current i_{DC} is controlled to a pulsed shape as shown in **Fig. 8b**. Depending on the local average value (averaged within one pulse period) of v_{pn}, the input voltage of the DC/DC-stage v_{qr} is a switched waveform alternately assuming the values of $\frac{V_{out}}{2}$ and V_{out} (*Boost-Mode #1*, see **Fig. 9**), or 0V and $\frac{V_{out}}{2}$ (*Boost-Mode #2*, see **Fig. 12**).

[0063] Furthermore, the converter CM voltage v_{CM} (for *Boost-Mode #1* see **Fig. 10b**, and for *Boost-Mode #2* see **Fig. 13b**) is generated by both the CSR-stage 11 and the DC/DC-stage 12, due to the operation of both stages in *Boost-Mode*.

[0064] Last but not least, the upper and lower output capacitors $C_{out,p}$ and $C_{out,n}$ are alternatively utilized when $\frac{V_{out}}{2}$ is required at the input 12 of the DC/DC-stage to balance the output mid-point *m*. As a result, the main frequency component of $v_{CM,DCDC}$ is at half of the switching frequency, while the one of $V_{CM,CSR}$ is at the three times of the mains frequency.

(ii.1) *Boost-Mode* #1 ($3\hat{V}_{in} > V_{out} > \sqrt{3}\hat{V}_{in}$)

[0065] A three-level (3-L) DC/DC-stage 12 is advantageously considered allowing to extend the output voltage range and reduce the switching losses in the DC/DC-stage (as compared to a two-level arrangement). Due to a comparably low output voltage in the *Boost-Mode #1*, the input voltage of the DC/DC-stage v_{qr} is a switched waveform alternately assuming the values of $\frac{V_{out}}{2}$ and V_{out} (*Boost-Mode #1*, see **Fig. 9**).

[0066] The CM voltage generated by the CSR-stage $v_{CM,CSR}$ is a switched waveform alternately assuming the values of two CM voltages during the active states, as shown in **Fig. 11**. Advantageously, the LF component of $v_{CM,CSR}$ is identical to the LF component of v_{CM}, which also satisfies the aforementioned requirement for the proposed CM filtering method. The DC/DC-stage only produces HF CM components, i.e. 0V if v_{qr} = 0V or V_{out}, $\frac{V_{out}}{4}$ if $T_{DC,hp}$ and $T_{DC,vn}$ are on, and $-\frac{V_{out}}{4}$ if $T_{DC,hn}$ and $T_{DC,vp}$ are on.

[0067] Considering the impact on CM and DM voltage-time area, the same carrier is advantageously used to generate the PWM signals of the CSR-stage

11 and of the DC/DC-stage 12, and the switching states featuring the larger values of two switched voltage waveforms v_{pn} and v_{qr} are centered in one switching period to ensure minimum CM and DM voltage-time area over the DC-link CM and DM inductors $L_{DC,p}$ and $L_{DC,n}$, as shown in **Fig. 9**.

(ii.2) *Boost-Mode #2* ($V_{out} > 3\hat{V}_{in}$)

[0068] Due to the increased V_{out}, the input voltage of the DC/DC-stage v_{qr} is a switched waveform alternately assuming the values of 0V and $\frac{V_{out}}{2}$ (*Boost-Mode #2*, see **Fig. 12**). When $V_{out} > 3\hat{V}_{in}$, V_{out} is large enough to balance the DM voltage-time area of the CSR-stage by only using 0V and $\frac{V_{out}}{2}$, so *Boost-Mode #2* is applied.

[0069] The CM voltage generated by the CSR-stage $v_{CM,CSR}$ is a switched waveform alternately assuming the values of two CM voltages of the active states, as shown in **Fig. 14**. Advantageously, the LF component of $v_{CM,CSR}$ is identical to the LF component of v_{CM}, which also allows to satisfy the aforementioned requirement for the selected CM filtering method. The DC/DC-stage only produces HF components, i.e. 0V if v_{qr} = 0V or V_{out}, $\frac{V_{out}}{4}$ if $T_{DC,hp}$ and $T_{DC,vn}$ are on, and $-\frac{V_{out}}{4}$ if $T_{DC,hn}$ and $T_{DC,vp}$ are on.

(iii) *Transition-Mode* Operation ($\frac{3}{2}\hat{V}_{in} < V_{out} < \sqrt{3}\hat{V}_{in}$)

[0070] In *Transition-Mode*, 3/3-PWM and 2/3-PWM are alternately applied based on the local average value of v_{pn}, $\bar{v}_{pn}$. If $\bar{v}_{pn} > V_{out}$, 3/3-PWM is used, and if $\bar{v}_{pn} < V_{out}$, 2/3-PWM is used, as shown in **Fig. 15**.

[0071] The DM and CM voltage analysis follows the behaviour described for 2/3-PWM and 3/3-PWM independently.

Control unit with synergetic control structure

[0072] **Fig. 16** shows a block diagram of control unit 20 implementing a synergetic control structure according to an aspect of the present invention. The control unit 20 advantageously comprises three main functional blocks 21, 22 and 23. Control unit 20 can be configured to receive as input a reference output voltage. Outputs of the control unit 20 are gate signals to the switches of the CSR stage 11, representative of a selected PWM scheme and gate signals to the switches of the DC/DC stage 12, which are particularly representative of a duty cycle which the control unit 20 has determined for these switches (in boost mode operation). On the other hand, in buck-mode operation, control unit 20 is configured to maintain DC/DC stage 12 inoperative as described above.

[0073] The first block 21 is formed by an *Output Voltage Controller*, and is configured to define the input power reference P^*, e.g. through a PI-controller, considering the error between the actual and the reference output voltage, V_{out} and V_{out}^*, respectively. Hence, by measuring the peak value of the three-phase mains voltages $\hat{V}_{in,meas}$ (constant over one mains period even for unbalanced mains conditions), the converter's input conductance reference G^* is calculated as:

$$G^* = \frac{P^*}{\frac{3}{2}\hat{V}_{in,meas}^2} \qquad (1)$$

and fed into the following block 22 responsible for the *DC-Link Current Reference Generation*.

[0074] In order to achieve PFC operation, the three-phase mains current references i_a^*, i_b^*, and i_c^* are set proportional to the corresponding three-phase mains voltages $v_{m,a}^*$, $v_{m,b}^*$, and $v_{m,c}^*$, and are limited to I_{max} to ensure the safe operation of the selected power semiconductors and to avoid the saturation of the DC-link inductor L_{DC}. The instantaneous values of these currents advantageously provide the sector information for the space vector pulse width modulator 24 of the CSR-stage 11, while the upper envelope of their absolute values $i_{DC,2/3}^*$, obtained by

$$i_{DC,2/3}^* = max\{|i_a^*|, |i_b^*|, |i_c^*|\}, \quad (2)$$

is the varying DC-link current reference for 2/3-PWM operation. Differently, multiplying G^* with the calculated peak value of the three-phase mains voltages $\hat{V}_{in,c}$ (different from $\hat{V}_{in,meas}$ only in case of unbalanced mains conditions), defined by:

$$\hat{V}_{in,c} = \sqrt{\frac{3}{2}(v_a^2 + v_b^2 + v_c^2)}, \qquad (3)$$

provides the peak value of the three-phase mains current references $\hat{I}_{in}^*$. $\hat{V}_{in,c}$ is constant and equal to $\hat{V}_{in,meas}$ only for symmetric mains conditions. If the mains is unbalanced, $\hat{V}_{in,c}$ shows a time-dependent behaviour within one switching period. The varying $\hat{V}_{in,c}$ ensures a sinusoidal shape of $I_{DC,3/3}^*$ during one-phase operation.

[0075] The DC-link current reference for 3/3-PWM operation $I_{DC,3/3}^*$, can be determined by the reference output power P^* and measured phase voltages v_a, v_b, v_c. This ensures the operation under unbalanced mains condition. Dividing $\hat{I}_{in}^*$ by the current conversion ratio of the AC/DC-stage $m_{AC/DC}^*$ and of the DC/DC-stage $m_{DC/DC}^*$, the DC-link current reference for 3/3-PWM operation $I_{DC,3/3}^*$, is calculated. $m_{AC/DC}^*$ and $m_{DC/DC}^*$ are derived from the reference output voltage V_{out}^* to operate with the minimum DC-link current i_{DC}. It will be convenient to note that the current

conversion ratio of the AC/DC-stage can alternatively be stated as $m^*_{AC/DC} = \frac{\hat{\imath}^*_{in}}{\hat{\imath}^*_{DC}}$ and of the DC/DC-stage as $m^*_{DC/DC} = \frac{\hat{\imath}^*_{DC}}{I_{out}}$. Therefore, as an advantage and as shown in **Fig. 16**, the present method advantageously allows to determine $I^*_{DC,3/3}$ without requiring to measure the output current I_{out}. In buck mode operation, the DC-link current reference for 3/3-PWM operation $I^*_{DC,3/3}$ corresponds to I_{out}.

[0076] Advantageously, the DC-link current reference i^*_{DC} takes the maximum value between $i^*_{DC,2/3}$, and $I^*_{DC,3/3}$,

$$i^*_{DC} = max\{i^*_{DC,2/3}, I^*_{DC,3/3}\}, \quad (4)$$

providing the input for the third block 23, controlling the DC-link current, and referred to as the *Synergetic DC-Link Current Control*. In particular, in one embodiment, automatic selection of the operating mode can be based on the value of i^*_{DC}, and hence based on comparison between $i^*_{DC,2/3}$ and $I^*_{DC,3/3}$.

[0077] If $i^*_{DC,2/3}$ is larger than I_{out}, hence larger than $I^*_{DC,3/3}$, the converter 10 operates in *Boost-mode*, with 2/3-PWM operation of the CSR stage 11. If smaller, the DC/DC-stage 12 does not operate, the switches $T_{DC,hp}$ and $T_{DC,hn}$ are permanently on, and the CSR-stage 11 operates with 3/3-PWM in *Buck-mode*, resulting in identical currents flowing through the DC-link inductor and at the DC output.

[0078] Advantageously, the method for determining i^*_{DC} shown in (4), ensures a seamless transition from 3/3-PWM to 2/3-PWM and vice versa. It furthermore advantageously ensures minimum conduction losses in *Transition-mode*.

[0079] In the *Synergetic DC-Link Current Control* block 23, i^*_{DC} is first compared with $i_{DC} = \frac{1}{2}(i_{DC,p} + i_{DC,n})$; their difference, e.g. by means of the DC-link current PI-controller, provides the voltage v^*_L to be generated across L_{DC} by switching the CSR-stage 11 and possibly the DC/DC-stage 12. The sum of v^*_L and the output voltage reference V^*_{out} results in the virtual DC-link voltage reference V^*_{DC}. Feeding V^*_{DC} into two voltage limiters, the virtual DC-link voltage references for 3/3-PWM $v^*_{DC,3/3}$ and for 2/3-PWM $v^*_{DC,2/3}$ are calculated. This is the core of the synergetic operation; in fact, when the three-phase mains voltages are large enough to generate the necessary V^*_{DC} without operating the DC/DC-stage, i.e. $V^*_{out} < V_{max}$, this stage is permanently clamped to eliminate its switching losses, while the CSR-stage provides the required voltage gain (*Buck-mode*), but must operate with 3/3-PWM. In this case, $v^*_{DC,3/3} = v^*_{DC} = v^*_{pn}$, i.e. the reference output voltage of the CSR-stage, and $v^*_{DC,2/3} = V^*_{out}$. Differently, when V^*_{out} is large enough to balance the volt-second area applied to L_{DC} by the CSR-stage

with $m_{AC/DC}$ = 1, i.e. $V_{out}^{*} > \frac{2}{\sqrt{3}} V_{max}$, the CSR-stage operates with 2/3-PWM and the DC/DC-stage is actively switched with PWM (*Boost-mode*). Specifically, $v_{DC,3/3}^{*} = V_{max}$, and $v_{DC,2/3}^{*} = v_{qr}^{*}$, i.e. the reference input voltage of the DC/DC-stage. Finally, when $V_{max} < V_{out}^{*} < \frac{2}{\sqrt{3}} V_{max}$, the current controller democratically switches between 2/3-PWM and 3/3-PWM, depending on the instantaneous v_{L}^{*} (*Transition-mode*).

[0080] Accordingly, the current control block 23 advantageously regulates the DC-link current i_{DC} always by means of only one stage, i.e. when operating with 3/3-PWM, the CSR-stage 11 is controlled by modifying $v_{DC,3/3}^{*}$ and $v_{DC,2/3}^{*}$ is not influenced thanks to the voltage limiter; when operating with 2/3-PWM, instead, the DC/DC-stage 11 is controlled by modifying $v_{DC,2/3}^{*}$ and $v_{DC,3/3}^{*}$ is clamped to V_{max}.

[0081] To ultimately operate the two stages, $v_{DC,3/3}^{*}$ and $v_{DC,2/3}^{*}$ are fed to the modulators 24, 25. For the CSR-stage, the reference DC-link current $i_{DC,CSR}^{*}$ utilized in the modulator 24 is determined based on $v_{DC,3/3}^{*}$ and on $m_{DC/DC}$. $i_{DC,CSR}^{*}$ and i_{DC}^{*} are identical in steady state. Specifically, in 3/3-PWM operation, V_{out}^{*} coincides with $v_{qn}^{*} = v_{DC,3/3}^{*}$ and $m_{DC/DC}^{*}$=1 because $T_{DC,hp}$ and $T_{DC,hn}$ are permanently on. Differently, in 2/3-PWM operation, $m_{DC/DC}^{*}$ must be considered due to the operation of the DC/DC stage. Given

$$\frac{V_{out}^{*}}{m_{DC/DC}^{*} \cdot V_{max}} = 1$$

the CSR-stage operates with the maximum modulation index, and i_{DC}^{*} is regulated by the DC/DC-stage only. The switching signals for the CSR-stage 11 can be calculated from i_{a}^{*}, i_{b}^{*}, i_{c}^{*}, and $i_{DC,CSR}^{*}$ as described in reference [4] and appropriately distributed to the twelve gate terminals.

[0082] An example is given in the following considering the sector where phase *c* has the minimum current value (see **Fig. 7**). The zero state used in this sector is [bb] from $\frac{\pi}{6}$ to $\frac{\pi}{3}$ and [aa] from $\frac{\pi}{3}$ to $\frac{\pi}{2}$, instead of [cc] as in the PWM schemes described in the prior art. The duty cycles of the two active states and of the zero state are calculated as:

$$\delta_{[ac]} = \frac{i_{a}^{*}}{i_{DC}^{*}}, \delta_{[bc]} = \frac{i_{b}^{*}}{i_{DC}^{*}}, and\ \delta_{[0]} = 1 - \delta_{[ac]} - \delta_{[bc]},$$

where $\delta_{[xy]}$ indicates the duty cycle of the state [xy].

[0083] Finally, the duty-cycle reference of the DC/DC-stage 12 is calculated by:

$$d^{*} = \frac{v_{DC,2/3}^{*}}{V_{out}^{*}} = \frac{v_{qn}^{*}}{V_{out}^{*}}$$

and then compared with a three-level triangular carrier to generate complementary switching signals.

[0084] Referring to FIG. 19, a battery charging system 700 comprises a power supply unit 704. The power supply unit 704 is coupled on one side to the AC grid through terminals A, B, C, and on the other side (at terminals P', N') to an interface 702, e.g. comprising a switch device, which allows to connect the power supply unit 704 to a battery 703. The power supply unit 704 comprises any one of the electrical converter 10 as described hereinabove with first and second converter stages and further can comprise a third converter stage 701, which in the present system is a DC-DC converter, e.g. an LLC resonant converter. The power supply unit 704, e.g. the third converter stage 701, can comprise a pair of coils which are inductively coupled through air (not shown), such as in the case of wireless power transfer. Alternatively, the DC-DC converter stage 701 can comprise or consist of an isolated DC-DC converter. In some cases, the interface 702 can comprise a plug and socket, e.g. in wired power transfer. Alternatively, the plug and socket can be provided at the input (e.g., at nodes A, B, C).

[0085] Referring to Fig. 20, an electric motor drive system 30 can incorporate the electrical converter as described herein. In an advantageous embodiment, the stator coils 33 of an electric motor (not shown) are connected to act as a common mode filter choke and/or as a differential mode inductor of the DC link 13. Additionally, or alternatively, the second converter stage 12 can be configured to operate as a traction inverter of the electric motor. The traction inverter can be formed by the half bridge 320 between nodes q and r. Switches 321, 322, 323, 324 can be semiconductor switches, e.g. just as switches $T_{DC,vp}$, $T_{DC,hp}$, $T_{DC,vn}$ and $T_{DC,hn}$ respectively of Fig. 1.

[0086] Aspects of the present disclosure are set out in the following numbered clauses.

1. Electrical converter for converting between an AC signal having at least three phases and a DC signal, comprising:

at least three phase terminals, a first DC terminal and a second DC terminal,

a first converter stage operably coupled to the at least three phase terminals and comprising a first intermediate node (p) and a second intermediate node (n), wherein the converter stage is operable to convert between an AC current at the at least three phase terminals and a first DC current at the first and second intermediate nodes (p, n),

a second converter stage operably coupled to the first DC terminal and the second DC terminal and comprising a third intermediate node (q) and a fourth intermediate node (r), wherein the second converter stage is operable to convert between a first DC signal at the third and fourth intermediate nodes (q, r) and a second DC signal at the first and second DC terminals, wherein the second converter stage comprises a middle voltage node (m) between the first and second DC terminals,

a first filter stage comprising a capacitor network (C_{in}) operably coupled to each of the three phase terminals, wherein the capacitor network comprises a star-point (k),

a DC link connecting the first intermediate node (p) to the third intermediate node (q) and the second intermediate node (n) to the fourth intermediate node (r),

wherein the DC link comprises a common mode filter, the common mode filter comprising a common mode capacitor (C_{CM}) connecting the middle voltage node (m) to the star-point (k).

2. Electrical converter of clause 1, wherein the common mode filter comprises a common mode filter choke operably coupled to the first intermediate node (p) and the second intermediate node (n), the third intermediate node (q) and the fourth intermediate node (r).

3. Electrical converter of clause 1 or 2, wherein the DC link comprises at least one differential mode inductor operably coupled to the first intermediate node (p) and the third intermediate node (q) and/or operably coupled to the second intermediate node (n) and the fourth intermediate node (r).

4. Electrical converter of clauses 2 and 3, wherein the common mode filter choke and the differential mode inductor comprise a common core or individual cores.

5. Electrical converter of any one of the preceding clauses, wherein the first DC signal is the first DC current.

6. Electrical converter of any one of the preceding clauses, wherein the second DC signal is a DC voltage across the first and second DC terminals.

7. Electrical converter of any one of the preceding clauses, wherein the first filter stage comprises inductors (L_m) coupled between the three phase terminals and the capacitor network (C_{in}).

8. Electrical converter of any one of the preceding clauses, wherein the second converter stage comprises a capacitor filter ($C_{out,p}$, $C_{out,n}$)

comprising a plurality of series connected capacitors across the first and second DC terminals, wherein the middle voltage node (m) is a middle node of the capacitor filter.

9. Electrical converter of any one of the preceding clauses, wherein the second converter stage comprises a boost circuit.

10. Electrical converter of clause 9, wherein the second converter stage comprises a plurality of series connected first switches ($T_{DC,vp}$, $T_{DC,vn}$) connected between the third intermediate node (q) and the fourth intermediate node (r), wherein a midpoint of the series connected first switches is connected to the middle voltage node (m).

11. Electrical converter of clause 9 or 10, wherein the boost circuit comprises a first boost circuit ($T_{DC,hp}$, $T_{DC,vp}$) and a second boost circuit ($T_{DC,hn}$, $T_{DC,vn}$) stacked between the first DC terminal and the second DC terminal, wherein the middle voltage node (m) is a common node of the first and second boost circuits.

12. Electrical converter of clause 11, wherein the first boost circuit and/or the second boost circuit is a multi-level boost circuit.

13. Electrical converter of any one of the preceding clauses, comprising a third DC terminal connected to the middle voltage node (m).

14. Electrical converter of any one of the preceding clauses, comprising a control unit, wherein the first converter stage and the second converter stage comprise active switching devices operably coupled to the control unit, wherein the control unit is implemented with a plurality of operating modes for operating the electrical converter.

15. Electrical converter of clause 14, wherein a first operating mode of the plurality of operating modes corresponds to a buck mode of operation, wherein the second converter stage is configured to operate to continuously connect the third and fourth intermediate nodes (q, r) to the first and second DC terminals respectively, and wherein the control unit is configured to actively operate the active switching devices ($T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$) of the first converter stage.

16. Electrical converter of clause 14 or 15, wherein a second operating mode of the plurality of operating modes corresponds to a boost mode of operation, wherein the control unit is configured to actively operate the active switching devices ($T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$, $T_{DC,hp}$, $T_{DC,vp}$, $T_{DC,hn}$, $T_{DC,vn}$) of both the first converter stage and the second converter stage.

17. Electrical converter of any one of the clauses 14 to 16, wherein the control unit is operable to operate the electrical converter in rectifier mode, wherein in rectifier mode, the control unit is operable to determine a first current

reference ($i^*_{DC,2/3}$) for a current in the DC link and a second current reference ($I^*_{DC,3/3}$) for the current in the DC link, wherein the control unit is operable to automatically select between the plurality of operating modes based on comparison of the first current reference and the second current reference.

18. Electrical converter of clause 17, wherein the first current reference is determined based on a reference output power and reference input phase currents.

19. Electrical converter of clause 17 or 18, wherein the second current reference is determined based on a reference output power and measured phase voltages.

20. Electrical converter of any one of the clauses 14 to 19, wherein the control unit is configured to operate the active switching devices through pulse width modulation.

21. Electrical converter of any one of the clauses 14 to 20, wherein the control unit is configured to operate the first converter stage and the second converter stage so as to obtain a voltage across the common mode capacitor (C_{CM}) being one of: a substantially constant zero voltage signal, a substantially triangular waveform and a substantially sinusoidal waveform, preferably comprising one or more harmonic frequencies of a fundamental frequency of the AC signal, preferably comprising a third harmonic frequency of the fundamental frequency.

22. Electrical converter of any one of the preceding clauses, wherein the control unit is operable to inject a common mode voltage signal to the third and fourth intermediate nodes (q, r) so as to control a voltage across the common mode capacitor (C_{CM}).

23. Electrical converter of clause 22, comprising measurement means for measuring a voltage signal at the middle voltage node (m) and at nodes (a, b, c) of the at least three phases, wherein the controller is operable to determine the common mode voltage signal injected to the third and fourth intermediate nodes (q, r) based on the measured voltage signals.

24. Electrical converter of clause 22 or 23, wherein the control unit is operable to add an offset to duty cycles of pulse width modulation signals controlling operation of active switches ($T_{DC,vp}$, $T_{DC,vn}$) of the second converter stage, thereby obtaining the common mode voltage signal injected to the third and fourth intermediate nodes (q, r).

25. Electric motor drive system, comprising the electrical converter of any one of the preceding clauses.

26. Electric motor drive system according to clause 25, further comprising an electric motor comprising stator coils, wherein the stator coils are connected to act as a common mode filter choke and/or as a differential mode inductor of the DC link of the electrical converter.

27. Electric motor drive system according to clause 25 or 26, comprising a traction inverter operable to drive the electric motor, wherein the traction inverter is configured to operate as the second converter stage when operating the electrical converter.

28. Battery charging system, in particular for charging electric vehicle drive batteries, wherein the battery charging system comprises a power supply, the power supply comprising the electrical converter of any one of the clauses 1 to 24.

29. Method of converting between an AC signal having at least three phases at at least three phase nodes (a, b, c) and a DC signal at a high node (p) and a low node (n), comprising switching by pulse width modulation between the at least three phase nodes (a, b, c) and the high node (p) and the low node (n) to obtain a switched voltage signal across the high node and low node, wherein a period of the switched voltage signal comprises a zero voltage level portion obtained by connecting the phase node having a smallest absolute instantaneous voltage value of the at least three phases of the AC signal to both the high node (p) and the low node (n).

30. Method of clause 29, wherein the switched voltage signal comprises a second voltage level portion obtained by connecting the phase node having the highest instantaneous voltage value of the at least three phases of the AC signal to the high node (p), and connecting the phase node having the lowest instantaneous voltage value of the at least three phases of the AC signal to the low node (n).

31. Method of clause 29 or 30, wherein the switched voltage signal comprises a third voltage level portion obtained by connecting the phase node having the smallest absolute instantaneous voltage value to the high node, and connecting the phase node having the lowest instantaneous voltage value of the at least three phases of the AC signal to the low node.

32. Method of any one of the clauses 29 to 31, applied to the electrical converter of any one of the clauses 1 to 24.

33. Electrical converter of any one of the clauses 1 to 24, comprising a control unit configured for operating the first converter stage according to the method of any one of the clauses 29 to 31.

CLAIMS

1. Electrical converter (10) for converting between an AC signal having at least three phases and a DC signal, comprising:

at least three phase terminals (A, B, C), a first DC terminal (P) and a second DC terminal (N),

a first converter stage (11) operably coupled to the at least three phase terminals and comprising a first intermediate node (p) and a second intermediate node (n), wherein the first converter stage (11) is operable to convert between an AC current at the at least three phase terminals and a first DC current ($i_{DC,p}$, $i_{DC,n}$) at the first and second intermediate nodes (p, n),

a second converter stage (12) operably coupled to the first DC terminal (P) and the second DC terminal (N) and comprising a third intermediate node (q), a fourth intermediate node (r) and a middle voltage node (m) between the first and second DC terminals, wherein the second converter stage is operable to convert between a first DC signal at the third and fourth intermediate nodes (q, r) and a second DC signal at the first and second DC terminals, wherein the second converter stage comprises a boost circuit (121, 122, 123, 124) comprising a plurality of first switches ($T_{DC,vp}$, $T_{DC,vn}$) series connected between the third intermediate node (q) and the fourth intermediate node (r), wherein a midpoint (s) of the series connected first switches is connected to the middle voltage node (m) so as to be at a same electrical potential as the middle voltage node,

a first filter stage (15) comprising a capacitor network (C_{in}) operably coupled to each of the three phase terminals, wherein the capacitor network comprises a star-point (k),

a DC link (13) connecting the first intermediate node (p) to the third intermediate node (q) and the second intermediate node (n) to the fourth intermediate node (r),

wherein the DC link comprises a common mode filter, the common mode filter comprising a common mode capacitor (C_{CM}) connecting the middle voltage node (m) to the star-point (k).

2. Electrical converter of claim 1, wherein the common mode filter comprises a common mode filter choke ($L_{DC,CM}$) operably coupled to the first intermediate node (p) and the second intermediate node (n), the third intermediate node (q) and the fourth intermediate node (r).

3. Electrical converter of claim 1 or 2, wherein the DC link comprises at least one differential mode inductor ($L_{DC,DM}$) operably coupled to the first

intermediate node (p) and the third intermediate node (q) and/or operably coupled to the second intermediate node (n) and the fourth intermediate node (r).

4. Electrical converter of claims 2 and 3, wherein the common mode filter choke ($L_{DC,CM}$) and the differential mode inductor ($L_{DC,DM}$) comprise a common core or individual cores.

5. Electrical converter of any one of the preceding claims, wherein the first DC signal is the first DC current ($i_{DC,p}$, $i_{DC,n}$).

6. Electrical converter of any one of the preceding claims, wherein the second DC signal is a DC voltage (V_{out}) across the first and second DC terminals.

7. Electrical converter of any one of the preceding claims, wherein the first filter stage (15) comprises inductors (L_m) coupled between the three phase terminals (A, B, C) and the capacitor network (C_{in}).

8. Electrical converter of any one of the preceding claims, wherein the second converter stage (12) comprises a capacitor filter ($C_{out,p}$, $C_{out,n}$) comprising a plurality of series connected capacitors across the first and second DC terminals, wherein the middle voltage node (m) is a middle node of the capacitor filter.

9. Electrical converter of any one of the preceding claims, wherein the boost circuit comprises a first boost circuit (121, 123) and a second boost circuit (122, 124) stacked between the first DC terminal (P) and the second DC terminal (N), wherein the middle voltage node (m) is a common node of the first and second boost circuits.

10. Electrical converter of claim 9, wherein the first boost circuit and/or the second boost circuit is a multi-level boost circuit.

11. Electrical converter of any one of the preceding claims, comprising a third DC terminal (125) connected to the middle voltage node (m).

12. Electrical converter of any one of the preceding claims, comprising a control unit (20), wherein the first converter stage (11) and the second converter stage (12) comprise active switching devices operably coupled to the control unit, wherein the control unit is implemented with a plurality of operating modes for operating the electrical converter.

13. Electrical converter of claim 12, wherein a first operating mode of the plurality of operating modes corresponds to a buck-mode of operation, wherein the second converter stage is configured to operate to continuously connect the third and fourth intermediate nodes (q, r) to the first and second DC terminals respectively, and wherein the control unit (20) is configured to operate the active

switching devices ($T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$) of the first converter stage (11) through pulse width modulation.

14. Electrical converter of claim 13, wherein in the first operating mode, the control unit is configured to operate the active switching devices of the first converter stage (11) according to a pulse-width modulation scheme switching between active states in which two phases of the at least three phases are connected to the first and second intermediate nodes (p, n) and zero states in which the first and second intermediate nodes (p, n) are short-circuited, wherein the control unit is configured to implement the zero states by connecting a phase of the at least three phases of the AC signal having a smallest absolute instantaneous voltage value to the first and second intermediate nodes (p, n).

15. Electrical converter of any one of the claims 12 to 14, wherein a second operating mode of the plurality of operating modes corresponds to a boost mode of operation, wherein the control unit (20) is configured to operate the active switching devices ($T_{a,h}$, $T_{a,l}$, $T_{b,h}$, $T_{b,l}$, $T_{c,h}$, $T_{c,l}$, $T_{DC,hp}$, $T_{DC,vp}$, $T_{DC,hn}$, $T_{DC,vn}$) of both the first converter stage (11) and the second converter stage (12) through pulse width modulation.

16. Electrical converter of claim 15, wherein in the second operating mode, the control unit (20) is configured to operate the active switching devices of the first converter stage (11) according to a pulse-width modulation scheme being free of zero states in which the first and the second intermediate nodes are short circuited by the active switches of the first converter stage.

17. Electrical converter of any one of the claims 12 to 16, wherein the control unit (20) is operable to operate the electrical converter in rectifier mode, wherein in rectifier mode, the control unit is operable to determine a first current reference ($i^*_{DC,2/3}$) for a current in the DC link and a second current reference ($I^*_{DC,3/3}$) for the current in the DC link, wherein the control unit is operable to automatically select between the plurality of operating modes based on comparison of the first current reference and the second current reference.

18. Electrical converter of claim 17, wherein the first current reference is determined based on a reference output power and reference input phase currents.

19. Electrical converter of claim 17 or 18, wherein the second current reference is determined based on a reference output power and measured phase voltages.

20. Electrical converter of any one of the claims 12 to 19, wherein the control unit (20) is configured to operate the first converter stage (11) and the second converter stage (12) so as to obtain a voltage across the common mode capacitor (C_{CM}) being one of: a substantially constant zero voltage signal, a substantially triangular waveform and a substantially sinusoidal waveform, preferably comprising one or more harmonic frequencies of a fundamental frequency of the AC signal, preferably comprising a third harmonic frequency of the fundamental frequency.

21. Electrical converter of any one of the claims 12 to 20, wherein the control unit (20) is operable to inject a common mode voltage signal to the third and fourth intermediate nodes (q, r) so as to control a voltage across the common mode capacitor (C_{CM}).

22. Electrical converter of claim 21, comprising measurement means for measuring a voltage signal at the middle voltage node (m) and at nodes (a, b, c) of the at least three phases, wherein the controller is operable to determine the common mode voltage signal injected to the third and fourth intermediate nodes (q, r) based on the measured voltage signals.

23. Electrical converter of claim 21 or 22, wherein the control unit is operable to add an offset to duty cycles of pulse width modulation signals controlling operation of active switches ($T_{DC,vp}$, $T_{DC,vn}$) of the second converter stage, thereby obtaining the common mode voltage signal injected to the third and fourth intermediate nodes (q, r).

24. Electric motor drive system (30), comprising the electrical converter of any one of the preceding claims.

25. Electric motor drive system according to claim 24, further comprising an electric motor comprising stator coils, wherein the stator coils are connected to act as a common mode filter choke and/or as a differential mode inductor of the DC link of the electrical converter.

26. Electric motor drive system according to claim 24 or 25, comprising a traction inverter operable to drive the electric motor, wherein the traction inverter is configured to operate as the second converter stage when operating the electrical converter.

27. Battery charging system, in particular for charging electric vehicle drive batteries, wherein the battery charging system comprises a power supply, the power supply comprising the electrical converter of any one of the claims 1 to 23.

28. Method of converting between an AC signal having at least three phases at at least three phase nodes (a, b, c) and a DC signal at a high node (p)

and a low node (n), comprising providing the electrical converter of any one of the claims 12 to 23, and switching by pulse width modulation between the at least three phase nodes (a, b, c) and the high node (p) and the low node (n) to obtain a switched voltage signal across the high node and low node, wherein a period of the switched voltage signal comprises a zero voltage level portion obtained by connecting the phase node having a smallest absolute instantaneous voltage value of the at least three phases of the AC signal to both the high node (p) and the low node (n).

29. Method of claim 28, wherein the switched voltage signal comprises a second voltage level portion obtained by connecting the phase node having the highest instantaneous voltage value of the at least three phases of the AC signal to the high node (p), and connecting the phase node having the lowest instantaneous voltage value of the at least three phases of the AC signal to the low node (n).

30. Method of claim 28 or 29, wherein the switched voltage signal comprises a third voltage level portion obtained by connecting the phase node having the smallest absolute instantaneous voltage value to the high node, and connecting the phase node having the lowest instantaneous voltage value of the at least three phases of the AC signal to the low node, or vice versa.

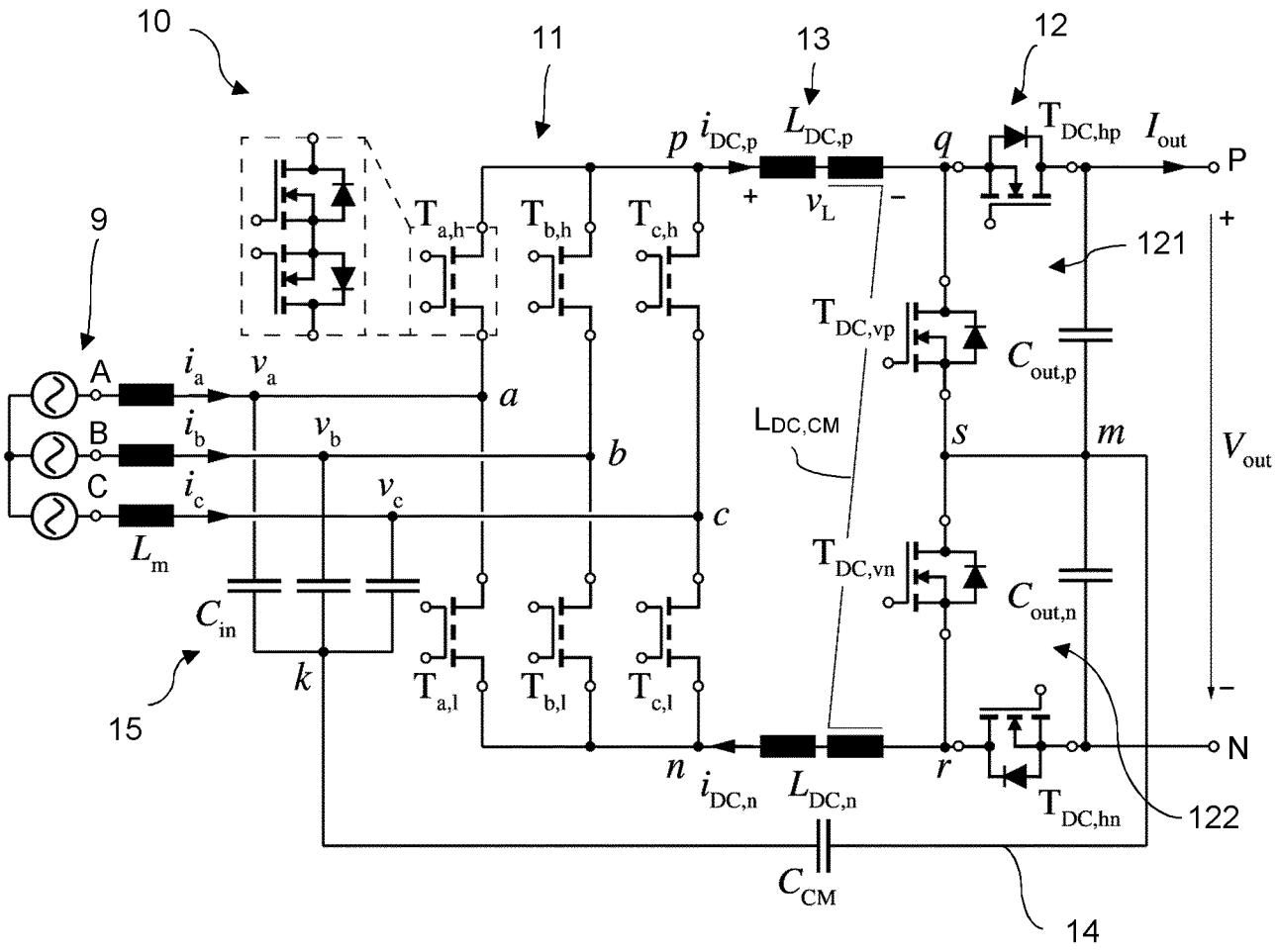
10
11
13
12
9
A
B
C
L_m
i_a
i_b
i_c
v_a
v_b
v_c
a
b
c
C_{in}
k
15
$T_{a,h}$
$T_{b,h}$
$T_{c,h}$
$T_{a,l}$
$T_{b,l}$
$T_{c,l}$
p
$i_{DC,p}$
$L_{DC,p}$
v_L
q
$T_{DC,hp}$
I_{out}
P
121
$T_{DC,vp}$
$C_{out,p}$
$L_{DC,CM}$
s
m
V_{out}
$T_{DC,vn}$
$C_{out,n}$
n
$i_{DC,n}$
$L_{DC,n}$
r
$T_{DC,hn}$
N
122
C_{CM}
14

FIG 1

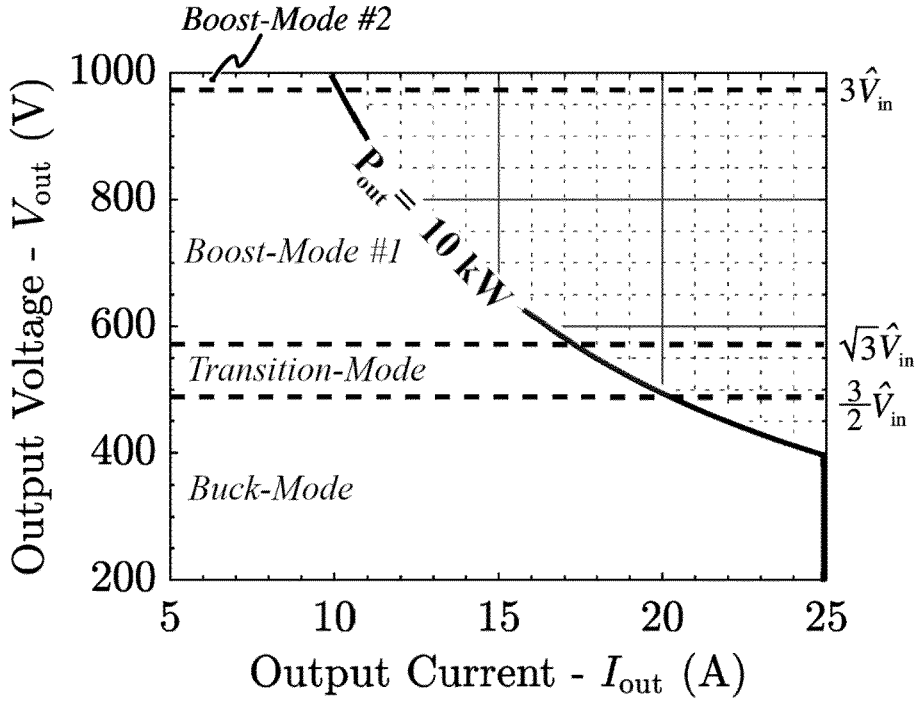
Boost-Mode #2
1000
800
600
400
200
$3\hat{V}_{in}$
$P_{out} = 10\,kW$
Boost-Mode #1
$\sqrt{3}\hat{V}_{in}$
Transition-Mode
$\frac{3}{2}\hat{V}_{in}$
Buck-Mode
Output Voltage - V_{out} (V)
5
10
15
20
25
Output Current - I_{out} (A)

FIG 2

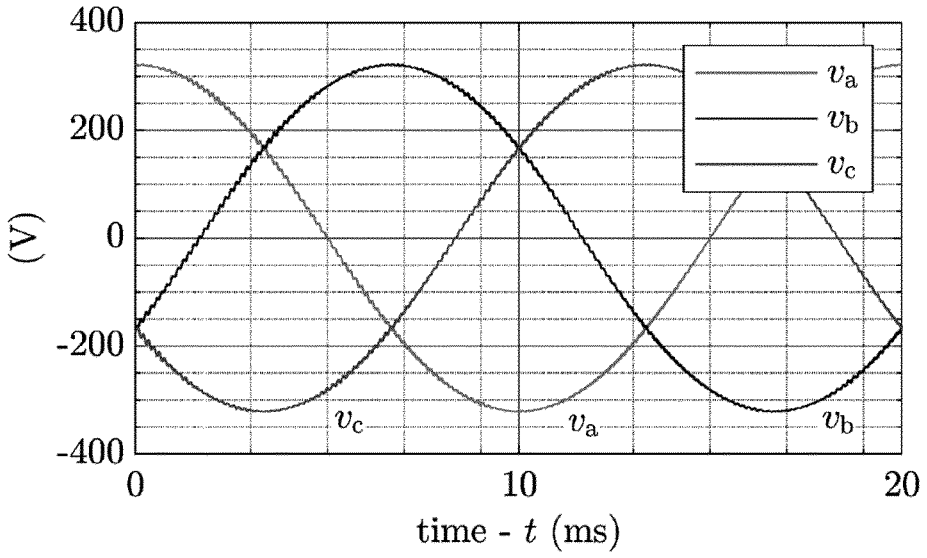
400
200
0
-200
-400
(V)
0
10
20
time - t (ms)
v_a
v_b
v_c
v_c
v_a
v_b

FIG 3a

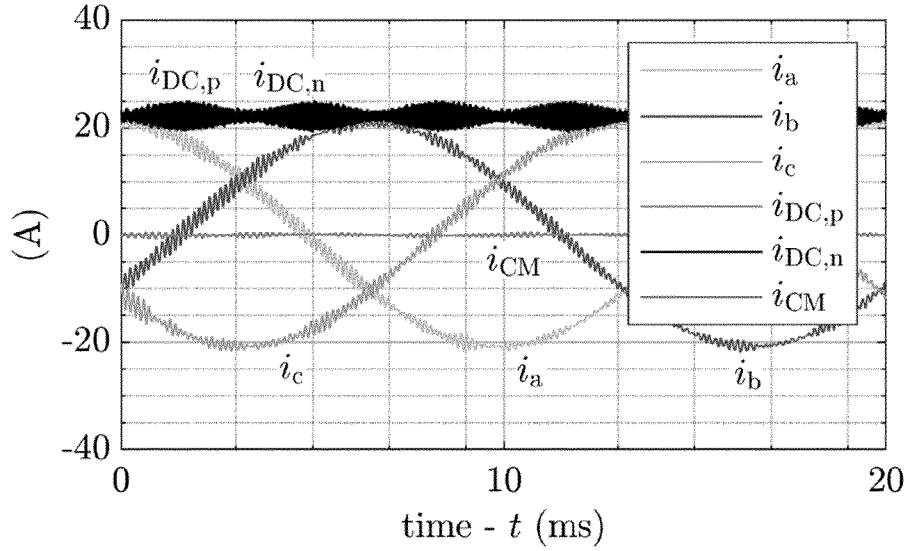
40
20
0
-20
-40
(A)
0
10
20
time - t (ms)
$i_{DC,p}$
$i_{DC,n}$
i_{CM}
i_c
i_a
i_b
i_a
i_b
i_c
$i_{DC,p}$
$i_{DC,n}$
i_{CM}

FIG 3b

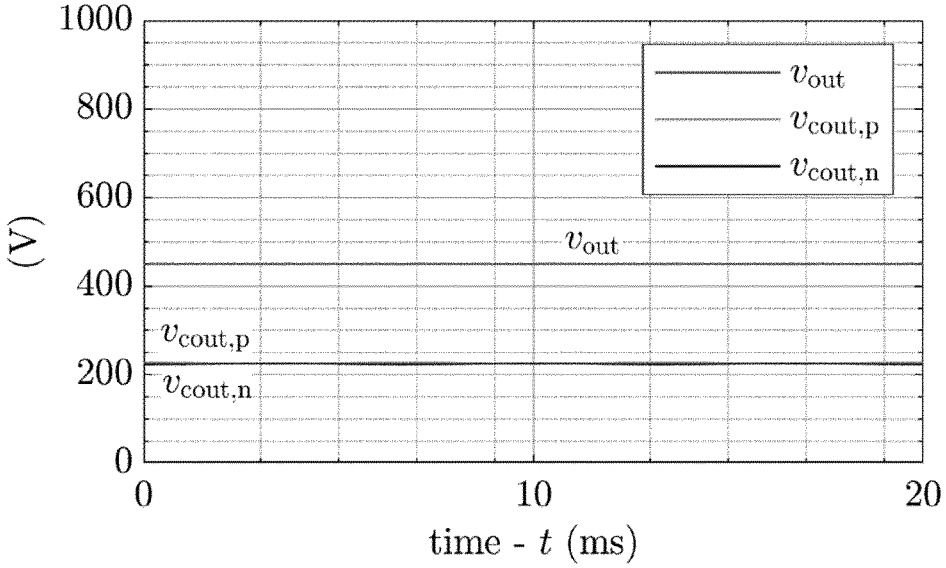
1000
800
600
400
200
0
(V)
0
10
20
time - t (ms)
v_{out}
$v_{\text{cout,p}}$
$v_{\text{cout,n}}$
v_{out}
$v_{\text{cout,p}}$
$v_{\text{cout,n}}$

FIG 3c

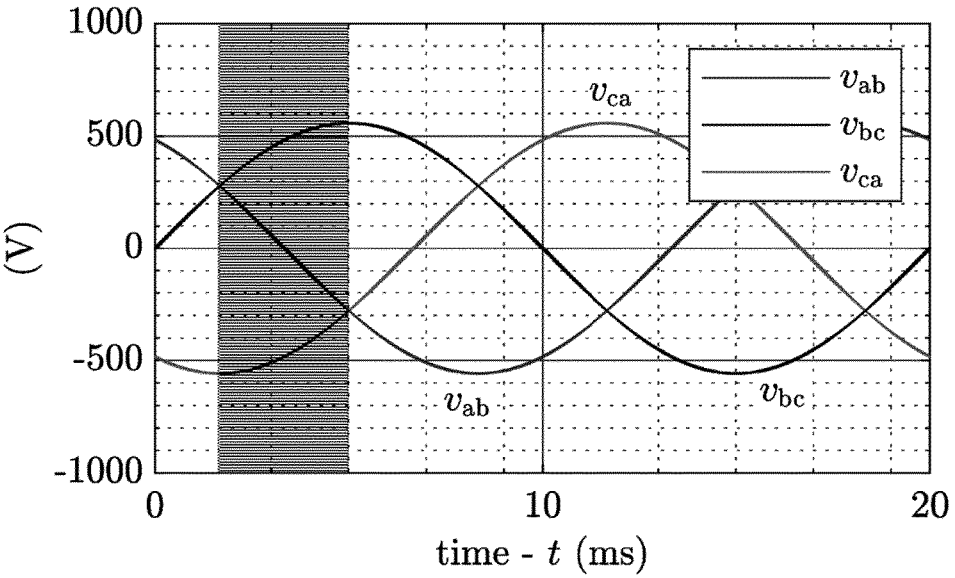
1000
500
0
-500
-1000
(V)
0
10
20
time - t (ms)
v_{ab}
v_{bc}
v_{ca}
v_{ca}
v_{ab}
v_{bc}

FIG 3d

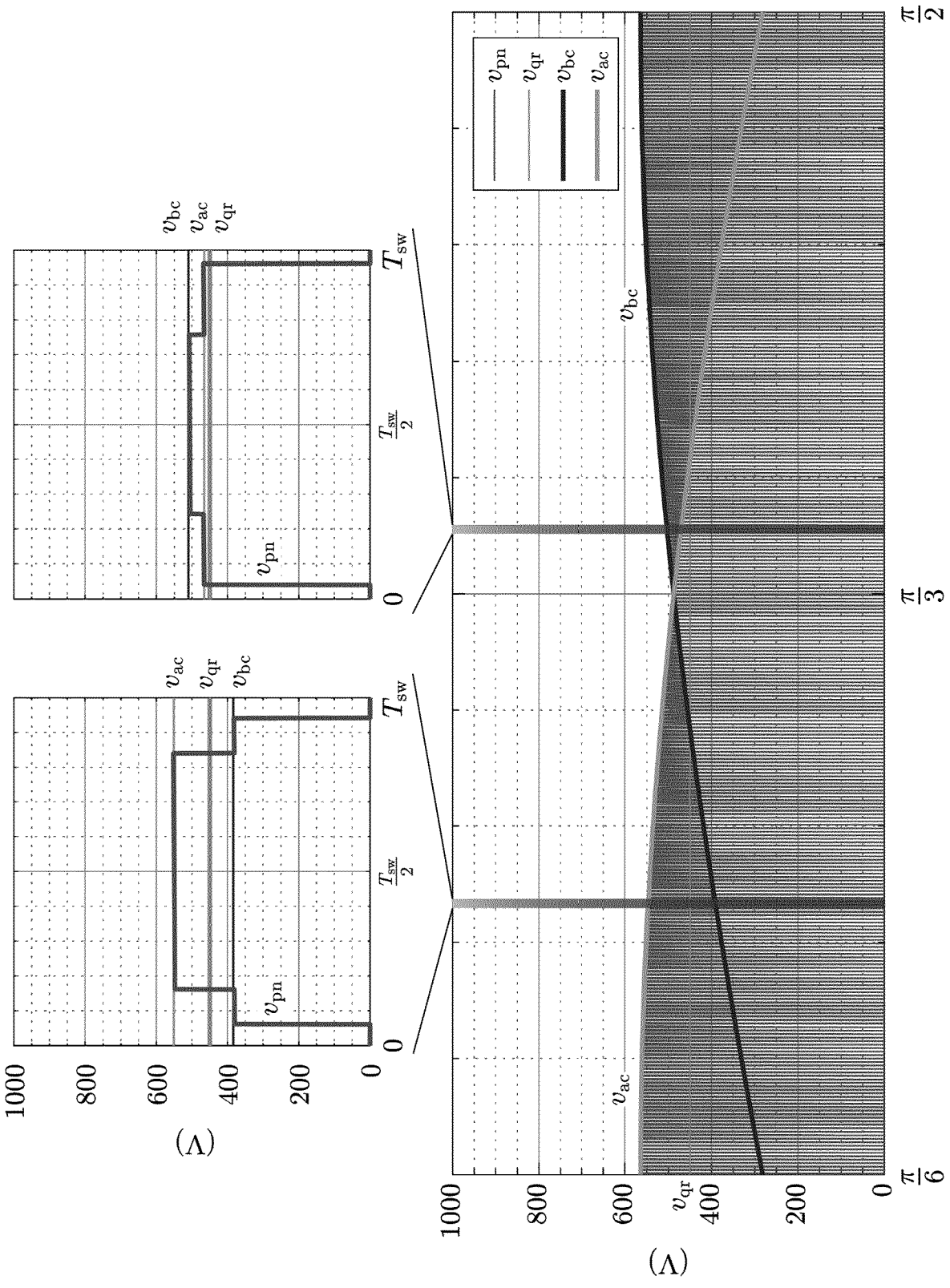
1000
800
600
400
200
0
(V)
v_{ac}
v_{qr}
v_{bc}
v_{pn}
0
$\frac{T_{sw}}{2}$
T_{sw}
v_{bc}
v_{ac}
v_{qr}
v_{pn}
0
$\frac{T_{sw}}{2}$
T_{sw}
v_{pn}
v_{qr}
v_{bc}
v_{ac}
v_{bc}
v_{ac}
1000
800
600
400
200
0
(V)
v_{qr}
$\frac{\pi}{6}$
$\frac{\pi}{3}$
$\frac{\pi}{2}$
Phase Angle - θ

FIG 4

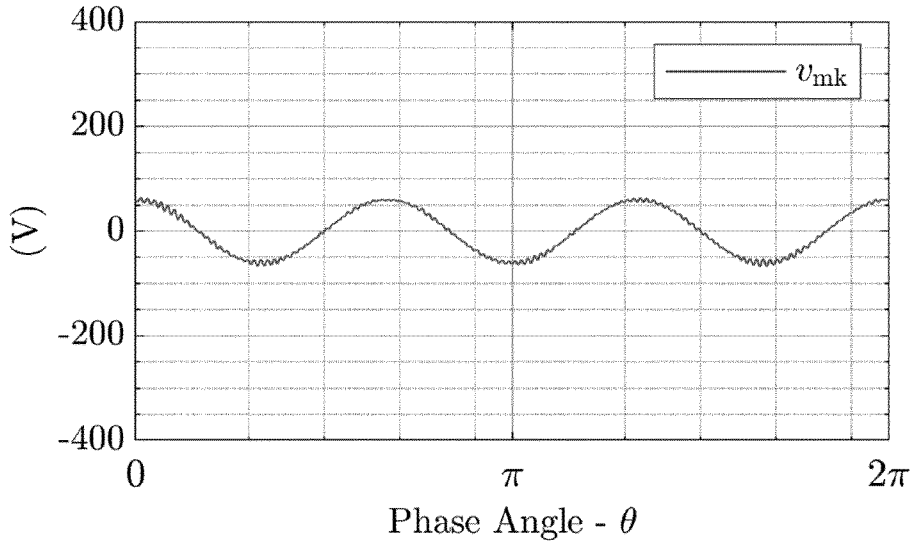
400
200
0
-200
-400
(V)
v_{mk}
0
π
2π
Phase Angle - θ

FIG 5a

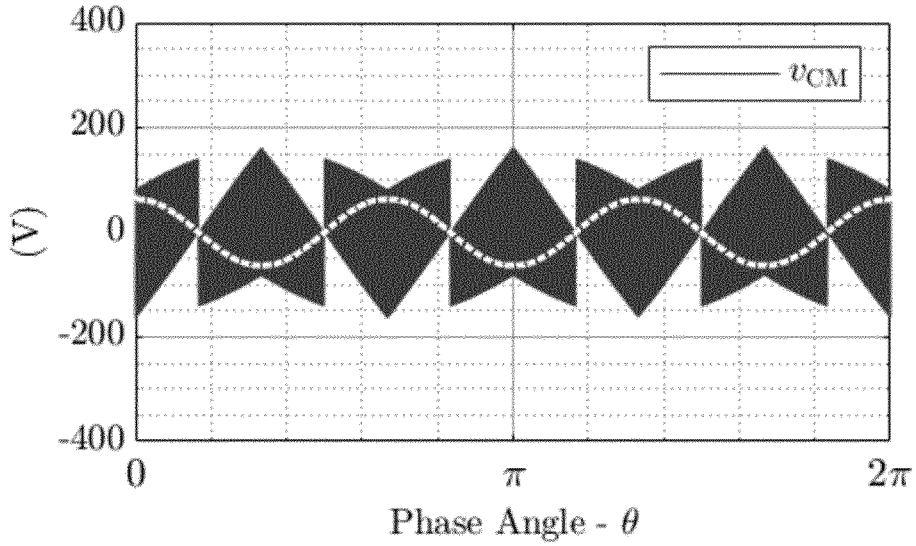
400
200
0
-200
-400
(V)
v_{CM}
0
π
2π
Phase Angle - θ

FIG 5b

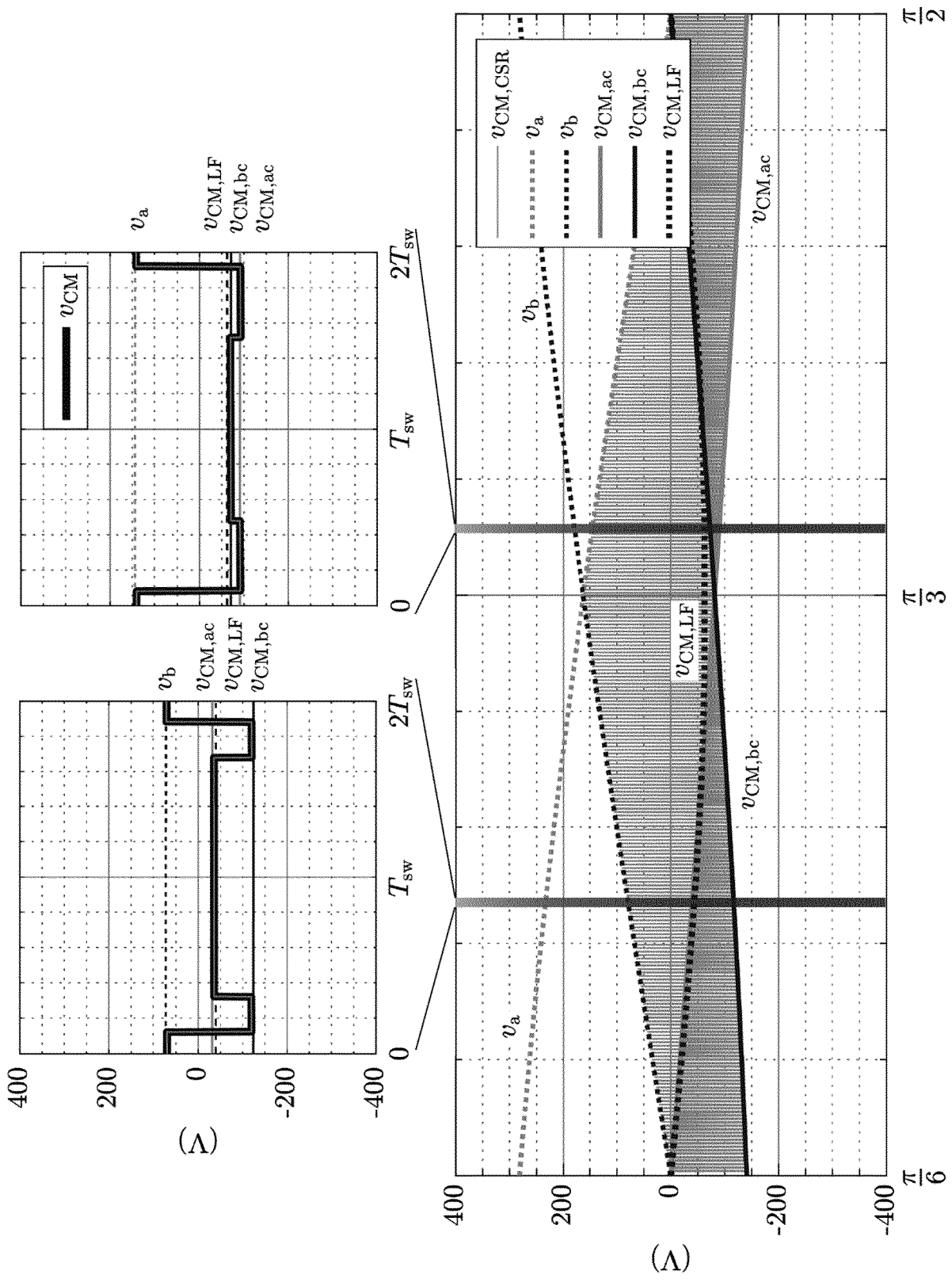
400
200
0
-200
-400
(V)
v_{CM}
v_a
$v_{CM,LF}$
$v_{CM,bc}$
$v_{CM,ac}$
v_b
T_{sw}
$2T_{sw}$
$v_{CM,CSR}$
$\frac{\pi}{6}$
$\frac{\pi}{3}$
$\frac{\pi}{2}$
Phase Angle - θ

FIG 6

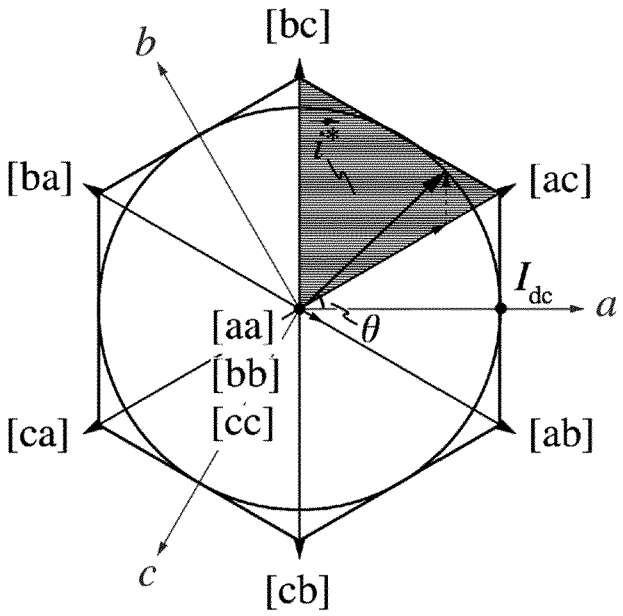
b
[bc]
[ba]
[ac]
$\vec{i}^*$
I_{dc}
a
[aa]
θ
[bb]
[cc]
[ca]
[ab]
c
[cb]

FIG 7

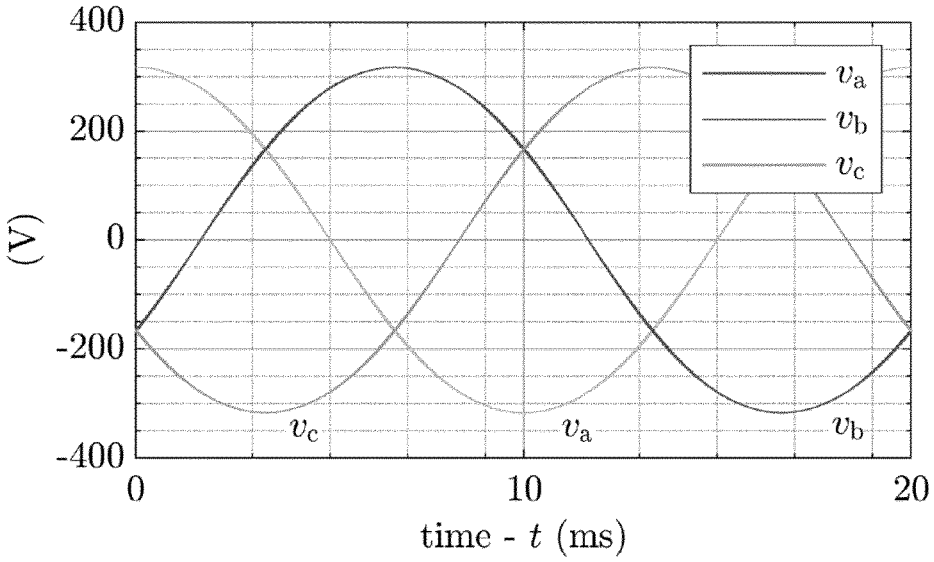
400
200
0
-200
-400
(V)
0
10
20
time - t (ms)
v_a
v_b
v_c
v_c
v_a
v_b

FIG 8a

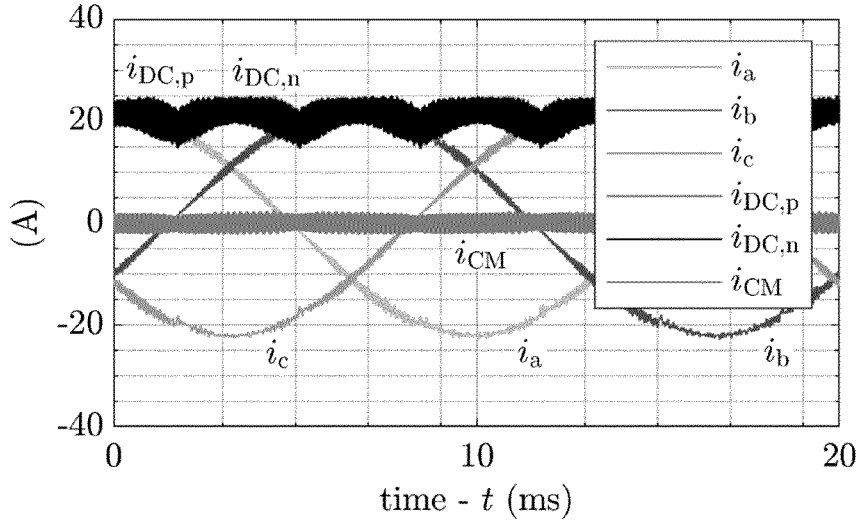

FIG 8b

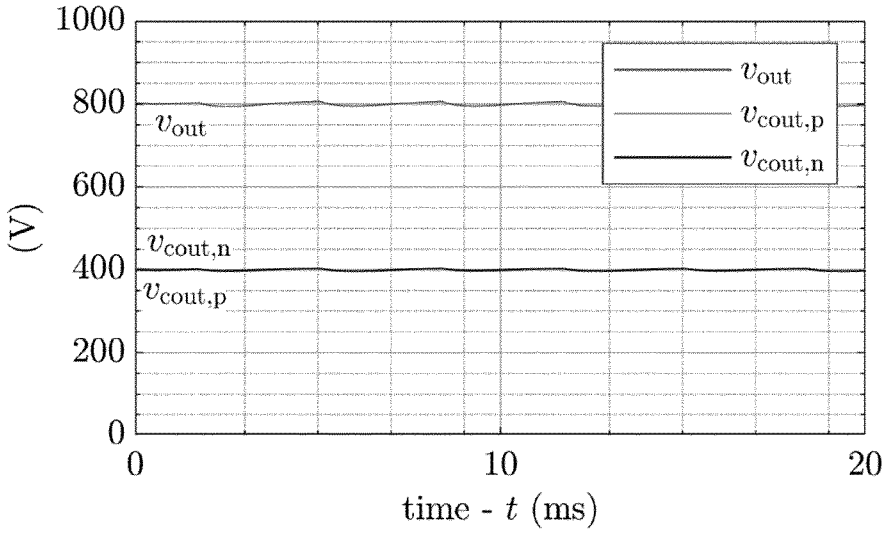

FIG 8c

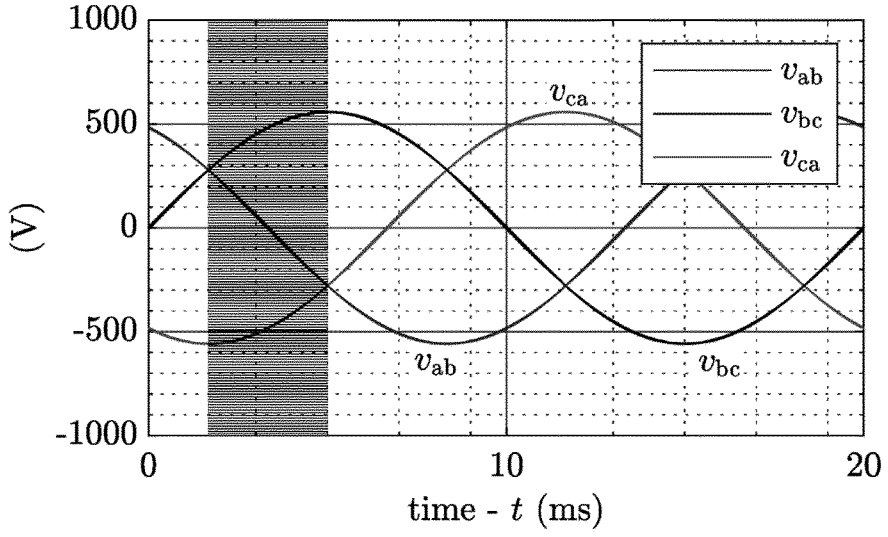

FIG 8d

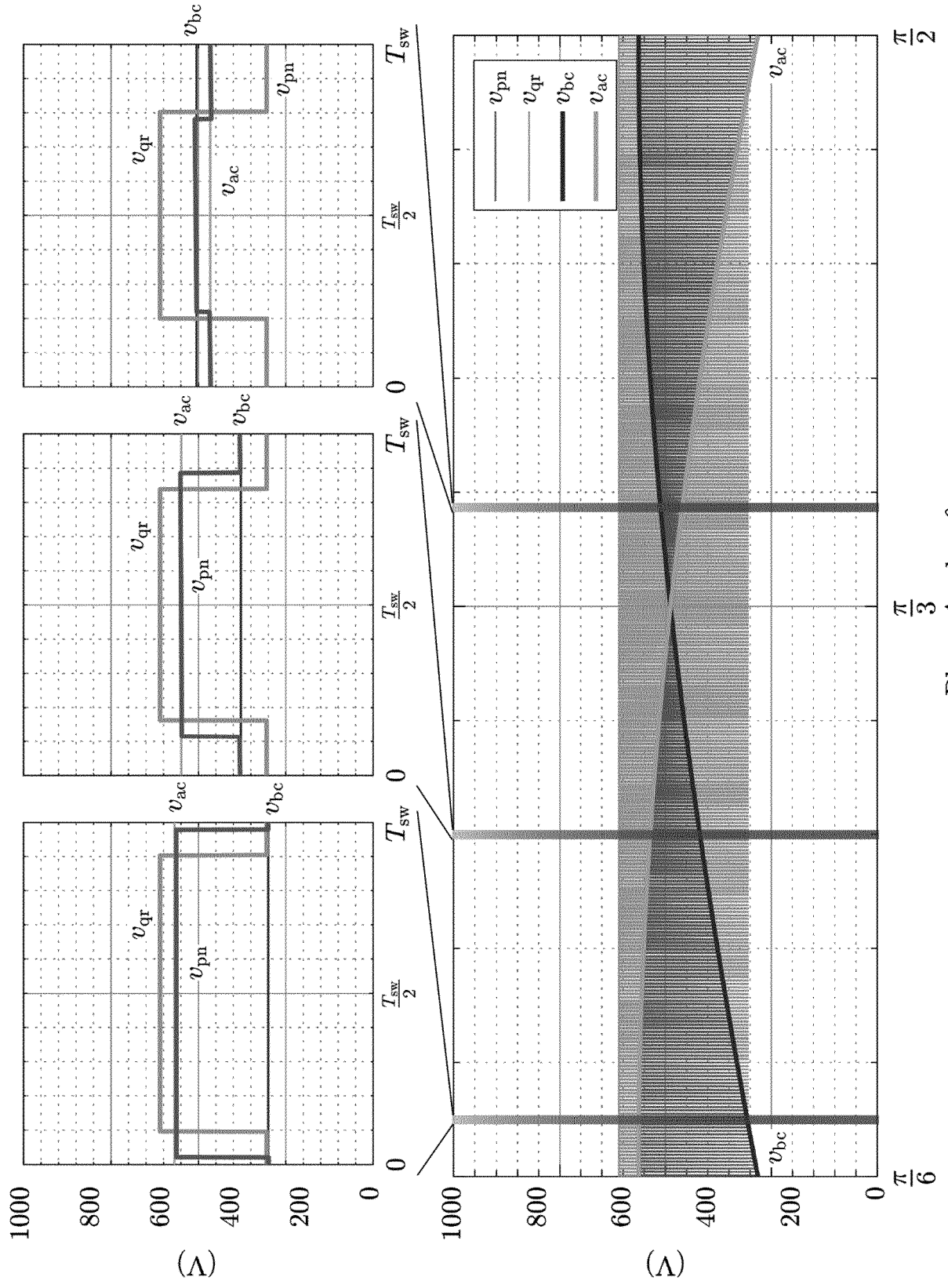
1000
800
600
400
200
0
(V)
0
$\frac{T_{sw}}{2}$
T_{sw}
v_{pn}
v_{qr}
v_{ac}
v_{bc}
$\frac{\pi}{6}$
$\frac{\pi}{3}$
$\frac{\pi}{2}$
Phase Angle - θ

FIG 9

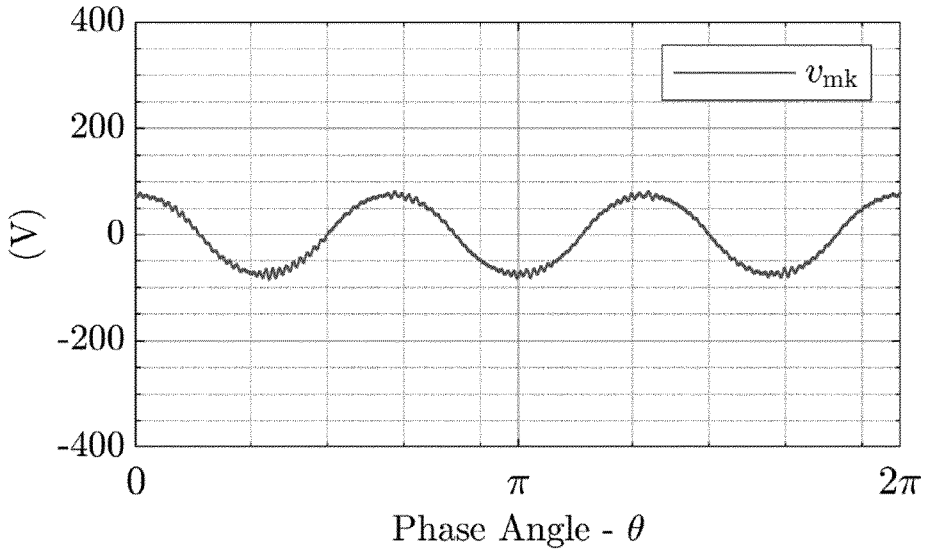

FIG 10a

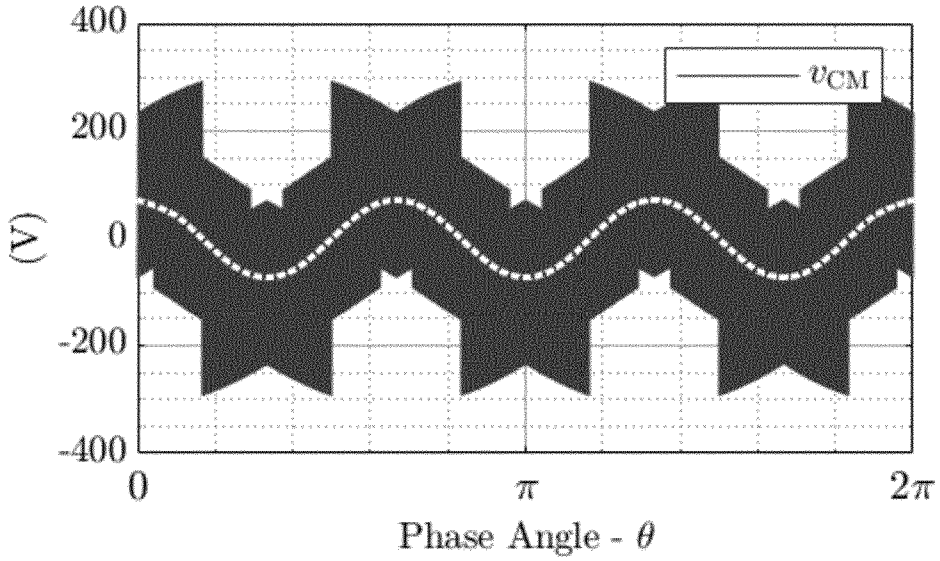

FIG 10b

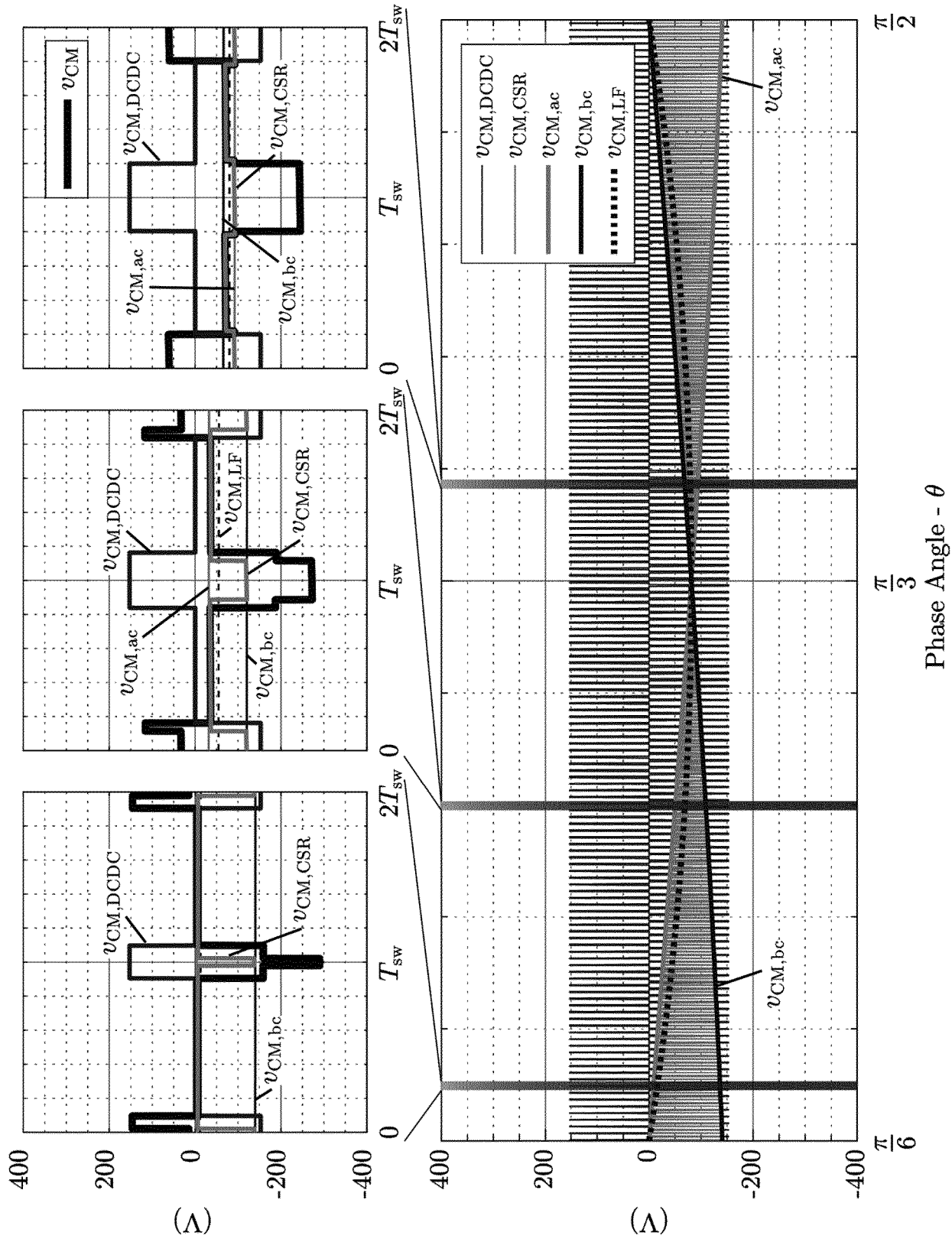
v_{CM}
$v_{CM,DCDC}$
$v_{CM,ac}$
$v_{CM,bc}$
$v_{CM,CSR}$
$v_{CM,LF}$
400
200
0
-200
-400
(V)
0
T_{sw}
$2T_{sw}$
$\frac{\pi}{6}$
$\frac{\pi}{3}$
$\frac{\pi}{2}$
Phase Angle - θ

FIG 11

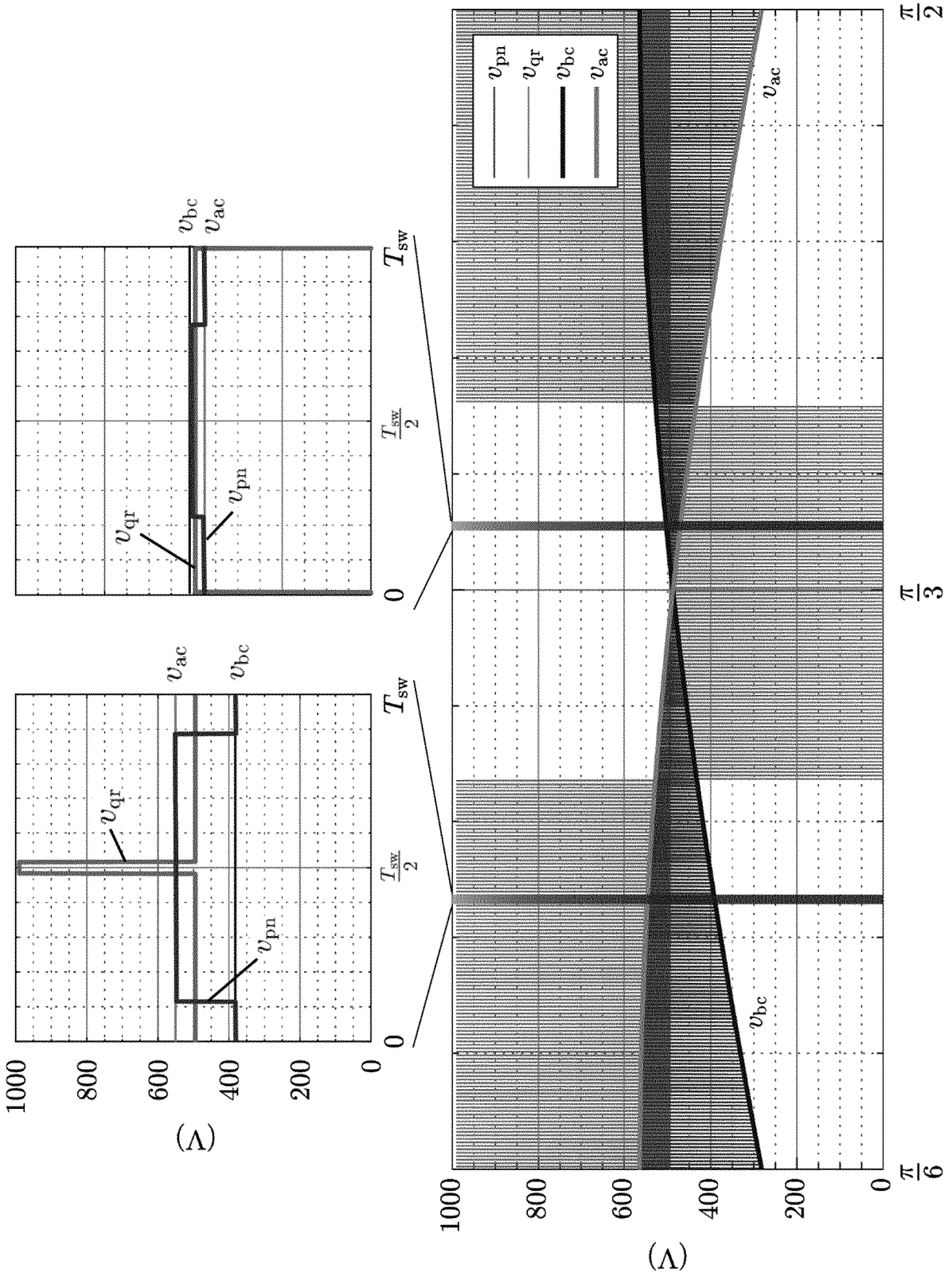
v_{pn}
v_{qr}
v_{bc}
v_{ac}
(V)
1000
800
600
400
200
0
$\frac{\pi}{6}$
$\frac{\pi}{3}$
$\frac{\pi}{2}$
Phase Angle - θ
T_{sw}
$\frac{T_{sw}}{2}$
0

FIG 12

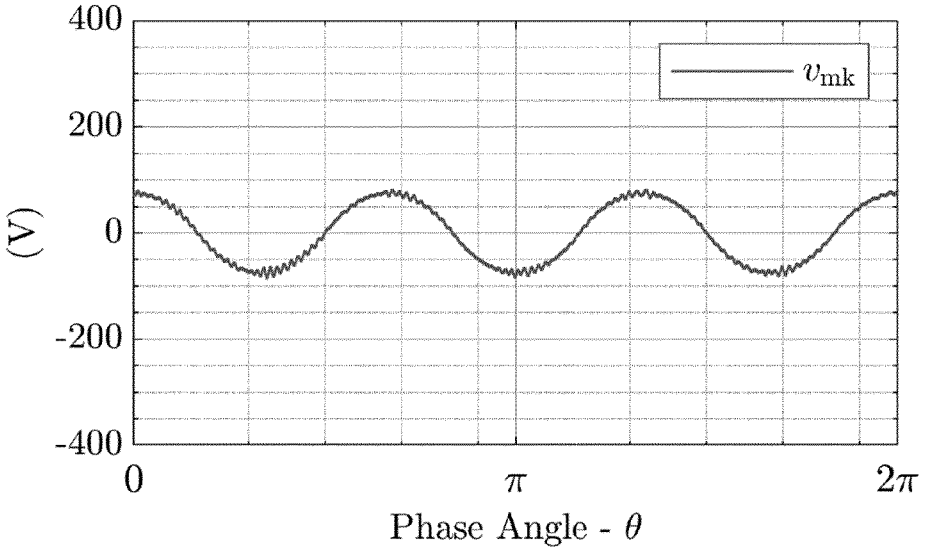

FIG 13a

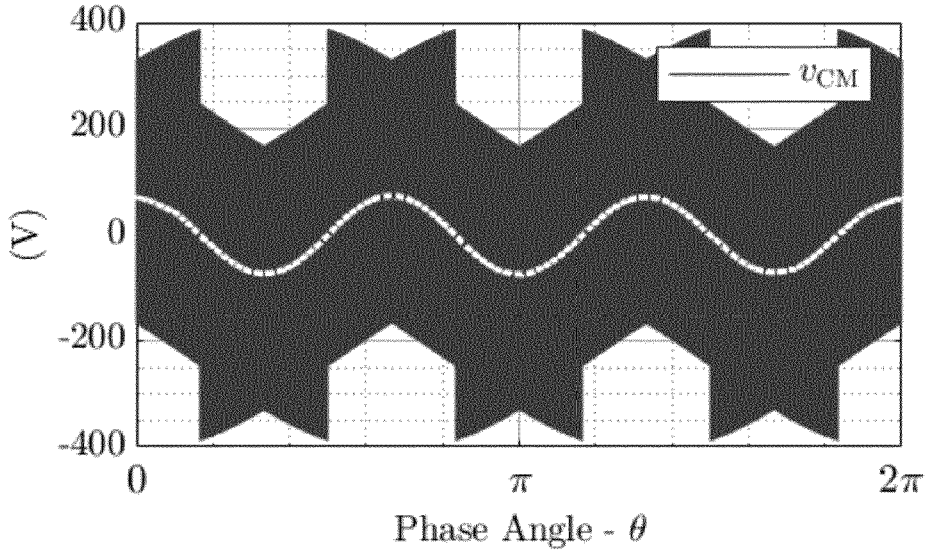

FIG 13b

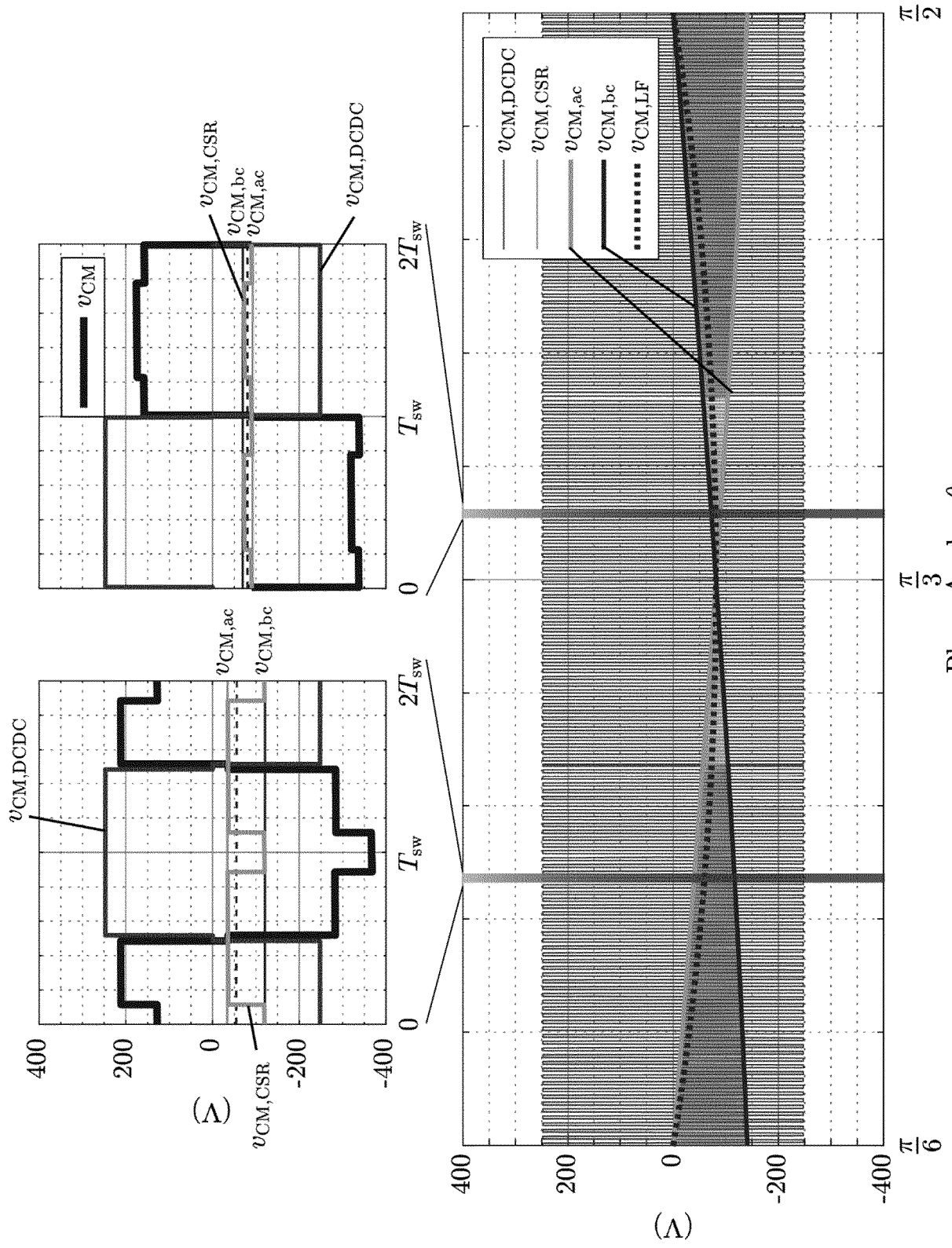
$v_{CM,DCDC}$
$v_{CM,CSR}$
$v_{CM,ac}$
$v_{CM,bc}$
v_{CM}
$v_{CM,LF}$
400
200
0
-200
-400
(V)
0
T_{sw}
$2T_{sw}$
$\frac{\pi}{6}$
$\frac{\pi}{3}$
$\frac{\pi}{2}$
Phase Angle - θ

FIG 14

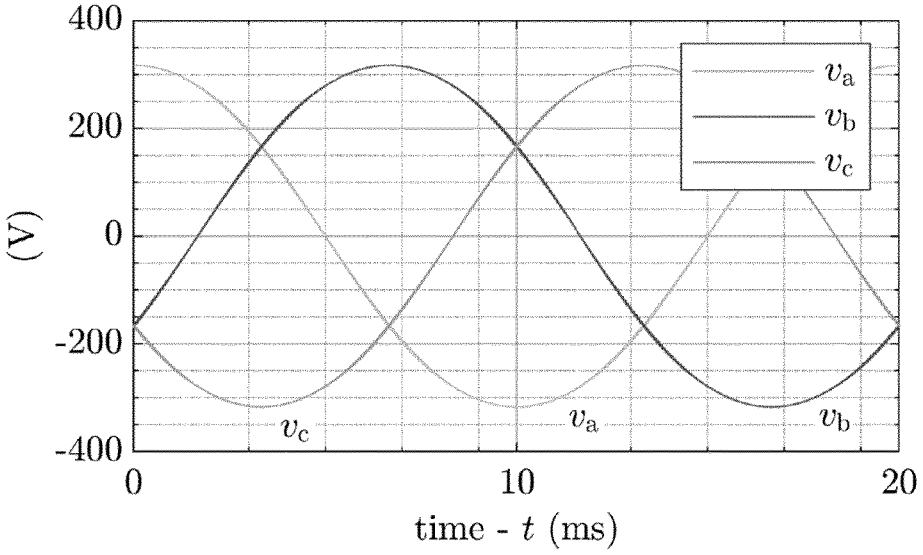

FIG 15a

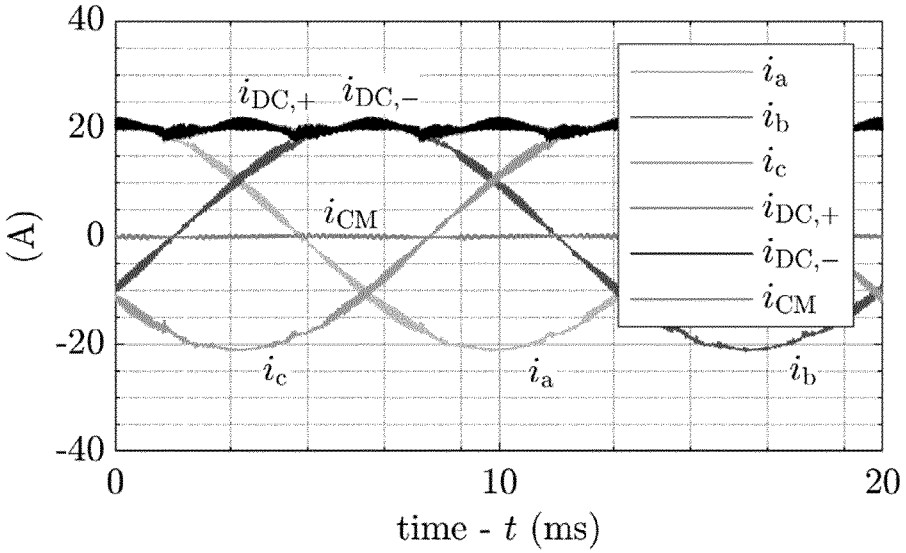

FIG 15b

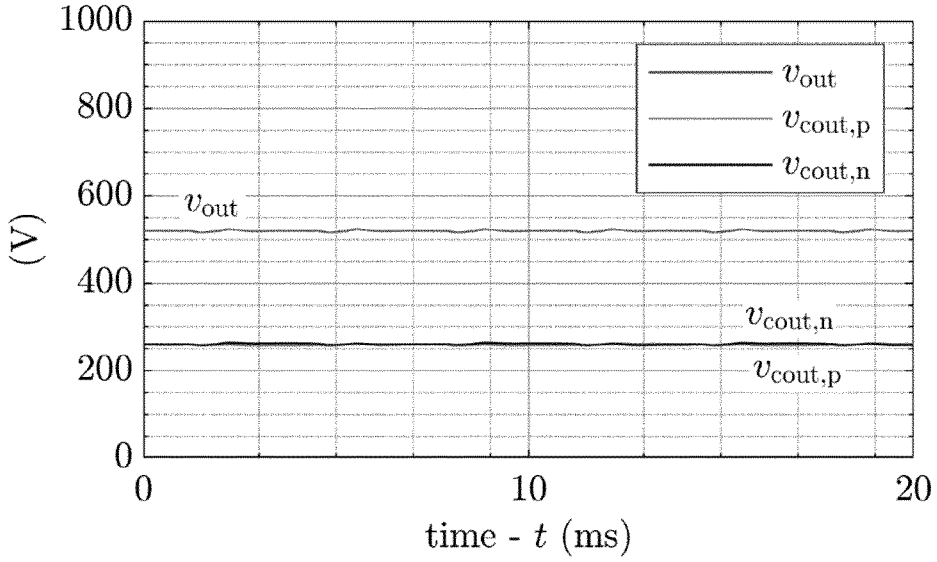

FIG 15c

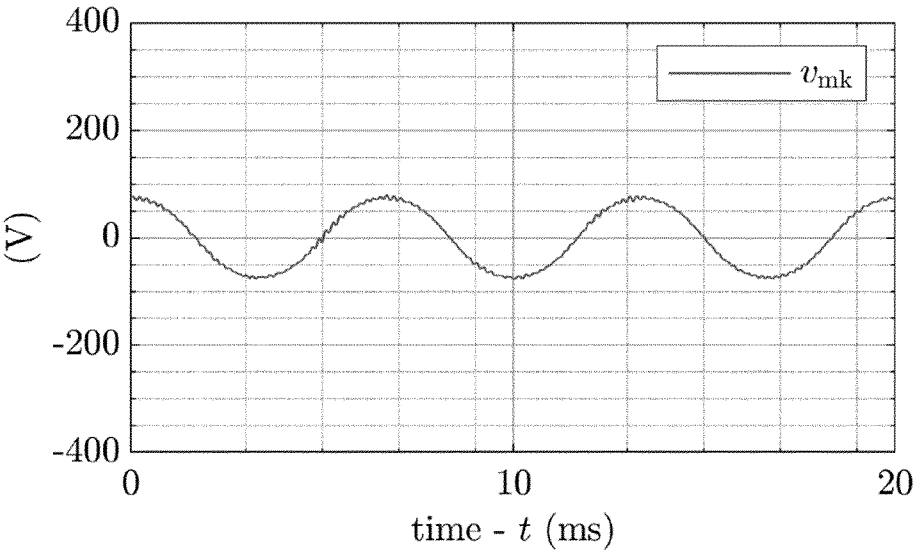

FIG 15d

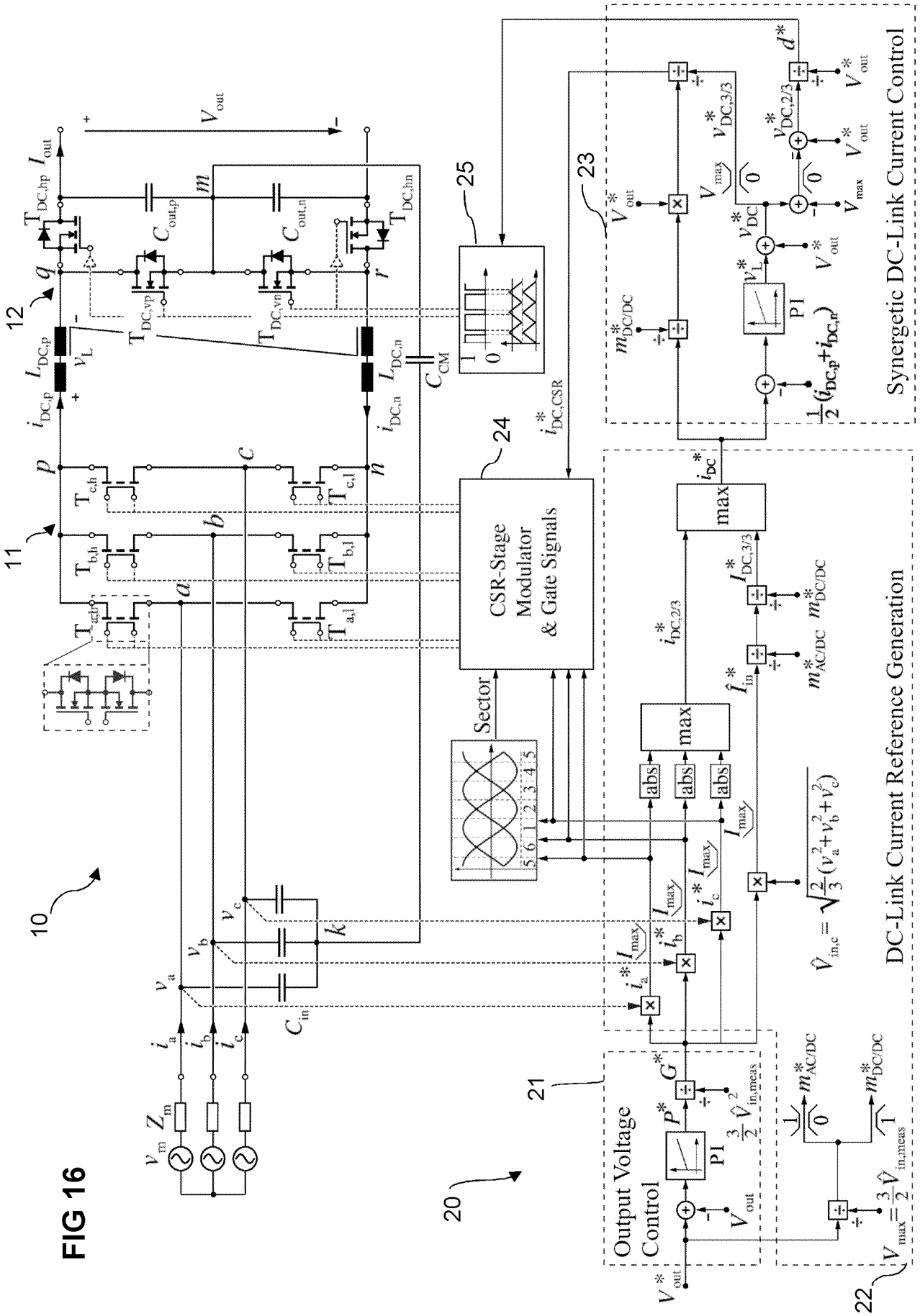
Synergetic DC-Link Current Control
DC-Link Current Reference Generation
Output Voltage Control
CSR-Stage Modulator & Gate Signals
Sector
PI
max
abs

FIG 16

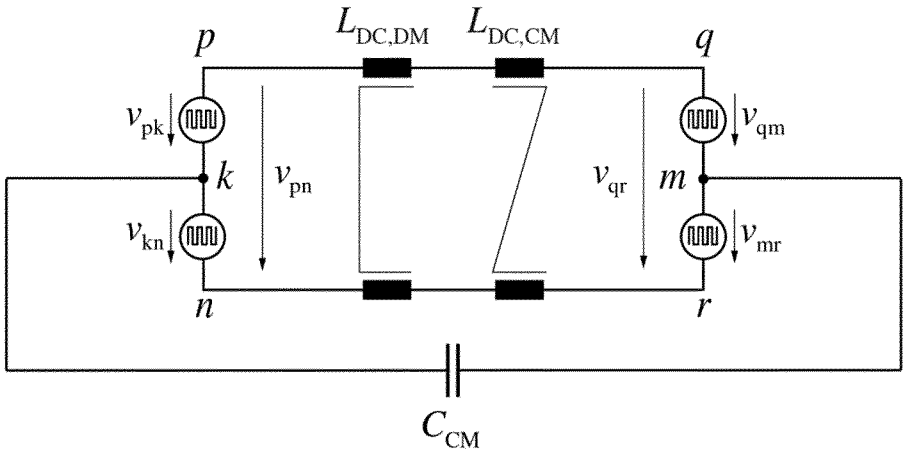

FIG 17a

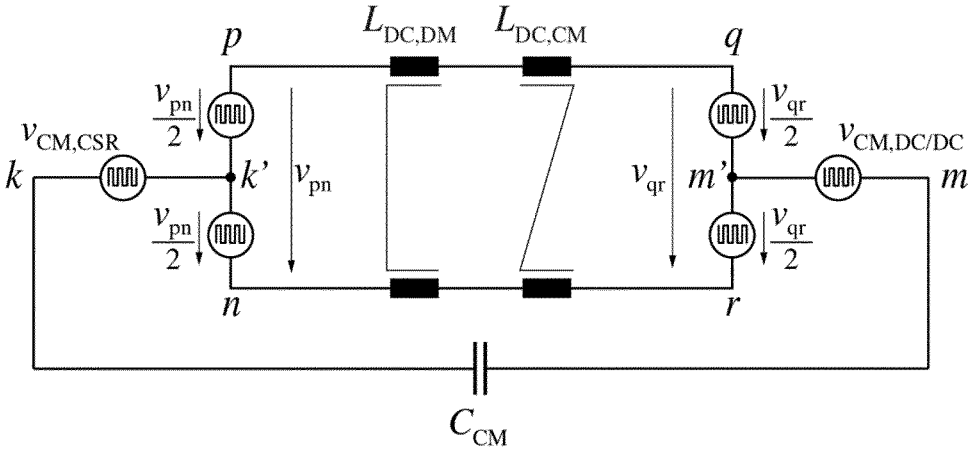

FIG 17b

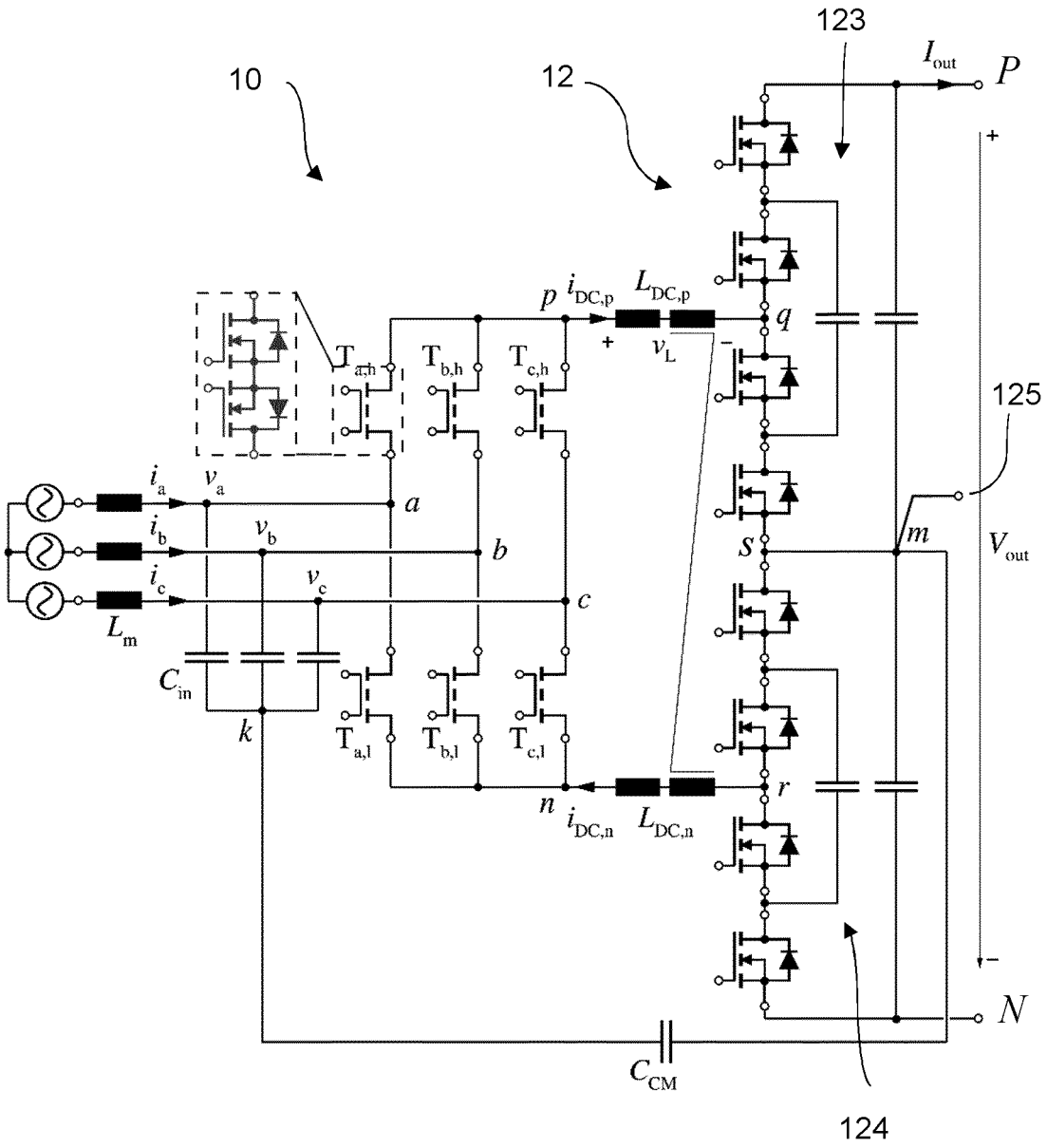
123
10
12
I_{out}
P
+
125
V_{out}
–
N
124
p
$i_{DC,p}$
$L_{DC,p}$
q
v_L
$T_{a,h}$
$T_{b,h}$
$T_{c,h}$
i_a
v_a
a
i_b
v_b
b
i_c
v_c
c
L_m
C_{in}
k
$T_{a,l}$
$T_{b,l}$
$T_{c,l}$
n
$i_{DC,n}$
$L_{DC,n}$
r
s
m
C_{CM}

FIG 18

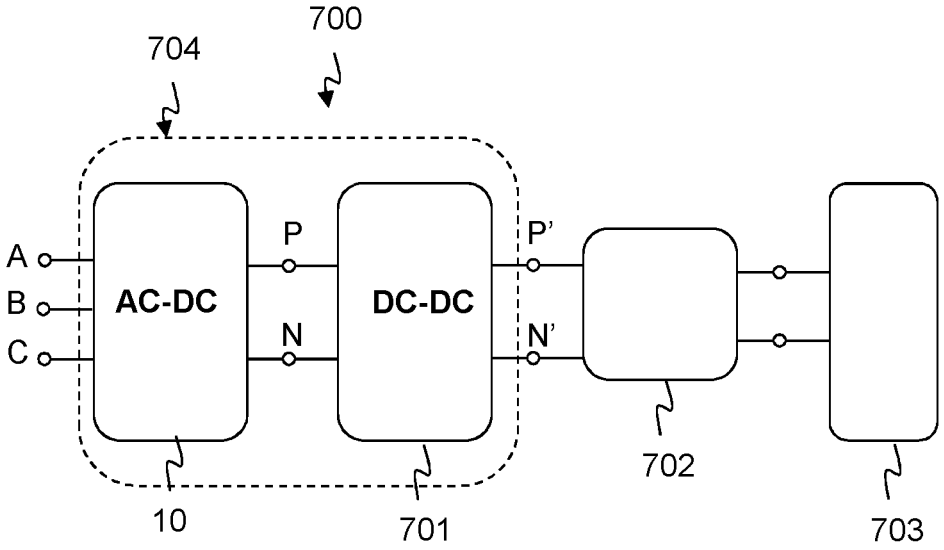
700
704
A
B
C
AC-DC
P
N
DC-DC
P'
N'
10
701
702
703

FIG 19

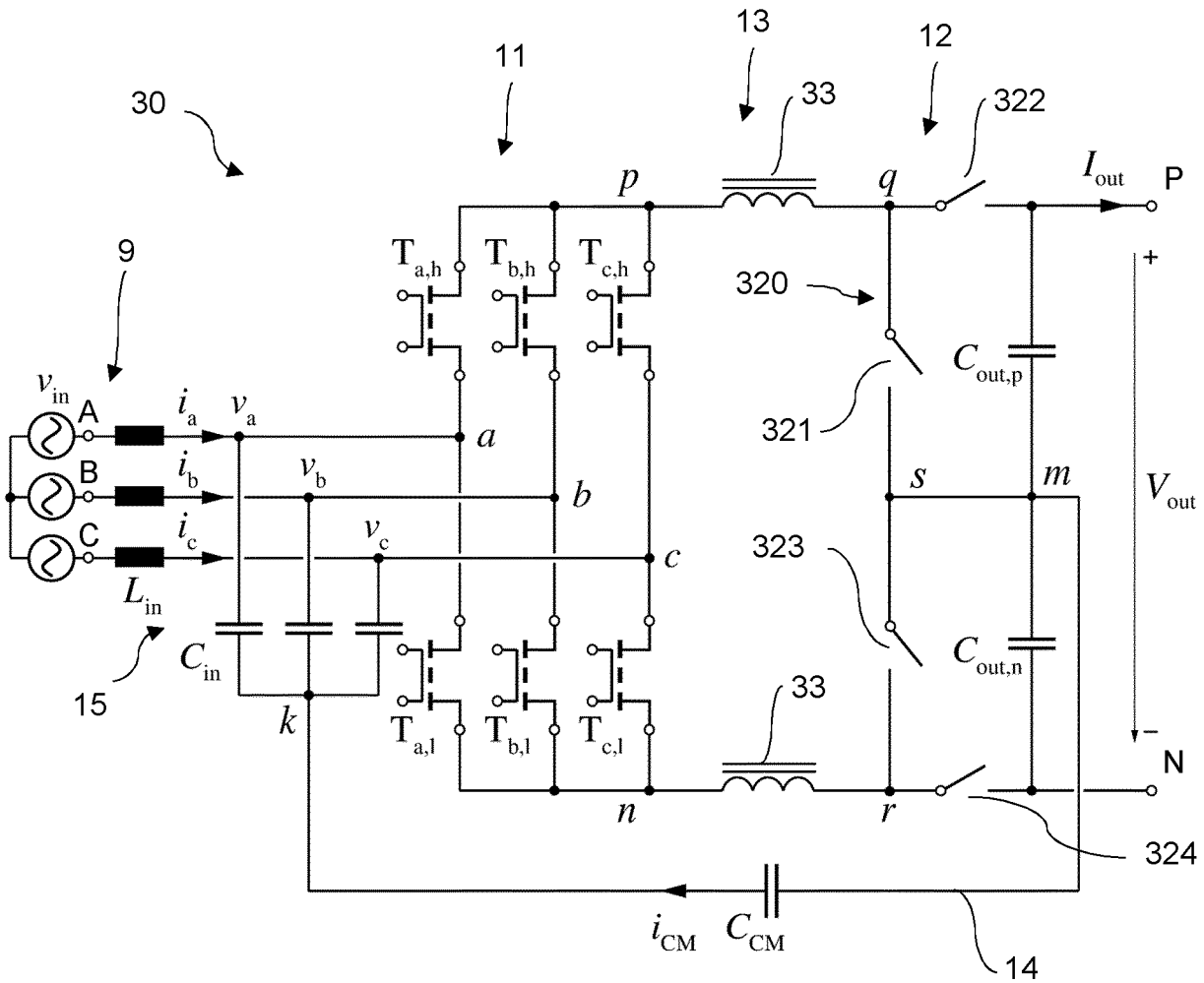
30
11
13
33
12
322
p
q
I_{out}
P
9
$T_{a,h}$
$T_{b,h}$
$T_{c,h}$
320
+
$C_{out,p}$
v_{in}
A
i_a
v_a
a
321
B
i_b
v_b
b
s
m
V_{out}
C
i_c
v_c
c
323
L_{in}
C_{in}
$C_{out,n}$
15
k
$T_{a,l}$
$T_{b,l}$
$T_{c,l}$
33
−
N
n
r
324
i_{CM}
C_{CM}
14

FIG 20

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2021/061203

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M1/12 H02M1/42 H02M3/158 H02M7/219 H02M7/5387 H02M7/797
ADD. H02M1/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013/235626 A1 (JANG YUNGTAEK [US] ET AL) 12 September 2013 (2013-09-12) paragraphs [0008], [0010] - [0013], [0023], [0065]; figures 9, 12, 13	1-30
A	AT 516 643 A1 (SCHNEIDER ELECTRIC POWER DRIVES GMBH [AT]) 15 July 2016 (2016-07-15) abstract; figure 1	1-30

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 June 2021	06/07/2021

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Van der Meer, Paul

1

Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	NADERI ROOZBEH ET AL: "Dual Flying Capacitor Active-Neutral-Point-Clamped Multilevel Converter", IEEE TRANSACTIONS ON POWER ELECTRONICS, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, USA, vol. 31, no. 9, 1 September 2016 (2016-09-01), pages 6476-6484, XP011604397, ISSN: 0885-8993, DOI: 10.1109/TPEL.2015.2501401 [retrieved on 2016-03-24] abstract; figure 1 -----	1-30
X	GUACCI MATTIA ET AL: "Novel Three-Phase Two-Third-Modulated Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs", 2019 IEEE 10TH INTERNATIONAL SYMPOSIUM ON POWER ELECTRONICS FOR DISTRIBUTED GENERATION SYSTEMS (PEDG), IEEE, 3 June 2019 (2019-06-03), pages 674-683, XP033601862, DOI: 10.1109/PEDG.2019.8807580 [retrieved on 2019-08-20] abstract Section II. DUAL-GATE MONOLITHIC BIDIRECTIONAL GAN E-FET; Section III. THREE-PHASE TWO-THIRD-MODULATED BUCK-BOOST CURRENT SOURCE INVERTER SYSTEM; figure 16a -----	1-30

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2021/061203

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013235626 A1	12-09-2013	NONE	
AT 516643 A1	15-07-2016	NONE	