Control and Implementation Aspects of a Multiphase Inductor-Based FIVR in 14 nm Bulk CMOS for Microprocessor Applications

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Abstract

This work investigates control and implementation aspects of a four-phase inductor-based Fully Integrated Voltage Regulator (FIVR) for microprocessor applications using the 14 nm Bulk CMOS technology. The considered converter system has a rated input voltage of $V_{\text{in}} = 1.6\,\text{V}$ and delivers an output power of $P_{\text{out}} = 1\,\text{W}$ at a nominal output voltage of $V_{\text{out}} = 0.8\,\text{V}$ to a microprocessor load. Voltage regulation allows varying the microprocessor supply voltage in the range of $0.6\,\text{V}$ to $1.0\,\text{V}$, which enables Dynamic Voltage and Frequency Scaling. From an in-depth evaluation of suitable control schemes, the V_2I_C control scheme, which uses the output voltage and the output capacitor current information as feedforward signals, is selected due to its fast response during transients and low implementation complexity, compared to fixed frequency hysteretic current mode control. The V_2I_C-controlled converter is implemented in transistor-level using models of the Global foundries' 14 nm LPP technology and Cadence simulation results confirm very fast output voltage recovery of $14.39\,\text{ns}$ during $625\text{mA}\,/\,0.5\text{ns}$ load current transients at nominal voltage and a settling time of $35\,\text{ns}$ during reference output voltage transients from $0.6\,\text{V}$ to $1.0\,\text{V}$ at nominal current .

Introduction and the State of the Art

State of the art buck-type fully integrated point-of-load converters typically employ hysteretic [1] or PWM based control schemes [2][3] for output voltage regulation. Besides zero DC offset in steady state and low output voltage ripple requirements, the voltage regulators used in microprocessor applications have also to react instantaneously to abrupt changes in reference voltage and load current. In [2] a conventional voltage mode control is used for output voltage regulation. In order to achieve acceptable recovery times a very high bandwidth controller is used. The converter is composed of 360 phases and is able to settle the output voltage during a load step of 8.5 A within 100 ns back to the programmed DC value. Reference [3] uses a modified form of peak-current mode control and manages to recover from a 600mA load step within 26.66 ns, taking into account the required DC deviation from the microprocessor load-line [7].

V_{in}	$1.6\ \text{V}$	Input Voltage	
V_{out}	$0.8\ \text{V}$	Nominal	Output Voltage
$V_{\text{out,min}}$	$0.6\ \text{V}$	Minimum	
$V_{\text{out,max}}$	$1.0\ \text{V}$	Maximum	
$\Delta V_{\text{out,pp}}$	$1\ \text{mV}$	Max. Output Voltage Ripple	
$I_{\text{out,max}}$	$1.25\ \text{A}$	Max. Output Current	
P_{out}	$1\ \text{W}$	Output power	
N_{phi}	4	Number of phases	
f_{sw}	$110\ \text{MHz}$	Buck Switching Frequency	
ΔV_{ref}	$0.5\ \text{V}$	Maximum voltage reference step	
$t_{\text{sett,ref}}$	$100\ \text{ns}$	Max. voltage reference settling time	
ΔI_{load}	$625\ \text{mA}$	Maximum voltage reference step	
$t_{\text{sett,load}}$	$70\ \text{ns}$	Max. load current step settling time	
$V_{\text{droop,load}}$	$70\ \text{mV}$	Max. voltage droop during load step	

Tab. 1 – Steady-state and dynamic system specifications

Fast reaction to load current steps is also achieved in [1], where load transients are detected by sensing the ground voltage noise, resulting in approximately 14 ns of reaction time for a 280 mA load current step.

The current mode PWM V_2I_C -control scheme [4] is selected for this work due to its capability of operation with constant switching frequency without the need of auxiliary circuits. By proper analytical tuning of the gains for the fast output voltage and output capacitor current feedback signals, fast transient detection and output voltage recovery is achieved, meeting the requirements of **Tab. 1**. Through regulation of the

peak current of each converter phase, balanced current distribution among the phases is achieved, which is necessary for maintaining high efficiency. More details on the control scheme comparison will be provided in the final version of this work.

System Specifications and Selected Topology

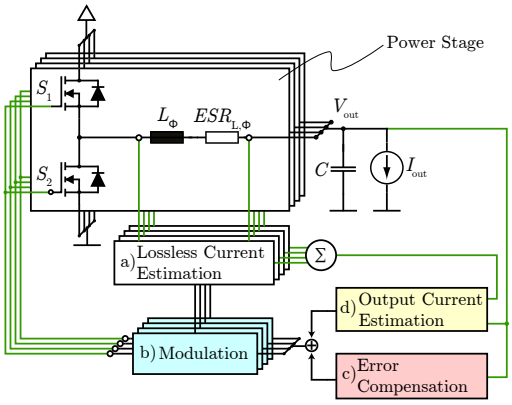

Fig. 1 – Considered multiphase converter topology with V_2I_C control scheme. Fig. 2 details the control blocks a) to d).

The selected topology, shown in **Fig. 1**, consists of a four-phase buck converter with interleaved gate signals reducing the requirements on minimum input and output capacitance values and improving transient performance compared to conventional single phase topologies [5]. The system's specifications, steady-state and dynamic operation parameters are listed in **Tab. 1**.

In contrast to [1], [2] and [3], which place the output filter passives in the package, this converter uses inductors and capacitors that are integrated into a silicon interposer. In order to achieve the required output voltage ripple and a phase current peak to average ratio PAR < 1.3, phase inductances of $15\ \mathrm{nH}$ and an output capacitance of $50\ \mathrm{nF}$ are selected. According with [5], those inductance and capacitor values would result in a high interposer power density of ~1 W/mm^2 using silicon devices.

Transistor Level Implementation in Cadence using the GF 14 nm LPP technology

The converter topology with V_2I_C control is shown in **Fig. 1**. The RC circuit in **Fig. 2a** is used to get an estimation of the phase currents. For lossless output current estimation an approach similar to [6] is employed, in which the capacitor current is sensed using the output voltage only. Power delivery to a microprocessor requires knowledge of the drawn output current to fulfill the load-line specifications [7]. The estimation of the output current is done separately using a second order band pass filter (**Fig. 2d**). For closing the output voltage loop, a type II compensation circuit as in **Fig. 2c** is used. The output of the compensator is summed with feedforward and feedback signals and is fed into the modulator circuit (cf. **Fig. 2b)**.

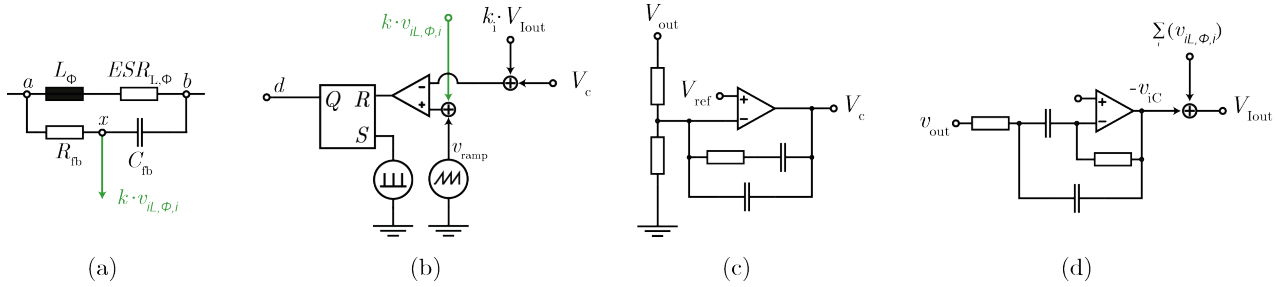

Fig.2 – (a) Circuit for phase current estimation, (b) Two stage OpAmp circuit, (c) Type II compensation circuit, (d) Second order band pass filter for capacitor current estimation

Fig. 3 shows the results of the V_2I_C control implemented in Cadence using the GF 14 nm LPP technology. The designed converter with V_2I_C control achieves very fast output voltage settling times during both, output voltage reference transients ($t_{\mathrm{sett,ref}} = 35\ \mathrm{ns}$ @ $0.6\ \mathrm{V}$ to $1.0\ \mathrm{V}$) and load transients ($t_{\mathrm{sett,load}} = 14.39\ \mathrm{ns}$ @ $625\ \mathrm{mA}$ step) . Schematic details about the implementation will be provided in the final version of this work.

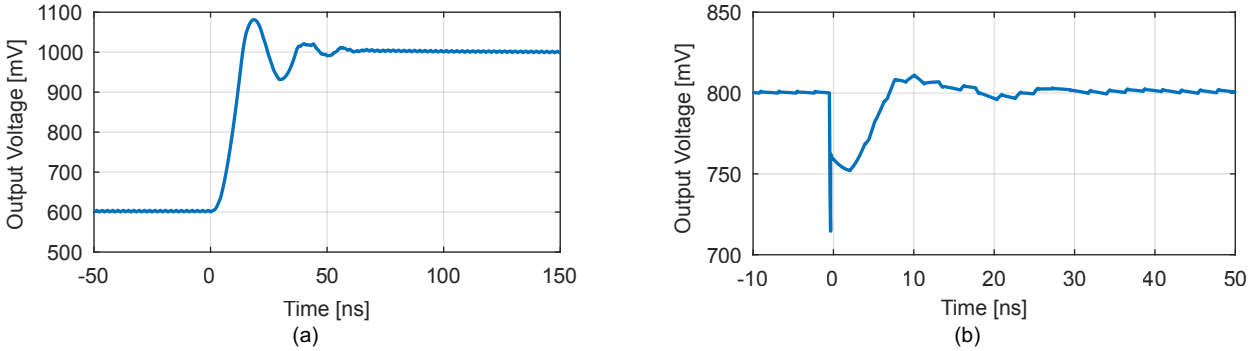

Fig. 3. – (a) Output voltage reference step (0.6 V to 1.0 V at nominal load current) and (b) load current step up transient (625 mA to 1.25 A step at nominal voltage) responses of the proposed converter using the V_2I_C control scheme.

Key Contributions and Conclusions

This work investigates selection and implementation of a high performant control scheme for a four-phase Inductor-based Fully Integrated Voltage Regulator (FIVR) using the 14 nm Bulk CMOS technology for Microprocessor Applications. The reasons for selecting the V_2I_C control scheme are presented and simulation results of a transistor level implementation using the GF 14 nm LPP technology are shown. The gain and time constant of the PI compensator are calculated such that high bandwidth and a phase margin of 70° result. With this, fast settling times and low overshoot are achieved for both, load current and reference voltage steps. The results demonstrate the good performance of the V_2I_C control scheme and the feasibility of a controller fulfilling the requirements, shown in Tab.1, in the 14 nm transistor technology. Compared to integrated voltage regulators in recent literature, the simulation results show comparable and better control performance. The controller designed in this work achieves a reference adjustment with a larger magnitude ΔV_{ref} in less time compared to the work done in [3]. In comparison to [2] and [3] the designed controller settles an output voltage disturbance caused by a higher load current perturbation in less time, so that a performance comparable to the hysteretic controlled system in [1] is achieved.

Design	2012 [3]	2014 [2]	2016 [1]	This work
Process	45nm CMOS	22nm CMOS	65nm CMOS	14nm CMOS
Modulation	PWM	PWM	Hysteretic	PWM
f_{sw} / N_{phi}	80 MHz / 4	140 MHz / 360	200 MHz / 4	110 MHz / 4
V_{in}	1.8 V	1.7 V	1.2 V	1.6 V
V_{out}	0.7 V to 1.3 V	1.05 V to 1.7 V	0.6 V to 1.0 V	0.6 V to 1.0 V
$\Delta V_{\mathrm{out,pp}}$	4 – 14 mV	3 mV	30 mV	1.2 mV
ΔV_{ref}	125 mV	-	-	400 mV
$t_{\mathrm{sett,ref}}$	70 ns			35 ns
ΔI_{load}	600 mA/ 100 ps	8500 mA / 1 ns	280 mA / 120 ps	625 mA / 0.5 ns
$t_{\mathrm{sett,load}}$	26.66 ns	70 ns	14 ns	14.39 ns
$V_{\mathrm{droop,load}}$	30 mV (with Loadline)	50 mV	78 mV	50 mV

Outlook and further improvements

The next steps in the course of this project include implementation of the converter chip layout and validation of the system's performance in the presence of the extracted layout parasitics and process tolerances. In addition, the compensation can be changed from a type II to a type III, essentially replace the PI by a PID compensator, increasing the control bandwidth and improving the system's dynamic performance.

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