Accurate Power Loss Model Derivation of a High-Current Dual Active Bridge Converter for an Automotive Application

Florian Krismer, *Student Member, IEEE*, and Johann W. Kolar, *Senior Member, IEEE*

***Abstract*—An accurate power loss model for a high-efficiency dual active bridge converter, which provides a bidirectional electrical interface between a 12-V battery and a high-voltage (HV) dc bus in a fuel cell car, is derived. The nominal power is 2 kW, the HV dc bus varies between 240 and 450 V, and the battery voltage range is between 11 and 16 V. Consequently, battery currents of up to 200 A occur at nominal power. In automotive applications, high converter efficiency and high power densities are required. Thus, it is necessary to accurately predict the dissipated power for each power component in order to identify and to properly design the heavily loaded parts of the converter. In combination with measured efficiency values, it is shown that conventional converter analysis predicts substantially inaccurate efficiencies for the given converter. This paper describes the main reasons why the conventional method fails and documents the different steps required to predict the power losses more accurately. With the presented converter prototype, an efficiency of more than 92% is achieved at an output power of 2 kW in a wide input/output voltage range.**

***Index Terms*—Bridge circuits, dc–dc power conversion, modeling, switching transients.**

I. Introduction

THE ever-increasing need for oil combined with a worldwide increasing traffic density, regulatory requirements for reduced emissions, and the ongoing discussion about climate change present strong incentives for the automotive industry to further improve the car drive trains, to reduce fuel consumption, and to lower emissions of exhaust gases that are harmful to the environment, such as carbon dioxide. The required efficiency improvement can be achieved with a hybrid drive train which combines an electric motor and a combustion engine in a way that facilitates the most desirable operation of each [1]. One or more additional energy sources, such as high-voltage (HV) batteries for continuous electric energy demand and ultracapacitors for high peak power [2], provide the electric power. Thus, in a hybrid electric vehicle, highly efficient and compact power electronic converters are required to provide the propulsion power and to facilitate the energy transfer between different dc voltage levels [3]. Depending on the drive train architecture, the electric power demand exceeds 10 kW [1], and accordingly, a dc bus voltage of more than 200 V is required in order to keep the currents within a technically reasonable range.

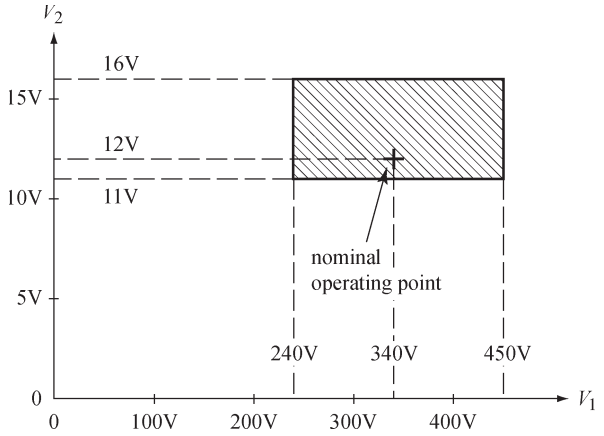

Fig. 1. Converter operating voltage ranges required for automotive application.

Currently, the electric system in a conventional car consists of a 14-V dc power system architecture that comprises of a 12-V battery, starter motor, battery charger, and all the vehicular loads such as lighting and radio [4]. Due to the long-term experience with the 14-V bus, the automotive industry is interested in keeping this system, including the 12-V battery and the low-voltage (LV) vehicular loads. Nowadays, the electric energy to the 14-V bus is provided with an alternator in a car. Taking advantage of the 200-V bus, a separate dc–dc converter can be used as a replacement for the alternator in order to supply energy from the HV dc bus to the 14 V power system [5]. Bidirectional power flow can be implemented to enable a power transfer from the 12-V battery to the HV bus (e.g., to charge the HV battery using another car). The required full power input and output voltage ranges of the bidirectional dc–dc converter for a typical automotive application are shown in Fig. 1. The power train supply voltage (V_1) is between 240 and 450 V, and the battery side voltage (V_2) ranges from 11 to 16 V. The HV ratio between V_1 and V_2 as well as the high automotive safety standards demand galvanic isolation [6], [7]. The required maximum output power is 2 kW over the specified voltage range. Hence, a large dc current of up to 200 A results on the battery side. In addition, a high converter efficiency (more than 90%), high reliability, and high power density are required [8]; this is typically achieved with soft switching techniques that result in low switching losses, and consequently, a high switching frequency can be employed [9]. The large input

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The authors are with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology Zürich, 8092 Zürich, Switzerland (e-mail: krismer@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

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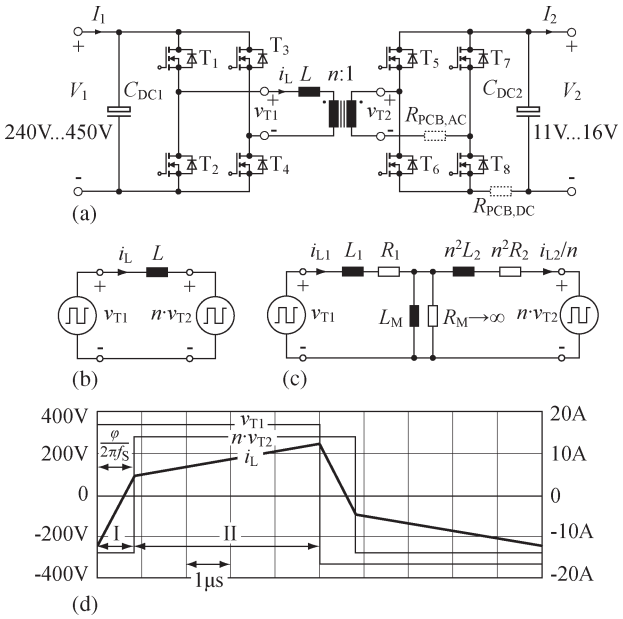

Fig. 2. (a) DAB topology. (b) Simple electrical DAB model. (c) Improved electrical DAB model; the resistors $R_{\mathrm{PCB,AC}}$ and $R_{\mathrm{PCB,DC}}$ model the PCB conduction losses (Section IV). (d) Voltage and current waveforms for $V_1 = 340$ V, $V_2 = 12$ V, $P_2 = 2$ kW.

and output voltage ranges, bidirectional power flow, galvanic isolation, and high-efficiency requirements limit the number of possible converter topologies. Among the most prominent converter candidates are the isolated boost, full bridge converter [10], and the L-type (or current doubler) converter [11] due to their suitability for high-frequency operation and due to the similarities to the well-known buck and boost converters. Both contain one or more comparably large dc inductors on the LV side and snubber circuits are required to avoid voltage spikes when switching.

The dual active bridge (DAB) converter [Fig. 2(a)] represents another prominent converter topology for the given application. Low number of components and its soft switching properties are the main advantages and allow the converter to be highly compact. However, depending on the operating voltages and the transferred power, large circulating currents may occur. Optimized modulation methods [12] or circuit variants—such as the three phase DAB [13]—enable a more effective converter utilization in order to reduce circulating currents and to obtain improved converter efficiency. For converter topologies without large dc inductors, further efficiency improvements are attained with resonant dc–dc converter topologies [14].

All the discussed topologies for isolated dc–dc converters are utilized most efficiently when the ratio of input to output voltage is close to the transformer turns ratio n. Therefore, a two-stage solution with an additional bidirectional buck/boost converter without galvanic isolation may be used to adjust the voltage applied to the isolation stage in order to achieve high total converter efficiency for the full operating range [15].

For the given application, the DAB topology [Fig. 2(a)], operated within the specified voltage ranges (Fig. 1), has been selected, mainly because it contains the lowest number of passive components: two capacitors, a high-frequency transformer, and a series inductance that can easily be integrated into the transformer. Its soft switching properties allow for an increased switching frequency and consequently for a reduced converter size. The topology is highly flexible regarding the optimization of key converter parameters such as the transformer turns ratio as well as the employed modulation method.

In order to design a high-efficiency converter with a LV and high-current port, a power loss model is necessary to identify and quantify the critical converter parts with respect to power dissipation. The possibility to accurately estimate the total power losses enables the prediction of efficiency for different operating points; the precise calculation of the distribution of the power losses allows for future optimization of converter components. Even more, a proper description of the converter losses facilitates a meaningful comparison of whether different modulation schemes result in an efficiency improvement for the investigated converter. However, up to now, no in-depth discussion of the underlying models used for the power loss calculation has been presented in the literature for this type of application.

In this paper, the DAB converter hardware is presented in Section II, and the basic mathematical model for the loss calculation is developed in Section III. Based on a comparison with measured efficiency values, the efficiencies calculated with the basic model prove considerably inaccurate. Thus, in Section IV, the required steps for a more accurate loss prediction are described and illustrated in detail. Finally, a comparison of the predicted losses and the experimental results is presented in Section V, and a high accuracy of the theoretical results is verified. In particular, the rapidly changing DAB transformer current is identified as the key property and needs to be determined precisely in order to allow for an accurate calculation of the converter losses (e.g., high-frequency conduction losses). Thus, the presented approach can also be employed to accurately predict the converter efficiency of high power density dc–dc converters different to the DAB (e.g., resonant dc–dc converters).

For all calculations and measurements in this paper, a reference temperature ($T = 25\ ^{\circ}\mathrm{C}$) has been used to avoid that two effects, namely, the electrical losses and the additional influence on the total losses due to components with different temperatures, occur at the same time. With this, a clear distinction between the different losses (e.g., copper losses, conduction losses, switching losses) of the power components is achieved. The shown experimental results have therefore been obtained at 25 °C with the run time of the converter being limited to 30 s in order to assure that no heating of the components occurs. In a next step, the discussed model can be extended with a coupled electrothermal converter model that includes the influence of raised component temperatures on the efficiency in order to accurately calculate the expected component temperatures [16], [17].

II. Automotive DAB

Prior to the construction of the converter prototype, a 3-D model of the converter was developed in order to determine a space-saving way to place the different components, such as the full bridge circuits (including gate drivers), transformer

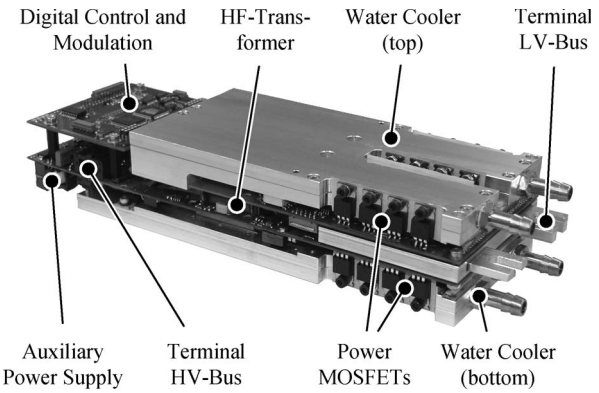

Fig. 3. Automotive DAB converter (273 × 90 × 53 mm).

and inductor, digital control, and auxiliary power supply. The resulting prototype comprises of the DAB converter, according to Fig. 3, with the LV side full bridge split up into two stages that are operated in parallel. The basic technical data of the converter are as follows:

1) PCB: four-layer PCB, 200-μm copper on each layer;
2) LV side:
   - dc capacitor: 96×10 μF/25 V/X5R in parallel;
   - switches: $8 \times$ IRF2804 in parallel;
3) HV side:
   - dc capacitor: 6×470 nF/630 V in parallel;
   - switches: SPW47N60CFD;
4) transformer core: two planar E58 cores;
5) transformer turns ratio: $n = 24 : 1$;
6) total DAB converter inductance: $L = 30.8$ μH;
7) switching frequency: $f_{\mathrm{S}} = 100$ kHz.

The converter prototype contains no additional voltage filtering besides the dc voltage capacitors, since the requirements for the maximum voltage ripple vary from application to application. In order to avoid ringing on the supply cables for the experimental setup, an external filter ($L = 20$ μH, $C = 220$ μF) is connected to the HV port and two external electrolytic capacitors ($C = 2 \times 10\,000$ μF) to the LV port.

A. Transformer

A planar core ($2 \times$ E58 : $58 \times 38 \times 21$ mm) is employed for the power transformer, mainly because of its advantageous properties with respect to high power density and excellent electromagnetic and thermal characteristics [16]. Its height (21 mm) is significantly lower than the total height of the converter (53 mm) what leaves space for a surrounding heat sink. For the selected ferrite core (material 3F3), a maximum peak flux density of 131 mT is calculated for $V_2 = 16$ V. The large safety margin between 131 mT and the saturation level of more than 300 mT has been selected to achieve low core losses and to prevent transformer saturation, since no dc coupling capacitors are implemented. DC coupling capacitors would require a significant realization effort, particularly on the LV side due to the high current ratings.

The transformer windings are made of litz wire and optimized according to [18] in order to achieve a minimal high-frequency resistance; the employed litz wire for both, the HV side winding and the LV side winding, contains 245 strands with a single strand copper diameter of 0.1 mm.

TABLE I
TRANSFORMER AND INDUCTOR PARAMETERS

	V_{core}	A_{core}	Total air gap	N	C_m	α	β
Transformer	24.6 cm^3	305 mm^2	–	24:1	14.5	1.34	2.63
Inductor	13.7 cm^3	387 mm^2	0.85 mm	5	14.5	1.34	2.63

TABLE II
MAXIMUM CURRENT STRESSES

	Low voltage side	High voltage side
Switch RMS currents	212A (11V ↔ 240V, 2kW)	8.8A (11V ↔ 240V, 2kW)
Switch peak currents	492A (11V ↔ 450V, 2kW)	20.5A (11V ↔ 450V, 2kW)
Transformer RMS currents	300A (11V ↔ 240V, 2kW)	12.5A (11V ↔ 240V, 2kW)
DC Capacitor RMS currents	242A (16V ↔ 240V, 2kW)	9.9A (11V ↔ 450V, 2kW)

B. Inductor

The converter inductor L can be placed on the LV side as well as on the HV side without affecting the converter functionality. For the given converter specifications, it is easier to place the inductor on the HV side due to the lower current rating, despite the larger inductance value required.

Since the transformer leakage inductance (10.2 μH) and the LV side stray inductances of MOSFETs and PCB (2.9 μH in total, when referred to the HV side) contribute to L, a reduced additional inductance value of 17.7 μH is required. The employed inductor is implemented using ferrite cores (three combinations E32/6/20 and PLT32/20/3 in parallel, material 3F3), according to Table I.

C. Power Switches

For the HV side full bridge, the SPW47N60CFD (CoolMOS) has been selected due to its low $R_{\mathrm{DS(on)}}$, fast switching, and the enhanced and robust body diode. With its nonlinear characteristic of the parasitic drain to source capacitance the proposed device is well suited for converters operating with zero voltage switching (ZVS).

The realization of the LV side full bridge is considerably more challenging, since high rms and peak current values (Table II) occur at 100-kHz switching frequency. Consequently, the DAB hardware prototype uses two full bridges which are operated in parallel, such that the current rating of a single full bridge is cut into half and thus, a converter realization using printed circuit boards becomes feasible. Each switch of the LV side full bridge is composed of eight IRF2804 MOSFETs ($R_{\mathrm{DS(on)}}$ of 2.2 mΩ) in parallel.

III. CONVENTIONAL ANALYSIS

A. Simple DAB Model

The heart of the DAB converter is the high-frequency power transformer connected in series to the converter inductor L,

enclosed by a HV full bridge and a LV full bridge [Fig. 2(a)]. These full bridge circuits generate rectangular voltages $v_{\mathrm{T1}}(t)$ and $v_{\mathrm{T2}}(t)$ with frequency f_{S}, a duty cycle of 50% and amplitudes V_1 and V_2, respectively. On the assumption of negligible conduction losses and a negligible transformer magnetizing current (which is sufficiently fulfilled for higher power levels), these considerations lead to the most simple lossless electrical DAB model [Fig. 2(b)] [19]. There, the resulting voltage $v_{\mathrm{T1}}(t) - n \cdot v_{\mathrm{T2}}(t)$ is applied to the inductor L where it excites a current $i_{\mathrm{L}}(t)$. This DAB model is used for the calculation of all the required quantities (e.g., the instantaneous and rms switch currents or the actually transferred power) in order to predict the efficiency.

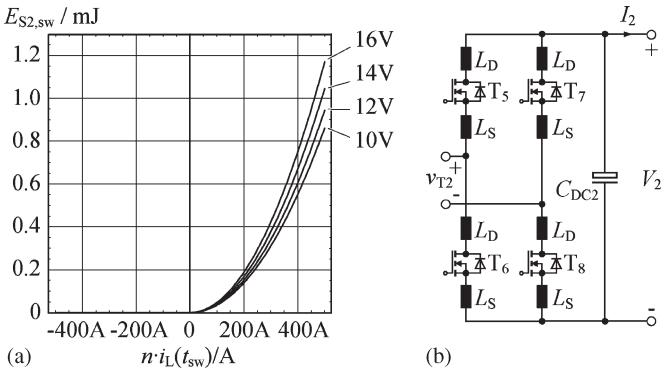

Fig. 4. (a) Estimated LV side switching losses. (b) LV side full bridge with the parasitic MOSFET lead inductances L_{S} and L_{D}.

B. Transformer, Inductor

For the given transformer (Section II-A) and for an output power higher than 20% of the nominal output power, the magnetizing current can be neglected. Thus, the transformer copper losses $P_{\mathrm{Tr,cond}}$ are calculated with the rms value $I_{\mathrm{L,RMS}}$ of the inductor current $i_{\mathrm{L}}(t)$ and the total HV side referred transformer copper resistance $R_{\mathrm{Tr}} = 250\ \mathrm{m\Omega}$ determined at the switching frequency. The transformer core losses are determined with the Steinmetz equation [20] with the Steinmetz parameters C_m, α, and β (Table I), the total core volume $V_{\mathrm{Tr,core}}$, and the peak magnetic flux density $\hat{B}_{\mathrm{Tr}} \approx V_2/(4\, f_{\mathrm{S}}\, N_2\, A_{\mathrm{Tr,Core}})$ assuming a negligible transformer stray inductance ($N_2 = 1$ for the given transformer). For the given converter, the losses predicted with the Steinmetz equation are considered accurate enough, since the core losses are found to account for less than 5% of the total losses. However, for different specifications, core losses may become more important and thus a more advanced method, e.g., the modified Steinmetz equation [20], finite element analysis or the use of measurement results [21], is required.

For the inductor, the copper losses are again calculated using the rms current $I_{\mathrm{L,RMS}}$ and the inductor copper resistance $R_{\mathrm{L}}(f_{\mathrm{S}}) = 22.5\ \mathrm{m\Omega}$, so $P_{\mathrm{L,cond}} = R_{\mathrm{L}}(f_{\mathrm{S}}) \cdot (I_{\mathrm{L,RMS}})^2$. The inductor core losses are estimated at the peak inductor current $\hat{I}_{\mathrm{L}}$ using the Steinmetz equation with $\hat{B}_{\mathrm{L}} \approx \mu_0 \cdot N_{\mathrm{L}} \cdot \hat{I}_{\mathrm{L}}/l_{\mathrm{L}}$ (N_{L}: number of turns, l_{L}: total air gap length; cf., Table I).

C. Power Switches

The calculation of the dissipated power in the switches considers two different loss mechanisms: conduction and switching losses. The conduction losses are calculated using the rms switch currents $I_{\mathrm{S1,RMS}}$ and $I_{\mathrm{S2,RMS}}$ for the HV side switches, $P_{\mathrm{S1,cond}} = 4 \cdot R_{\mathrm{S1}} \cdot (I_{\mathrm{S1,RMS}})^2$, and the LV side switches, $P_{\mathrm{S2,cond}} = 4 \cdot R_{\mathrm{S2}} \cdot (I_{\mathrm{S2,RMS}})^2$, respectively. Since every switch conducts current during half of the cycle time $T_{\mathrm{S}} = 1/f_{\mathrm{S}}$ in steady state operation, the rms switch currents are easily obtained from the rms inductor current $I_{\mathrm{L,RMS}}$

$$I_{\mathrm{S1,RMS}} = I_{\mathrm{L,RMS}}/\sqrt{2} \quad I_{\mathrm{S2,RMS}} = n \cdot I_{\mathrm{L,RMS}}/\sqrt{2}. \quad (1)$$

Typically, the influences of high-frequency skin and proximity effects are neglected for power semiconductor devices and thus the switch resistances for the selected MOSFETs (Section II-C) are obtained from the datasheet values with

$$R_{\mathrm{S1}} = R_{\mathrm{DS(on),SPW47N60CFD}} = 83\ \mathrm{m\Omega}$$
$$R_{\mathrm{S2}} = R_{\mathrm{DS(on),IRF2804S}}/8 = 2.2\ \mathrm{m\Omega}/8 = 275\ \mu\Omega \quad (2)$$

(on the LV side, eight MOSFETs are operated in parallel).

The calculation of the switching losses is more demanding, since they not only depend on the selected power MOSFETs themselves; surrounding parasitic components (e.g., PCB stray inductances) may as well influence the switching losses considerably. On the HV side, however, very low switching losses are obtained when ZVS is achieved. These can be neglected within the most simple loss model: $P_{\mathrm{S1,sw}} = 0$. In contrast, hard switching operation of the HV MOSFETs leads to excessive semiconductor losses and must be avoided in any case (e.g., using advanced modulation methods [12] or additional circuitry [22], [23]). On the LV side, soft switching (i.e., ZVS) is effectively not achieved, by reason of the energy stored in the parasitic drain and source lead inductances L_{D} and L_{S}. Accordingly, the switching losses, which occur if the condition for ZVS is satisfied, can be estimated with [12]

$$E_{\mathrm{S2,sw}} = \frac{1}{2} \cdot 2(L_{\mathrm{D}} + L_{\mathrm{S}}) \cdot [n \cdot i_{\mathrm{L}}(t_{\mathrm{sw}})]^2 \cdot \frac{V_{\mathrm{pk}}}{V_{\mathrm{pk}} - V_2}. \quad (3)$$

($n \cdot i_{\mathrm{L}}(t_{\mathrm{sw}})$ denotes the instantaneous MOSFET current at the switching time t_{sw}). With a repetition rate of $2f_{\mathrm{S}}$ (two half-cycles) and two simultaneously switching half-bridges, total losses of $P_{\mathrm{S2,sw}} = 4f_{\mathrm{S}} \cdot E_{\mathrm{S2,sw}}$ result. The parameters V_{pk} and $L_{\mathrm{DS}} = L_{\mathrm{D}} + L_{\mathrm{S}}$ need to be determined using datasheet values, calculations (e.g., finite element simulations) or measurements; for the given setup, the total parasitic inductance $L_{\mathrm{DS}} = 2.4$ nH, and the peak voltage $V_{\mathrm{pk}} = 32.7$ V have been identified using measured switching losses. If the LV side MOSFETs are operated with hard switching, comparably low switching losses occur (cf., Section IV-D) and thus hard switching losses may be neglected, there. The total estimated switching losses are shown in Fig. 4 ($i_{\mathrm{L}}(t_{\mathrm{sw}}) \leq 0$ denotes hard switching and $i_{\mathrm{L}}(t_{\mathrm{sw}}) > 0$ denotes the operation with ZVS).

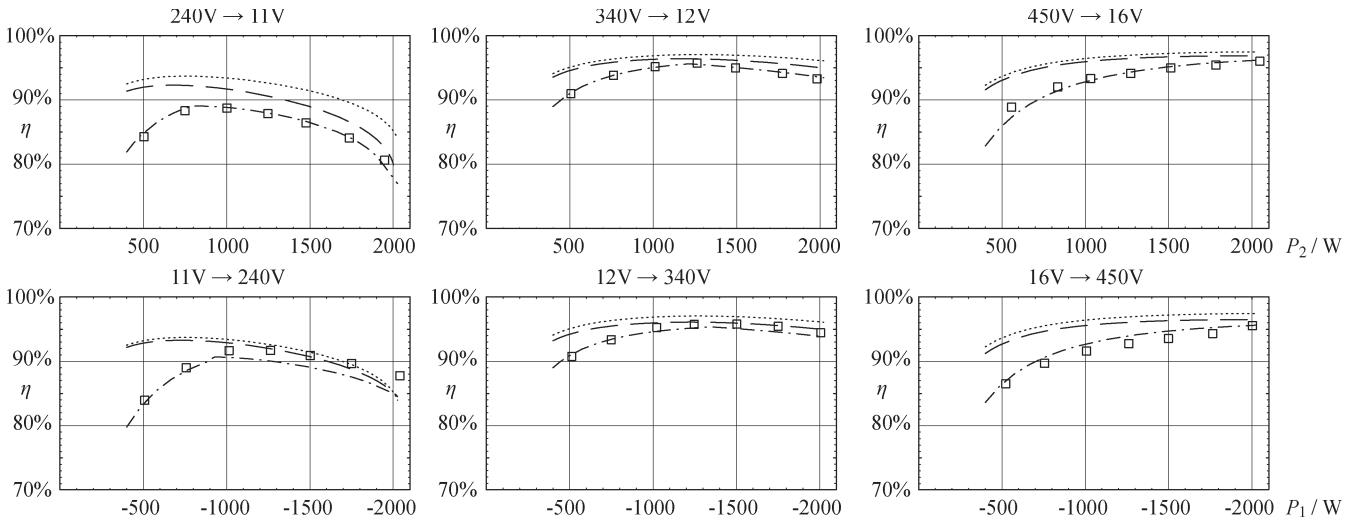

Fig. 5. Calculated and measured efficiencies for different operating points (negative power indicates power being transferred from the LV port to the HV port). (Dotted lines) Conventional analysis. (Dashed lines) Includes accurate conduction losses. (Dashed and dotted lines) Accurate conduction and switching losses. The boxes □ indicate measured values.

D. Total Losses, Predicted Efficiency

The total losses include all the discussed power losses as well as the auxiliary power required on the HV side ($P_{1,\mathrm{aux}}$) and on the LV side ($P_{2,\mathrm{aux}}$): the HV side auxiliary supply powers the DSP plus the HV side gate drivers and the LV side auxiliary supply provides power to the LV side gate drivers. Approximately constant power consumption has been measured

$$P_{1,\mathrm{aux}} = 6.2\ \mathrm{W} \quad P_{2,\mathrm{aux}} = 9.5\ \mathrm{W}. \tag{4}$$

Thus, the total losses P_t are calculated with

$$P_t = P_{1,\mathrm{aux}} + P_{\mathrm{S1,cond}} + P_{\mathrm{S1,sw}} + P_{\mathrm{L,cond}} + P_{\mathrm{L,core}} + P_{\mathrm{Tr,cond}} + P_{\mathrm{Tr,core}} + P_{\mathrm{S2,cond}} + P_{\mathrm{S2,sw}} + P_{2,\mathrm{aux}}. \tag{5}$$

In the most simple model, all required quantities (e.g., rms current values) are evaluated for a given input power P_{in} in order to already include the impact of the losses on these quantities. The efficiency $\eta = P_{\mathrm{out}}/P_{\mathrm{in}}$ is then calculated using the output power $P_{\mathrm{out}} = P_{\mathrm{in}} - P_t$. The result (Fig. 5, dotted lines) shows that a very poor match is obtained with this simple model. Main reasons are as follows.

1) The calculated converter quantities (e.g., rms switch currents) significantly deviate from measured values, since losses are completely neglected within the simple electrical DAB model [Fig. 2(b)].
2) Inaccurate calculation of the conduction losses lead to a wrong estimation of the dissipated power. This occurs mainly on the LV side, where high currents at high frequencies generate considerably more losses than predicted with (5).
3) Switching losses cause a large part of the total losses, and therefore, the switching losses need to be known in detail. It further turns out that, depending on the operating point, the switching action may change the transformer current considerably.

IV. Model Improvements

A. Improved Electrical DAB Model

A precise calculation of the inductor current i_{L} is considered to be most important for an accurate prediction of the DAB converter losses, since conduction losses and switching losses directly depend on $i_{\mathrm{L}}(t)$. Thus, the improved electrical DAB model includes the most important effects that influence i_{L}. Essentially, conduction losses modify the piecewise linear current waveform to a piecewise exponential waveform. In order to analyze the impact of the conduction losses on i_{L}, the different possible inductor current paths need to be examined.

Each DAB full bridge circuit resides in one of two states in order to generate a rectangular voltage with 50% duty cycle, e.g., possible values for $v_{\mathrm{T1}}(t)$ are

$$v_{\mathrm{T1}} = \begin{cases} +V_1, & \text{for state I: } \mathrm{T_1}, \mathrm{T_4} \text{ on; } \mathrm{T_2}, \mathrm{T_3} \text{ off} \\ -V_1, & \text{for state II: } \mathrm{T_2}, \mathrm{T_3} \text{ on; } \mathrm{T_1}, \mathrm{T_4} \text{ off} \end{cases} \tag{6}$$

(provided that the full bridges are ideal; failure modes—e.g., bridge leg short circuits—and dead-time intervals are not considered). Independent on the actual switching state of the full bridge circuits, the inductor current path always includes the resistors $2 \cdot R_{\mathrm{S1}}$, R_{L} and R_{Tr} on the HV side and $2 \cdot R_{\mathrm{S2}}$ as well as the PCB resistance values $R_{\mathrm{PCB,AC}}$ and $R_{\mathrm{PCB,DC}}$ [Fig. 2(a)] on the LV side

$$\begin{aligned} R_1 &= 2 \cdot R_{\mathrm{S1}} + R_{\mathrm{L}} + R_{\mathrm{Tr1}} = 281.5\ \mathrm{m\Omega} \\ n^2 \cdot R_2 &= n^2 \cdot (R_{\mathrm{Tr2}} + 2 \cdot R_{\mathrm{S2}} + R_{\mathrm{PCB,AC}} + R_{\mathrm{PCB,DC}}) \\ &= 838\ \mathrm{m\Omega} \end{aligned} \tag{7}$$

(R_{Tr1} denotes the ac resistance of the HV side transformer winding and R_{Tr2} considers the LV side transformer copper losses; in total $R_{\mathrm{Tr1}} + n^2 R_{\mathrm{Tr2}} = R_{\mathrm{Tr}}$).

TABLE III
IMPROVED DAB MODEL, COMPONENT VALUES

R_{S1}	R_L	R_{Tr1}	R_{Tr2}	R_{S2}	$R_{PCB,AC}$	$R_{PCB,DC}$
83mΩ	22.5mΩ	93mΩ	273μΩ	350μΩ	263μΩ	219μΩ

L_1	L_2	L_M
22.8μH	14nH	4.3mH

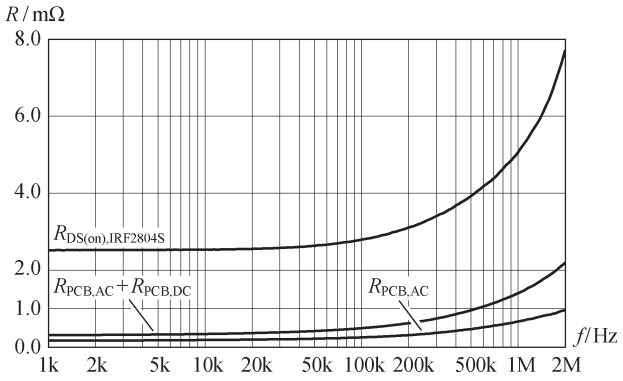

Fig. 6. Measured ac resistances for $R_{\mathrm{PCB,AC}}$, the sum $R_{\mathrm{PCB,DC}} + R_{\mathrm{PCB,AC}}$, and the on-state resistance of a single IRF2804S MOSFET with a gate to source voltage of 10 V. A 13 : 1 measurement transformer is employed in order to obtain reasonable impedance values for the measurement using the Agilent 4294A precision impedance analyzer. At 100 kHz, the calculated maximum error is ±13% for $R_{\mathrm{PCB,AC}}$, ±7% for $(R_{\mathrm{PCB,DC}} + R_{\mathrm{PCB,AC}})$, and ±3% for $R_{\mathrm{DS(on),IRF2804S}}$.

The DAB inductance is as well split up into the HV side inductance L_1 and the LV side inductance L_2 with $L_1 + n^2 L_2 = L$. Moreover, the improved electrical DAB model contains the magnetizing inductance L_M [Fig. 2(c)]. Core losses are not considered, since their influence on the transformer currents is negligible $(R_M \gg \omega L_M)$.

The improved electrical DAB model is parameterized with resistance and inductance values measured at f_S. The employed component values are listed in Table III.

B. Conduction Losses and High-Frequency Effects

The HV side MOSFET conduction losses are again calculated using the channel resistance of the selected MOSFET and the rms switch current, $P_{\mathrm{S1,cond}} = 4 \cdot R_{\mathrm{S1}} \cdot (I_{\mathrm{S1,RMS}})^2$. However, the calculations of the copper losses of the inductor, the transformer, and the PCB as well as the conduction losses of the LV side switches include current harmonics, since measurements confirm a significant impact of high-frequency effects on their resistance values (Fig. 6). For the calculated results the harmonic components up to $20 \cdot f_S$ are considered.

C. Accurate Switching Losses, HV Side

The switching losses of a single half-bridge [MOSFETs T_1 and T_2 in Fig. 7(a)] are measured on the final converter PCB in order to obtain accurate results. Since a significant amount of stored energy may be transferred from one switch to another during the switching process, the drain currents i_{D1} and i_{D2} as well as the blocking voltages v_{DS1} and v_{DS2} of the respective

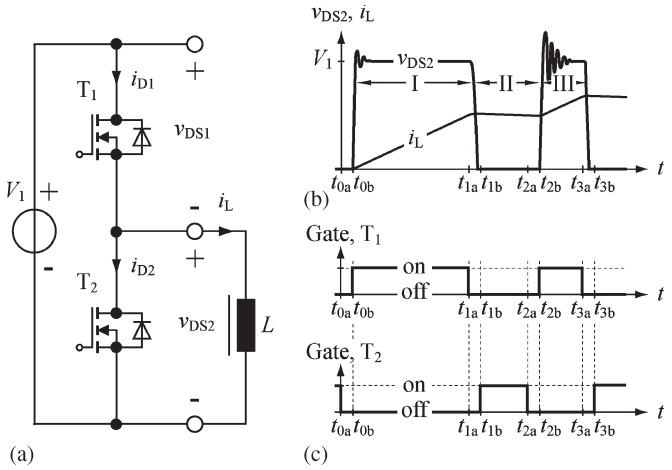

Fig. 7. (a) Switching loss measurement setup. (b) Employed double pulse signal. (c) Respective gate signals for T_1 and T_2.

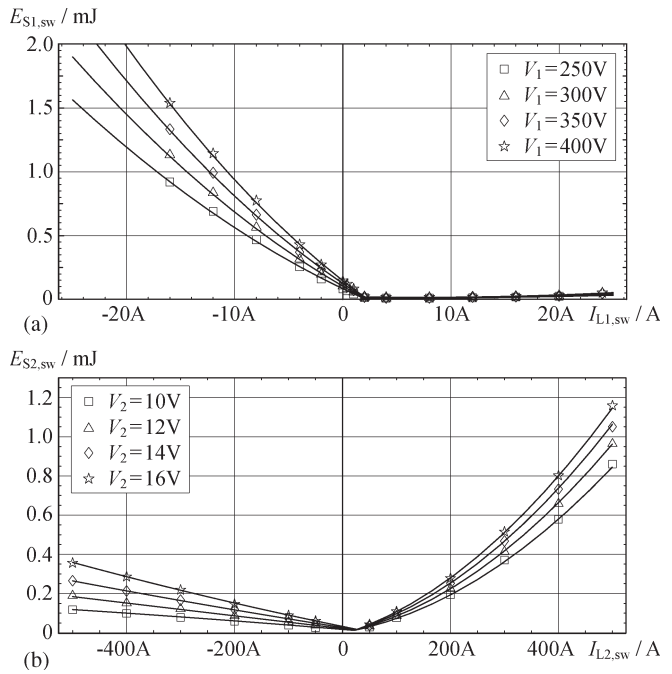

Fig. 8. Measured switching losses at $T_j = 25\ ^\circ\mathrm{C}$ for a single switching action. (a) HV side. (b) LV side. $I_{\mathrm{L1,sw}}$ and $I_{\mathrm{L2,sw}}$ indicate the instantaneous currents during switching. Negative currents $I_{\mathrm{L1,sw}}$ and $I_{\mathrm{L2,sw}}$ denote hard switching. For positive currents $I_{\mathrm{L1,sw}}$ and $I_{\mathrm{L2,sw}}$, the ZVS condition is satisfied.

half-bridge are measured simultaneously. The dissipated energy during switching is then calculated with

$$E_1 = \int_{t_1}^{t_2} v_{\mathrm{DS1}}(t) \cdot i_{\mathrm{D1}}(t) dt \quad E_2 = \int_{t_1}^{t_2} v_{\mathrm{DS2}}(t) \cdot i_{\mathrm{D2}}(t) dt \quad (8)$$

whereas t_1 denotes the beginning and t_2 the end of the switching process. For the measurement of the switching losses, a double pulse signal is used [Fig. 7(b)] with a first interval (I) where the desired output current $i_{\mathrm{L}}(t_{1\mathrm{a}})$ is generated, a second time interval (II) where the output current can freewheel through T_2, followed by another interval (III) with increasing

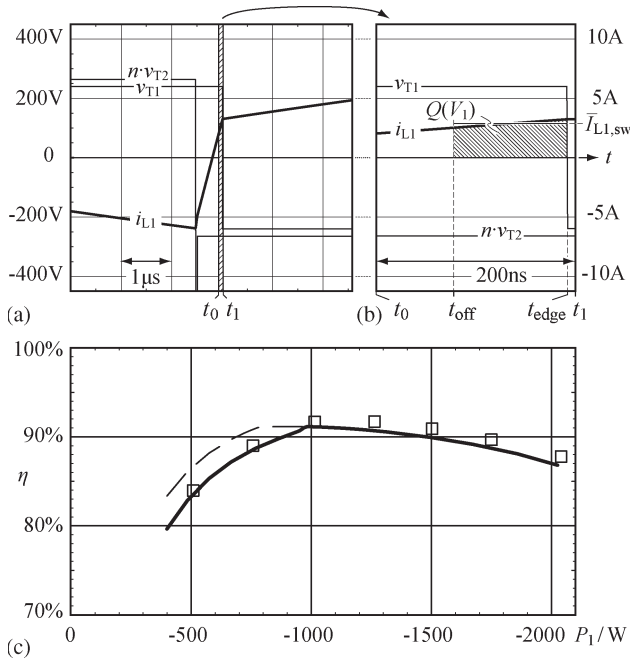

Fig. 9. Implemented HV side switch current estimation. (a) Calculated voltage and current waveforms for $V_1 = 240$ V, $V_2 = 11$ V, and $P_1 = -2$ kW (power is transferred from the LV side to the HV side). (b) Magnified time interval $t_0 < t < t_1$ depicts the turn-off process for an HV MOSFET with involved charge $Q(V_1)$ and the current $\bar{I}_{\mathrm{L1,sw}}$. The MOSFET gate is turned off at t_{off}, and the drain to source voltage changes at t_{edge}. (c) Achieved improvement of the efficiency prediction (solid line: calculation uses $\bar{I}_{\mathrm{L1,sw}}$, dashed line: $i_{\mathrm{L1}}(t_{\mathrm{edge}})$ is used to determine the HV switching losses).

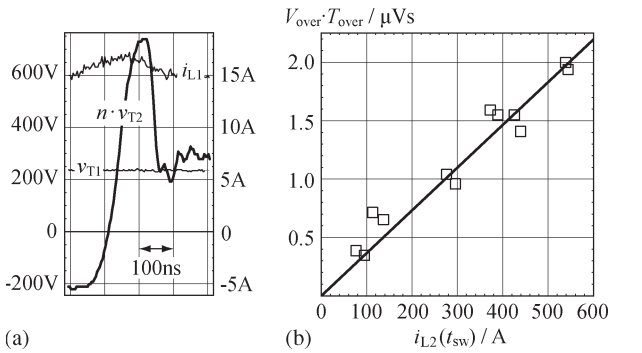

Fig. 10. (a) LV side overvoltage by reason of the parasitic MOSFET and PCB inductances (magnified detail of the measured waveforms for $V_1 = 240$ V, $V_2 = 11$ V, $P_2 = 2$ kW and power being transferred from the HV side to the LV side). (b) Measured voltage time areas (□) for different switching currents $i_{\mathrm{L2}}(t_{\mathrm{sw}})$ and phase shift modulation. The bold line denotes the approximated voltage time area $V_{\mathrm{over}} \cdot T_{\mathrm{over}} = 3.66$ nVs/A $\cdot\, i_{\mathrm{L2}}(t_{\mathrm{sw}})$. For all calculations, $V_{\mathrm{over}} = 20.4$ V is considered.

output current. In order to avoid a current shoot through in the half-bridge, a dead time $T_{\mathrm{deadtime}} = 200$ ns is used [Fig. 7(c)]. With the double pulse signal, the switching losses for ZVS and hard switching operation can both be measured, as the conditions for ZVS are fulfilled at time $t_{1\mathrm{a}}$ and hard switching occurs at $t_{2\mathrm{b}}$. In Fig. 8(a), the sum $E_1 + E_2$ is shown for a single switching process and for different switching currents $I_{\mathrm{L1,sw}}$ as well as different operating voltages V_1. Negative switching currents in Fig. 8(a) indicate hard switching operation of the half-bridge circuit where significant losses occur due to the slow MOSFET body diodes. For positive switching currents greater than 2 A, the circuit is successfully operated with ZVS giving very low switching losses. Low currents ($0\ \mathrm{A} \leq I_{\mathrm{L1,sw}} \leq 2\ \mathrm{A}$) are insufficient to recharge the parasitic drain to source capacitors within the dead-time interval, which leads to increased turn-on losses.

Depending on the switching current of the bridge, two different polynomial functions—one for hard switching and one for soft switching—are fitted to the switching losses using a least means squares approximation. However, the switching losses are measured with constant inductor current $i_{\mathrm{L}}(t)$ during the dead-time interval what may not be true in reality. Thus, wrong results are obtained for certain operating points, if the calculated current at the switching time is directly applied to the switching loss function [Fig. 9(c)]. In order to improve the results, the soft switching case and the hard switching case need to be looked at separately, due to essentially different switching processes.

For the soft switching case [$I_{\mathrm{L1,sw}} > 2$ A in Fig. 8(a)], the voltage v_{T1} changes within the dead-time interval, whereas a certain charge must be supplied in order to achieve ZVS [i.e., to charge and discharge the respective MOSFET junction capacitors, Fig. 9(a) and (b)]

$$Q(V_1) = \int_{t_{\mathrm{off}}}^{t_{\mathrm{edge}}} i_{\mathrm{L1}}(t)dt \tag{9}$$

(t_{off} denotes the MOSFET turn-off time and t_{edge} is the time when v_{T1} changes). The amount of charge depends on the employed power MOSFETs, e.g., $Q(V_1) \approx 220\ \mathrm{nC} + V_1 \cdot 218\ \mathrm{pF}$ for the SPW47N60CFD at room temperature (estimated using datasheet information). With known $Q(V_1)$, $i_{\mathrm{L1}}(t)$, and t_{edge}, the turn-off time t_{off} that is required in order to fully charge and discharge the MOSFET capacitors, can be calculated.[1]

For the hard switching case [$I_{\mathrm{L1,sw}} < 0$ in Fig. 8(a)], the voltage v_{T1} changes after the dead-time interval has elapsed. On the assumption of negligible turn-on and turn-off delays, the MOSFET turn-off time is determined with $t_{\mathrm{off}} = t_{\mathrm{edge}} - T_{\mathrm{deadtime}}$.

It finally turns out that the calculated switching losses become significantly more accurate if the switching loss function is evaluated using the average current during the time interval $t_{\mathrm{off}} < t < t_{\mathrm{edge}}$ [Fig. 9(c)]

$$\bar{I}_{\mathrm{L1,sw}} = \frac{\int_{t_{\mathrm{off}}}^{t_{\mathrm{edge}}} i_{\mathrm{L1}}(t)dt}{t_{\mathrm{edge}} - t_{\mathrm{off}}} \qquad P_{\mathrm{S1,sw}} = 4 f_{\mathrm{S}} \cdot E_{\mathrm{S1,sw}}(\bar{I}_{\mathrm{L1,sw}}). \tag{10}$$

D. Accurate Switching Losses, LV Side

The LV side switching losses are measured using one of the two input stages of the full converter with four MOSFETs

[1]Whenever $t_{\mathrm{off}} < t_{\mathrm{edge}} - T_{\mathrm{deadtime}}$ occurs, then the injected charge during the dead time interval is not sufficient to achieve soft switching [$0 < I_{\mathrm{L1,sw}} < 2$ A in Fig. 8(a)]; consequently, t_{off} needs to be limited to $t_{\mathrm{edge}} - T_{\mathrm{deadtime}}$.

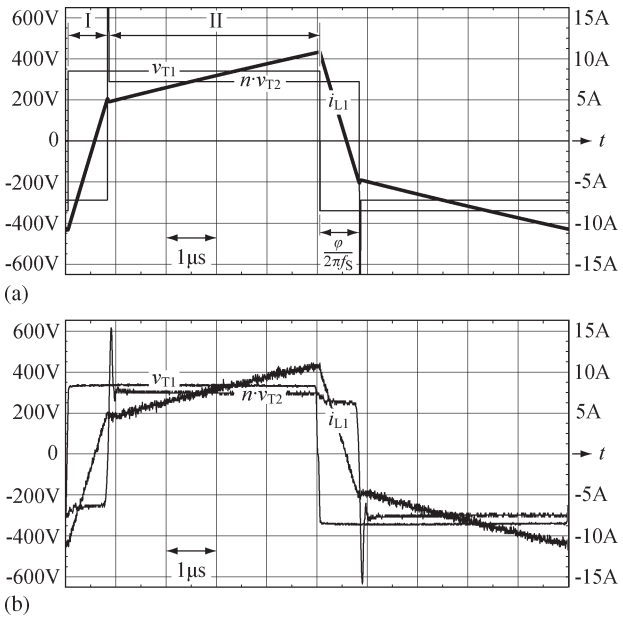

Fig. 11. (a) Calculated and (b) measured voltage and current waveforms for $V_1 = 340$ V, $V_2 = 12$ V, $P_2 = 2$ kW, and power being transferred from the HV port to the LV port. During time interval I, the transformer current $i_{\rm L}$ changes rapidly, while most energy is transferred during time interval II. The waveform $v_{\rm T2}(t)$ contains overvoltage switching spikes according to Section IV-D.

TABLE IV
DIFFERENCE BETWEEN CALCULATED AND MEASURED LOSSES

	Maximum relative difference	Maximum absolute difference	Average relative difference	Average absolute difference
Simple Model	61.9%	167W	41.3%	45.6W
Accurate conduction losses	59.7%	103W	28.4%	29.6W
Accurate conduction and switching losses	32.1%	91W	9.6%	11.4W
Full model (Figure 12)	22.8%	30W	8.0%	8.2W

being operated in parallel; again, the double pulse signal [cf., Fig. 7(b)] is employed with a dead time of 240 ns. For each of the MOSFETs, the drain currents and the drain to source voltages are measured simultaneously in order to calculate the respective switching losses. Fig. 8(b) presents the measured and scaled switching losses of the half-bridge for the fully equipped LV side with eight parallel MOSFETs per switch. There, hard switching operation occurs for $I_{\rm L2,sw} < 0$ and ZVS for $I_{\rm L2,sw} > 0$. Comparably low switching losses occur during hard switching, partly due to the small reverse recovery charge of the selected LV MOSFET. Moreover, the parasitic MOSFET lead inductances (approximately 15 nH per MOSFET) are large enough to enable zero current switching in the hard switching range when the applied voltage is sufficiently low (i.e., less than 20 V). For $I_{\rm L2,sw} > 0$, these lead inductances cause increasing losses as they store a significant amount of energy, which is dissipated once the MOSFETs turn off. Hence, a considerable voltage spike occurs on $v_{\rm T2}$ when the LV full bridge of the DAB is operated with ZVS (Fig. 10) and this, in turn, may significantly decrease $i_{\rm L2}(t)$. Analytical considerations show that the inductor current $i_{\rm L2}(t_{\rm sw})$ drops by a value $\Delta i_{\rm L2}$

$$\Delta i_{\rm L2} = 2 \cdot i_{\rm L2}(t_{\rm sw}) \cdot \frac{L_{\rm DS}}{L/n^2} \tag{11}$$

proportional to $i_{\rm L2}(t_{\rm sw})$ and independent on the actual supply voltages V_1 and V_2 ($t_{\rm sw}$ denotes the beginning of the switching process and the factor 2 in (11) is due to the phase shift modulation where both half-bridges switch simultaneously). Therefore, this effect can be accurately modeled using a rectangular overvoltage source with a constant magnitude $V_{\rm over} = 20.4$ V and a variable pulsewidth $T_{\rm over} = c \cdot i_{\rm L2}(t_{\rm sw})$, $c = 0.179$ ns/A, in series to $v_{\rm T2}$ after the LV side switches turn off (Fig. 10).

Similar to the HV side, two different polynomial functions are fitted to the measured switching losses. Again, the switching losses are measured using a constant inductor current $i_{\rm L}(t)$ during the dead-time interval. However, due to high currents and low voltages, the switching process either commences directly after turn off [$I_{\rm L2,sw} > 0$ in Fig. 8(b)] or directly after turn on ($I_{\rm L2,sw} < 0$) and thus the switching losses can be accurately evaluated using the instantaneous current $i_{\rm L2}(t_{\rm sw})$ at the time $t_{\rm sw}$ when $v_{\rm T2}$ changes.

E. Accurate Input and Output Power Calculation

So far, all quantities required to calculate the efficiency are determined at a certain input power (cf., Section III-D). However, input and output power which are calculated with the electrical DAB model (e.g., $P_{1,\rm model} = V_1 \cdot I_1$ is the input power if power is transferred from the HV port to the LV port, Fig. 2) may be inaccurate, since the losses considered within the DAB model may deviate significantly from the accurately calculated losses. Consequently, an inaccurate efficiency results; this can be observed in Fig. 5 with the diagram entitled "11 V $\rightarrow$ 240 V" where the calculation obviously fails.

A reference power level $P_{\rm ref}$ is introduced in order to achieve a more accurate calculation of input and output power levels. $P_{\rm ref}$ is calculated based on the HV port DAB power $P_{1,\rm model} = V_1 \cdot I_1$ and the HV side conduction losses using (7)[2]

$$P_{\rm ref} = P_{1,\rm model} - R_1 \cdot I^2_{\rm L1,RMS}. \tag{12}$$

The HV port power P_1 and the LV port power P_2 are then obtained according to

$$\begin{aligned} P_1 &= P_{\rm ref} + (P_{1,\rm aux} + P_{\rm S1,cond} + P_{\rm S1,sw} + P_{\rm L,cond} \\ &\qquad + P_{\rm L,core} + P_{\rm Tr1,cond} + P_{\rm Tr,core}/2) \\ P_2 &= P_{\rm ref} - (P_{\rm Tr,core}/2 + P_{\rm Tr2,cond} + P_{\rm S2,cond} \\ &\qquad + P_{\rm S2,sw} + P_{2,\rm aux}) \end{aligned} \tag{13}$$

whereas evenly shared transformer core losses between LV side and HV side are assumed.

[2] $P_{\rm ref}$ could as well be calculated using $P_{2,\rm model} = V_2 \cdot I_2$. However, overvoltage switching transients are regarded on the LV side and therefore $P_{2,\rm model}$ partly contains switching losses; it is thus more intuitive to use $P_{1,\rm model}$ for the shown calculation.

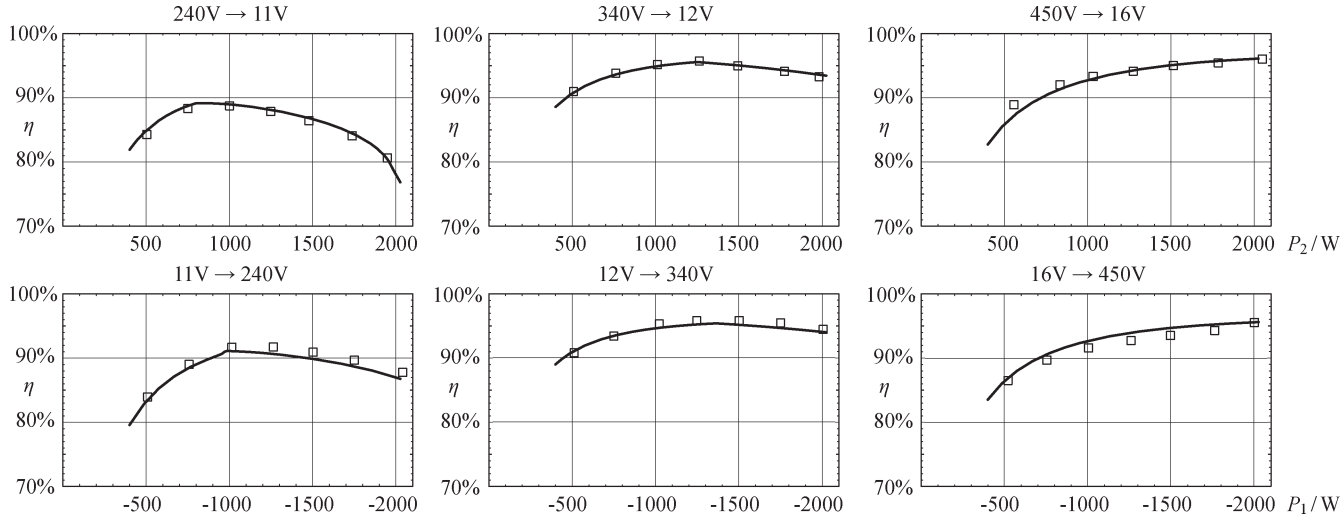

Fig. 12. (Solid lines) Predicted efficiencies and (□) measured efficiencies for different operating conditions. The efficiencies are calculated with the improved DAB loss model which includes all methods discussed in Section IV.

V. Discussion

A numerical solver calculates the transformer currents $i_{\mathrm{L1}}(t)$ and $i_{\mathrm{L2}}(t)$ in steady state operation using piecewise constant transformer voltages $v_{\mathrm{T1}}(t)$ and $v_{\mathrm{T2}}(t)$. Excellent matching to measured current waveforms are achieved (Fig. 11). The resulting rms currents, harmonic components, and instantaneous current values are applied to the methods discussed in Section IV; evidently, the efficiency gradually improves with increasing level of detail (Fig. 5). Table IV summarizes the achieved refinements of the predicted losses P_t that are compared to the measured losses $P_{t,\mathrm{meas}}$ (the absolute differences in Table IV are equal to $|P_t - P_{t,\mathrm{meas}}|$, the relative differences are calculated with $|P_t - P_{t,\mathrm{meas}}|/P_{t,\mathrm{meas}}$). In particular, the accurate considerations of conduction losses—including high-frequency effects—and switching losses result in a major improvement and reduce the relative error from 41.3% to 9.6% in average. With the full model, an average relative error of 8.0% is achieved.

In Fig. 12, the measured efficiency is compared to the calculated efficiency for different operating points. Very good agreement between the results obtained from the theoretical model and the experimental values is observed. Fig. 12 as well shows the strong dependence of the efficiency on the operating point. Interestingly, the efficiency as well depends on the direction of power transfer, even though the DAB topology shows a symmetric structure. The main reason for this difference is the transformer current reduction due to LV side switching according to (11). For power being transferred to the LV port (mode A), this current reduction occurs at the beginning of the main energy transfer interval (interval II in Fig. 11) and consequently reduces the amount of transferred power. Thus, the phase angle $\varphi = \varphi_A$ must be increased in order to obtain the required output power $P_{2\mathrm{A}}$. For power being transferred to the HV port (mode B), the current reduction due to LV side switching occurs at the end of the main energy transfer interval. Hence, a lower phase angle $|\varphi_B| < |\varphi_A|$ is attained for the same output power level $|P_{1\mathrm{B}}| = P_{2\mathrm{A}}$ which results in less circulating currents and lower switching losses.

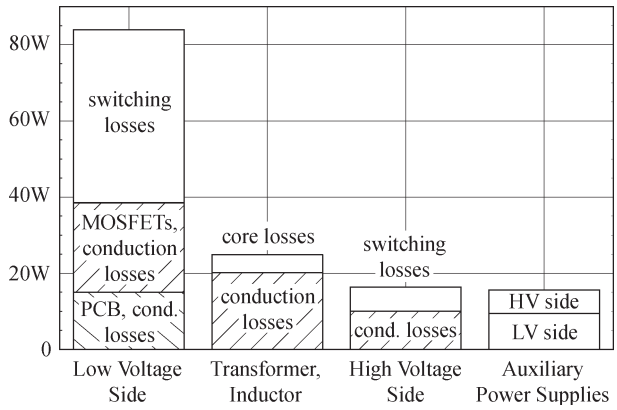

Fig. 13. Calculated distribution of the power losses for operation at $V_1 = 340$ V, $V_2 = 12$ V, and $P_2 = 2$ kW.

The presented loss model facilitates the prediction of the power loss distribution in the converter as well as the ability to calculate the temperature rise in each power component. In Fig. 13, the losses for nominal operation are presented for the PCB, the LV and HV side MOSFETs, the transformer, the inductor, and the auxiliary power supplies that provide the gate driver power. The largest losses of 69 W occur for the LV side MOSFETs; however, a temperature rise of approximately 1 °C is expected since each switch comprises of eight parallel connected MOSFETs (thermal resistance R_{jh} of junction to heat sink is 0.45 K/W for each MOSFET, equal power distribution among all 32 switches is assumed). Low losses of 16 W occur on the HV side and a temperature rise of less than 2 °C is calculated at the semiconductor junction using a $R_{\mathrm{jh}} = 0.3$ K/W for each MOSFET. The temperature rise is low since both bridges are overrated in terms of current in order to meet the efficiency requirements. The transformer has 25 W of losses, so active cooling is required for reliable operation. Using double-sided water cooling, a temperature rise of 50 °C is expected at the innermost winding. However, the presented loss model does not include the effect of the temperature rise on the efficiency. Thus, besides the discussed electrical model,

a thermal converter model needs to be implemented which contains accurate information on the temperature dependence of the losses in order to precisely calculate the expected component temperatures [16], [17].

For nominal operation of the DAB, high efficiency of more than 90% is achieved. The efficiency decreases for operating points that diverge significantly from the nominal operating point. The main reasons for the additional power loss arise from the conduction losses due to circulating transformer currents and increased switching losses on the LV side. A considerable improvement of the converter performance is achieved with optimized modulation methods where circulating transformer currents and switching losses are reduced [12], [24].

The development of the loss model has shown that the critical parts of the converter are the resistive losses on the LV side as well as switching losses. Accordingly, the losses on the LV side are significantly higher than on the HV side (about five times higher in Fig. 13), even though the LV side contains eight switches in parallel and occupies twice the volume of the HV side.

Therefore, the following issues must be considered carefully in the design of a LV and high-current converter to achieve high efficiency.

1) Circulating transformer currents should be as small as possible.
2) The impact of high-frequency skin and proximity effects must be considered (transformer and PCB).
3) Low voltage side switching should occur at low currents.

One important aspect is the layout of the LV side PCB in order to achieve good current distribution in the PCB and between the parallel connected MOSFETs. The transformer terminal of the LV side full bridge needs also to be designed carefully due to high-frequency losses. A model with calculated resistance and switching loss values can be used in a first step to design the system and can be refined with measurement results from a prototype.

VI. Conclusion

An accurate power loss model for a bidirectional dc–dc converter with a high-current/LV port was developed. It shows that switching losses and the LV side conduction losses are most critical for the design of the converter. Calculated results were compared to measurements obtained from a 2-kW experimental system in order to verify the loss model. Based on this model the expected converter efficiency as well as the distribution of the power losses in the converter are calculated. This enables the evaluation of the temperature rise for each power component in order to identify the most heavily loaded components. For the given prototype, it is found that a high-temperature rise occurs in the transformer winding. An improved transformer construction is necessary to overcome excessive power dissipation. Conversely, the dissipated heat in the power MOSFETs causes only a small temperature rise. Thus, the MOSFET current rating could be reduced to lower converter cost without significantly lowering converter reliability.

Even though the discussions focus is on a high-current DAB, the general nature of the presented methods enables an accurate prediction of the power losses of other dc–dc converter topologies operated at high switching frequencies; the presented approach is particularly suitable for power converters that exhibit large current ripples. The method could thus be applied to automotive power converters with high power density [25] or resonant dc–dc converters with one or more high-current ports.[3]

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Florian Krismer (S'05) received the M.Sc. degree (with honors) from the University of Technology Vienna, Vienna, Austria, in 2004. He is currently working toward the Ph.D. degree in the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology Zürich, Zürich, Switzerland.

His research interests include the analysis, design, and optimization of high-current and high-frequency power converters.

Johann W. Kolar (S'89–M'91–SM'04) received the Ph.D. degree (*summa cum laude*) in industrial electronics from the University of Technology Vienna, Vienna, Austria.

From 1984 to 2001, he was with the University of Technology Vienna, where he was teaching and working in research in close collaboration with industry in the fields of high-performance drives, high-frequency inverter systems for process technology, and uninterruptible power supplies. Since 2001, he has been a Professor and Head of the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology Zürich, Zürich, Switzerland. The focus of his current research is on novel ac–ac and ac–dc converter topologies with low effects on the mains for telecommunication systems, More-Electric-Aircraft applications, and distributed power systems utilizing fuel cells. A further main area of research is the realization of ultracompact intelligent converter modules employing the latest power semiconductor technology (SiC) and novel concepts for cooling and electromagnetic interference filtering. He has authored or coauthored over 150 scientific papers in international journals and conference proceedings and has filed more than 50 patents.

Dr. Kolar is a member of the Institute of Electrical Engineers of Japan and of the Technical Program Committees of numerous international conferences (e.g., Director of the Power Quality branch of the International Conference on Power Conversion and Intelligent Motion). From 1997 to 2000, he served as an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and, since 2001, as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS.