

# An Optimized, 99% Efficient, 5 kW, Phase-Shift PWM DC-DC Converter for Data Centers and Telecom Applications

U. Badstuebner, J. Biela, and J.W. Kolar

Power Electronic Systems Laboratory, ETH Zurich  
Physikstrasse 3, 8092 Zurich, Switzerland

Email: badstuebner@lem.ee.ethz.ch; www.pes.ee.ethz.ch

**Abstract**—The development of new power supply systems is increasingly focused on higher efficiency, while the power density should remain on a high level. This is especially true for data center and telecom application Power Supply Units (PSU).

The commonly-used DC-DC converter in telecom and data center PSU's are full-bridge phase-shift PWM converter, which enables a high power and highly efficient conversion, compact design and simple control due to constant switching frequency.

The component dimensioning of the converter system has many degrees of freedom, as the design parameters are interdependent from each other to some extent. An automatic optimization procedure based on comprehensive analytical models leads to the optimal design parameters, such as switching frequency and geometry of the magnetic components.

In this paper, the development, optimization and design process for an efficiency-optimized 5 kW, 400 V to 48..54 V phase-shift PWM DC-DC converter with LC-output filter and synchronous rectification is presented. The proposed optimization algorithm, which considers the part-load-efficiency as well, results directly in the component values for the realized prototype. The design of the converter is explained in detail and measurement results are presented and discussed.

**Index Terms**—Phase-shift PWM DC-DC converter, optimization, design process, high efficiency, synchronous rectifier

## I. INTRODUCTION

In recent decades, power electronic research focused mainly on maximizing the power density of PWM converter systems. This has roughly doubled every 10 years since 1970 [1]. Above all, this was enabled by the continuous improvements of power semiconductor devices, which allow higher switching frequency and thereby to decrease the volume of magnetic components [2]. Especially in the area of Power Supply Units (PSU) for data center and telecom applications, the development of high power density converter systems was of great significance, as the Capital Expenditure (CapEx) was measured by the square footage occupied, rather than power consumption [3]. The demand for data centers is continuously increasing and rising energy prices have resulted in the cost of power and cooling exceeding the purchase cost in less than two years [3]. This has caused a change of the driving force in power converter system development towards highly efficient power conversion, although high power density is still required. Additional design constraints such as cost, weight and reliability have resulted in multi-objective targets for the system development [4].

In [5] a power density optimized, 5 kW, 400 V to 48..54 V phase-shift PWM DC-DC converter for data center and telecom application (cf. table I) is presented. There, the

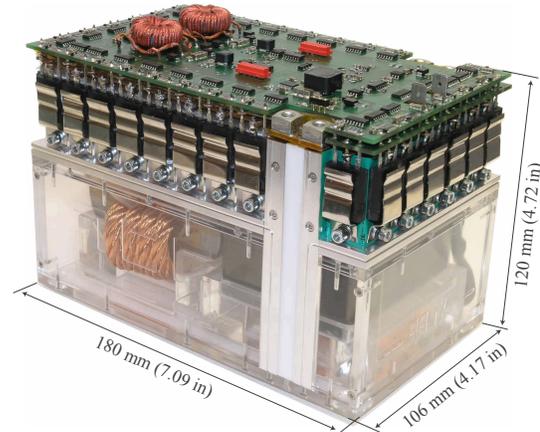


Figure 1. Realized highly efficient DC-DC converter prototype. 400 Vdc to 48..54 Vdc, 5 kW, Efficiency  $\eta \geq 99\%$  over a wide load range, power density  $\rho = 38 \text{ W/in}^3$  (2.3 kW/liter).

optimization-procedure-based design process results in a prototype with a power density  $\rho = 9 \text{ kW/liter}$  ( $147 \text{ W/in}^3$ ) and the measured efficiency  $\eta = 94.75\%$ . This design leads to the point of highest power density in the power-density - efficiency plane ( $\rho - \eta$  - plane) and presents a pareto-optimal point, as explained in [4], [6].

In this paper, the design process of an efficiency-optimized DC-DC converter with LC-output filter (cf. Fig. 2) and similar specifications (cf. table I) is explained, which presents the "pareto"-optimal point of highest power density in the  $\rho - \eta$  - plane.

The optimization procedure applied, which is based on comprehensive analytical models of the converter system with simultaneous consideration of the part-load efficiency, is targeted at an efficiency  $\eta \geq 99\%$ . The optimization procedure is explained in **Section II** and the analytical models are summarized, whose derivation is presented in [7]. The optimization results are presented and discussed in **Section III**. The main focus in this paper lays on the prototype

Table I  
SPECIFICATIONS FOR THE PROTOTYPE DC-DC CONVERTER.

Input voltage	$V_{in}$	400 V
Output voltage	$V_{out}$	48..54 V
Output power	$P_{out}$	5 kW
Output ripple voltage	$V_{ripple}$	300 mV <sub>pp</sub>

realized as presented in Fig. 1, with a power density  $\rho = 2.3 \text{ kW/liter}$  ( $38 \text{ W/in}^3$ ) and a calculated efficiency  $\eta \geq 99\%$  over a wide load range as presented in detail in **Section IV**. There, measurement results with the assembled prototype are presented and discussed based on comparison with theoretical and simulation results.

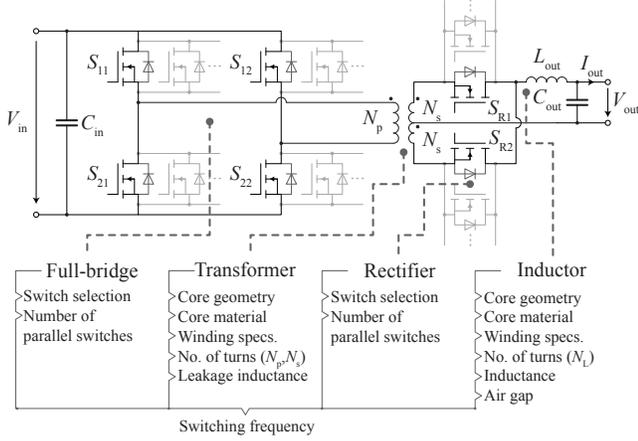


Figure 2. Schematic of the phase-shift PWM converter with LC-output filter for 99% efficiency,  $V_{in} = 400 \text{ V}$ ,  $V_{out} = 48..54 \text{ V}$ ,  $P_{out} = 5 \text{ kW}$ . The free design-parameter are illustrated. All four components with the presented free parameters are additionally dependent on the switching frequency.

## II. EFFICIENCY OPTIMIZATION PROCEDURE

The design of the converter system has many degrees of freedom, even though standard topologies are applied. The proposed topology for the highly efficient DC-DC converter in Fig. 2 consists of a full-bridge on the high-voltage side, a center-tapped transformer, two synchronous rectifier switches and LC-output filter. The major design parameters, which have to be established during the development process, are illustrated in Fig. 2, beneath the schematic of the converter. As these design parameters are interdependent to some extent from each other, the entire system rather than a single component must be optimized. The geometry of the inductor, for instance, defines the inductance and thus the current ripple, thereby influencing not only losses in the inductor windings and core but also the losses in the output capacitor, full-bridge switches, synchronous rectifier and transformer. An automatic optimization procedure considering the entire converter system is applied as the solution for this challenging design process. The optimization procedure and the integration of the part-load efficiency are explained below. The underlying comprehensive analytical converter models are described shortly. The formulas and derivations are omitted in this paper for the sake of brevity, and referenced to the respective literature.

In Fig. 3 the proposed efficiency optimization procedure is depicted. At the top of the procedure or at the beginning of the design process, respectively, the fixed parameters have to be defined, i.e. electrical specifications and magnetic constraints. In order to reduce the calculation time, the core materials and switches (MOSFETs are applied here) have been preselected

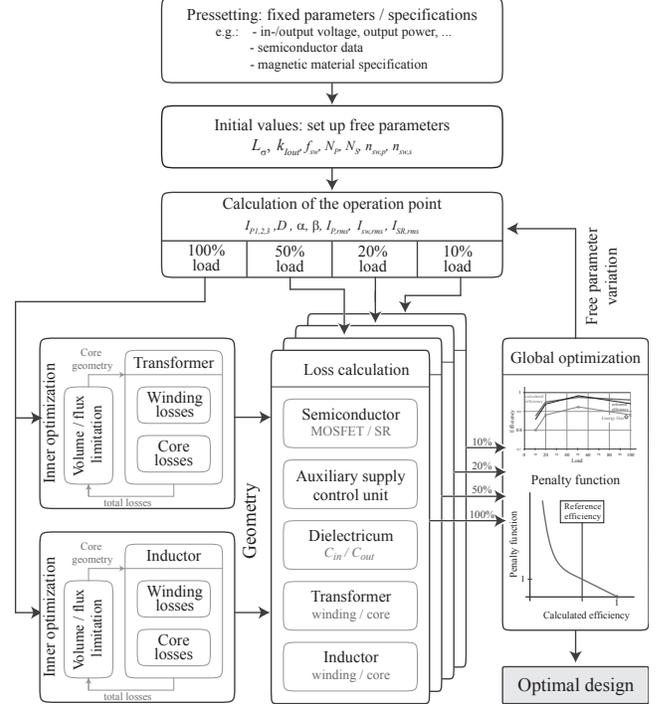


Figure 3. Automatic efficiency optimization procedure for the phase-Shift PWM DC-DC converter considering also part load efficiency according to Energy Star® [8].

Table II  
FIXED PARAMETERS FOR THE PROPOSED OPTIMIZATION PROCEDURE:  
ELECTRICAL SPECIFICATIONS, APPLIED MATERIALS AND SEMICONDUCTOR.

Input	Voltage $V_{in}$	400 V
Output	Voltage $V_{out}$	48 V..54 V
	Power $P_{out}$	5 kW
Transformer	Core material	N87
	Max. volume	0.3 liter
Inductor	Core material	Metglas® 2605SA1
	Max. volume	0.3 liter
MOSFETs	Full bridge	ST STY112N65M5
	Sync. rectifier	IR IRF4668PbF
Control	Gate driver	IXYS IXDD414
	Digital control	TI TMS320F2808

in preliminary considerations, i.e. a first optimization run identifies an optimal operation point and after that, the parameters of several switches have been applied in the optimization algorithm and based on the results, the best configuration has been chosen.

The most important fixed parameters (applied components, materials and specifications) are listed in table II.

The optimization algorithm is launched for the first time with the initial set of the free parameters, which are:

- The switching frequency  $f_{sw}$
- The primary and secondary turn numbers of the transformer  $N_p$  and  $N_s$
- The leakage inductance  $L_\sigma$

- The output inductor current ripple  $k_{I_{out}}$
- The number of parallel primary  $n_{sw,p}$  and synchronous rectifier MOSFET's  $n_{sw,s}$ .

Only integer values are considered for the number of turns ( $N_p$  and  $N_s$ ) and the number of parallel full-bridge and rectifier switches ( $n_{sw,p}$  and  $n_{sw,s}$ ). This is both practical and drastically reduces the calculation time. Further reduction of computation time is achieved by preselecting the switching frequency points 16 kHz, 25 kHz, 37.5 kHz, 50 kHz, 100 kHz and 200 kHz. The minimum switching frequency is selected right above the audible frequency and more frequency points have been selected between 16 kHz and 50 kHz, as the optimum switching frequency is supposed in that range.

The remaining free parameters, whose values can be arbitrary in a certain range, are the leakage inductance  $L_\sigma$  of the transformer and the permissible output current ripple factor  $k_{I_{out}}$  which determines the output inductance value  $L_{out}$ . The optimization loop is launched with these two parameters.

The first step in the loop is the calculation of the operation point, i.e. the determination of all relevant current and voltage waveforms. The required output inductance  $L_{out}$  and the capacitance  $C_{out}$  are calculated under full load conditions for the given specifications (cf. table I) and the free parameter  $k_{I_{out}}$ . The derivation of the current waveform by means of a coupled inductance model for the center-tapped transformer is described in detail in [7]. The determination of current and voltage waveforms and their respective rms-/average values and harmonics is the basis for the following loss calculations.

In the next step, the geometry of the inductor and transformer core is determined in two inner optimization procedures, where the geometry for the transformer E-Cores and the inductor C-Cores with foil windings are changed systematically, until the minimal full-load losses are found while the flux density  $B$  is kept below the respective limit (transformer:  $B_{max} = 300$  mT, material N87; inductor:  $B_{max} = 1.2$  T, material Metglas<sup>®</sup> 2605SA1). The volume of the magnetic components must also be limited, as the efficiency-optimum is continuously increasing for unbounded volumes as presented in [7].

The losses in the magnetic components are core and winding losses, considering the high frequency losses, as well. The optimal foil thickness of the windings is calculated based on a one-dimensional approach as presented in [9]. As the current ripple in the output inductor is small compared to the DC-current, the foil thickness would result in large values and thus, the thickness of the inductor foil winding is limited to 300  $\mu$ m, which is practical to realize.

The core losses are determined by the Steinmetz parameter for the applied core material with the extended Steinmetz formula due to the non-sinusoidal current waveform, as explained in [10]. The approach given in [11] is applied to calculate the HF-losses in the windings, considering the skin and proximity effect. The HF-winding losses in the inductor only have minor influence due to the small AC-component.

After the geometry parameters of the transformer and inductor are determined (resulting in the minimum losses), the loss calculation continues in the outer optimization loop. The

losses in the converter system are considered at four load-points, as proposed by the Energy Star<sup>®</sup> requirements for computer servers [8]: 10 %, 20 %, 50 % and 100 % of full load. The losses in the transformer and inductor are already determined for full load operation in the inner optimization loops. In addition to that, the following losses are considered and calculated for each of the four load levels:

- Transformer losses
  - Core losses
  - Winding losses (incl. HF-losses)
- Inductor losses
  - Core losses
  - Winding losses
- Full-bridge losses
  - Conduction losses
  - Switching losses
  - Gate drive losses
- Synchronous rectifier losses
  - Conduction losses
  - (Recovery losses)
  - Gate drive losses
- Auxiliary supply and control losses
- Dielectric losses in the output capacitor

The losses in the magnetic components, which have a major impact on the total losses, are determined as described above. The second major loss contributors are losses in power semiconductor, i.e. the full-bridge MOSFETs and synchronous rectifier MOSFETs. There, the number of parallel connected switches, which varies during the optimization process, has a significant influence.

The full-bridge losses are derived with the  $R_{DS,on}$ , the gate charge  $Q_G$ , the energy equivalent output capacitance  $C_{oss,eq}$  at  $V_{DC} = 400$  V and the energy in the output capacitance  $E(V)$  as function of the applied voltage for the preselected MOSFET. As the converter topology offers Zero Voltage Switching (ZVS) by inserting an interlock delay between the switching states, switching losses are, in principle, almost zero. However, especially at part load conditions, the load current and/or interlock delay might be insufficient for a complete resonant discharge of the MOSFETs in one bridge leg, i.e. a residual voltage  $V_{res}$  remains, which has to be discharged by the MOSFET. The residual voltage is calculated based on a RLC-resonant circuit consisting of the leakage inductance  $L_\sigma$ , the energy equivalent output capacitance  $C_{oss,eq}$  and the  $R_{DS,on}$  of the parallel connected MOSFETs. The switching losses  $P_{sw}$  of one bridge leg can be determined with the characteristic energy curve of the MOSFET used, which is described by piecewise polynomial function dependent on the applied residual voltage. In addition to the switching losses, conduction losses and gate drive losses are added in order to calculate the total semiconductor losses, as presented in [7].

Conduction and gate drive losses in the synchronous rectifier switches are calculated in the same manner as for the full bridge switches. As the rectifiers MOSFETs are turned-on during the free-wheeling phase, when the transformer voltage

and thus the voltage over the rectifier is clamped to approx. zero by the primary switches, the turn on losses are negligible. Switching losses will occur during the turn-off phase of the rectifier; as the current is commutated in the body diode then the input voltage is reapplied to the transformer after the free-wheeling phase. However, recovery losses in the body diode are largely dependent on the later assembly and thus the losses cannot be calculated with reasonable accuracy. In a first run, the turn-off losses in the diodes are set to zero with the assumption, that loss-reducing measures will be applied as will be discussed in section IV.

Especially at light-load conditions, the small but almost constant losses in the auxiliary supply and control electronics influence the efficiency. The predicted losses in control electronic and the dielectric losses in the output capacitor are thus considered in the total losses of the converter system as well.

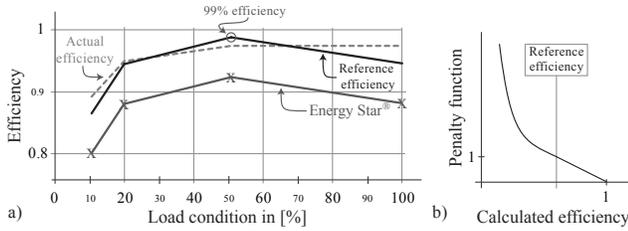


Figure 4. a) Proposed part load efficiency for computer servers (Energy Star® [8]), optimization reference efficiency and example efficiency curve calculated in the optimization procedure. b) Penalty function for calculating the optimization criteria.

At the end of one pass through the optimization loop, the optimization criterion is calculated. The proposed Energy Star® efficiency curve for computer servers in [8] is depicted in Fig. 4 a). The goal of the converter is a maximum efficiency of  $\eta \geq 99\%$  at 50% load, i.e. the Energy Star® efficiency curve is shifted to this level, as depicted in Fig. 4 a). The efficiency actually calculated for the four load points are now compared with the reference efficiency curve and are evaluated with a penalty function (cf. Fig. 4 b)):

$$penalty(\Delta\eta) = \begin{cases} \frac{1}{1 - \eta_{ref}} \cdot (1 - \eta_{act}), & \text{for } \Delta\eta < 0 \\ \frac{1}{(1 - \eta_{ref} + \eta_{act})^{20}}, & \text{for } \Delta\eta \geq 0, \end{cases} \quad (1)$$

which is linearly decreasing for deviations  $\Delta\eta$  smaller than 1, a polynomial increasing function for deviations  $\Delta\eta$  higher than 1 and result in 1, if the actual and reference values are equal. The sum of the penalty values result in the optimization criterion. The global optimization algorithm changes the free converter parameters systematically, until the minimum optimization criterion is found. The outputs of the optimization procedure are the design parameters of the converter which directly enables a prototype assembly.

### III. OPTIMIZATION RESULTS

In this section, the results based on the optimization procedure explained in the last section, are presented and discussed.

Table III

FREE PARAMETER OPTIMIZATION RESULTS WITH A VOLUME LIMIT OF  $18.3 \text{ in}^3$  (0.3 LITER). ( $f_{sw}$  = SWITCHING FREQUENCY,  $N_P / N_S / N_L$  = PRIMARY / SECONDARY / OUTPUT INDUCTOR TURNS NUMBER,  $L_\sigma$  = TRANSFORMER LEAKAGE INDUCTANCE,  $L_{out}$  = OUTPUT INDUCTANCE).

$f_{sw}$	$N_P$	$N_S$	$N_L$	$n_{sw,P}$	$n_{sw,S}$	$L_\sigma$ [ $\mu\text{F}$ ]	$L_{out}$ [ $\mu\text{F}$ ]
16.0 kHz	22	3	5	2	12	2.0	48.8
<b>25.0 kHz</b>	<b>22</b>	<b>3</b>	<b>4</b>	<b>2</b>	<b>11</b>	<b>1.8</b>	<b>43.0</b>
37.5 kHz	15	2	3	2	9	1.0	34.6
50.0 kHz	15	2	3	1	8	1.3	34.0
100.0 kHz	15	2	2	1	6	1.8	23.1
200.0 kHz	7	1	2	1	4	1.8	1.8

As starting point of the procedure, the fixed parameters in table II have been set. As the maximum allowed volume for both magnetic components, transformer and inductor,  $V_{max} = 0.3 \text{ liter}$  ( $18.3 \text{ in}^3$ ) was chosen as limit, because the losses in the magnetic components show only a small decrease upon this level for the maximum allowed volume, as presented in [7].

Furthermore, the MOSFETs for the full-bridge and synchronous rectifier have been preselected based on the optimization results for a fixed operation point. The best results for the full-bridge switches could be achieved with the parameters of the STY112N65M5 from STMicroelectronics [12]. The IRF4668PbF from International Rectifier [13], which allow minimal losses, was selected as MOSFETs for the synchronous rectifier.

The optimization results of the remaining free design parameters are presented in table III. The minimum of the optimization criterion, as defined in section II, is achieved at a switching frequency  $f_{sw} = 25 \text{ kHz}$ . Due to the flux density limitation, the number of turns in the magnetic components is higher for lower switching frequency. The output inductance is higher for lower switching frequency which results in smaller winding turns, as well, while the current ripple is almost constant. As illustrated in Fig. 5, where the component power losses are shown as function of the switching frequency, at higher switching frequencies, the number of parallel full-bridge switches  $n_{sw,p}$  decreases because the switching losses increase with the switching frequency, due to not completely dis-/charge of the drain-source capacitor especially at low-load condition. In addition, the number of parallel full-bridge and synchronous rectifier MOSFETs  $n_{sw,p}$  and  $n_{sw,s}$  are decreasing at higher switching frequencies because of the frequency-dependent gate drive losses. The smaller number of parallel MOSFETs results in higher conduction losses. The bend in the total losses curve after 37.5 kHz is mainly caused by this effect, as the number of parallel switches in the full bridge change from two to one.

The most significant impact in the decrease of the total power losses with increasing switching frequency are the losses in the synchronous rectifier, which are due to the continuously decrease of parallel switching devices (cf. table III).

As the synchronous rectifier MOSFETs operate at ZVS at

turn on and recovery losses are neglected in the first step, switching losses do not force the optimization procedure to reduce the number of parallel switches. The decrease is caused by the increasing gate-driver losses with higher switching frequencies, which lead to a significant efficiency drop at lower load-conditions. That is why the number of synchronous rectifier switches is reduced by the optimization algorithm. However, this leads to higher conduction losses at full load. The number of parallel switches would decrease even more at higher switching frequencies with the consideration of switching losses.

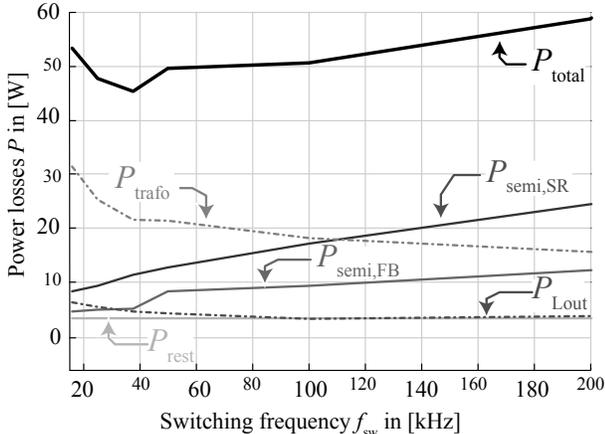


Figure 5. Losses of the optimized Phase-Shift PWM converter as a function of frequency. ( $P_{total}$  = total losses,  $P_{semi,FB}$  = full-bridge semiconductor losses,  $P_{semi,SR}$  = synchronous rectifier losses,  $P_{trafo}$  = transformer losses,  $P_{Lout}$  = output inductor losses,  $P_{rest}$  = losses in aux. supply, control unit, output capacitors).

The total losses in Fig. 5 at lower frequency range are determined mainly by the magnetic components due to the volume limitation. In addition, the minimum number of turns rises due to the flux density limitation, which leads to higher winding losses. Due to the decreasing turn numbers and smaller required cross section areas for higher switching frequencies, losses in the magnetic components also decrease. The winding losses, due to proximity and skin effect, as well as core losses increase again for frequencies higher than 200 kHz.

The losses for the output inductor are mainly caused by conduction losses, which decrease for higher frequencies due to the decreasing turn number. However, for higher switching frequencies, HF-winding losses and core losses increase, as for the transformer.

The remaining losses (control unit, auxiliary supply, output capacitors) stay approx. constant over the entire frequency range.

#### IV. PROTOTYPE

In this section the construction of a prototype assembly is shown in the first part, followed by the presentation of measurement results. The measurement results are discussed and compared with the calculation results. An improved switching strategy for the synchronous rectifier MOSFETs, leading to greater efficiency, is introduced.

#### A. Converter Assembly

Standard components, currently available on the market, were considered for the construction of the converter prototype. The resulting optimized core geometry of the transformer can be realized approximately by paralleling two EPCOS E70/33/32 core-sets [14]. The resulting inductor core cross section area is close to the Metglas® AMCC 320 core [15], whereas the legs of this C-core must be cut due to the oversized winding window width of the commercial core.

Copper foils have been considered in the optimization procedure for the windings and the optimal thickness has been calculated. In order to utilize the winding window of the standard cores mentioned above better, litz wires have been used instead of foil windings (details are presented in table IV). Litz wires are applied, although the minimal winding losses as calculated in the optimization procedure could not be reached, as the required foil winding were not available.

Table IV  
SUMMARY OF THE APPLIED COMPONENTS IN THE PROTOTYPE.

Transformer	Core (2 sets in parallel)	EPCOS E70/33/32
	Primary winding turns	22
	Primary winding litz wire	175x0.2 mm
	Secondary winding turns	3
Inductor	Secondary winding litz wire	600x0.2 mm
	Core (cut legs)	Metglas® AMCC320
	Inductance	43.6 $\mu$ H
	Air gap	519 $\mu$ m
	Winding turns	4
	Winding litz wire	1200x0.2 mm
Full-bridge	MOSFETs (2 parallel)	Infineon IPW60R041C6
Rectifier	MOSFETs (11 parallel)	IR IRF4668PbF
Capacitors	Output (44 parallel)	Murata X7R
		2.2 $\mu$ F/100 V

As the full-bridge MOSFETs (STY112N65M5), which have been assumed in the optimization, are not yet available, the Infineon CoolMOS™ IPW60R041C6 [16] has been applied. Although the CoolMOS™ device has a higher on-resistance ( $R_{DS,on} = 41$  m $\Omega$ , compared to  $R_{DS,on} = 19$  m $\Omega$  of the STY112N65M5), the efficiency theoretically still reaches 99 % at the maximum with the same assumptions made in the optimization procedure. A summary of the components used is given in table IV.

Due to the selection of commercial cores instead of calculated ones, the volume is higher than the volume limit of 0.3 liters (18.3 in<sup>3</sup>) used in the optimization procedure. The volume of the transformer is 0.48 liters (29.2 in<sup>3</sup>) and 0.39 liters (23.1 in<sup>3</sup>) for the output inductor. The larger volume theoretically leads to further improvements in the calculated efficiency of the magnetic devices, but to a lower power density. Due to the used core-assembly in the prototype, the cross-section area is increased by factor 1.5, which results in decreased core losses by a factor  $\approx 2.8$  (from 10.0 W to 3.6 W). The drawback in the assembly is the smaller winding-window height, where the calculated optimal foil windings

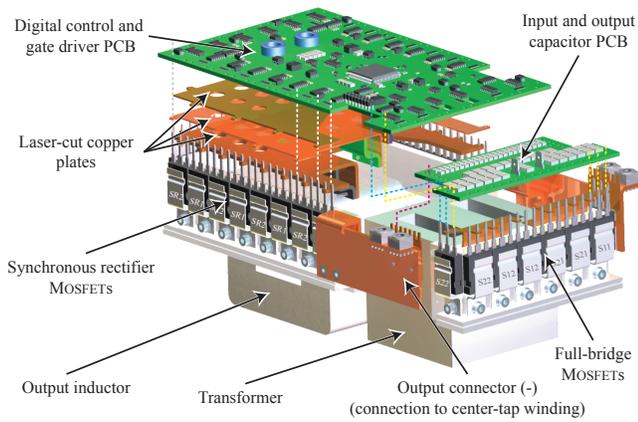


Figure 6. Exploded assembly drawing of the realized converter prototype. (The case not shown.)

could not be applied and the resulting winding losses are higher.

In Fig. 6, the exploded assembly drawing of the prototype is presented. The MOSFETs are clamped on mounting frames, which are electrically isolated for the synchronous rectifier and the full-bridge. The synchronous rectifier MOSFETs are directly assembled with thermal grease on the plate (alternately, i.e. SR1 - SR2 - SR1 ...), as the drains have the common inductor potential. The phase-change material Hi-Flow<sup>®</sup> 300P [17] has been applied as electrical insulation for the full-bridge switches. The low-resistive connections between MOSFETs and windings were made with laser-cut copper plates. A Printed Circuit Board (PCB) with the output capacitors and low-inductive input capacitors for the full-bridge MOSFETs is arranged first above the connection layers. On top of the converter system is the control electronics PCB.

The MOSFET's mounting frames are arranged around the magnetic devices (transformer and output inductor). Except as presented in [5], the transformer, inductor and power semiconductors are cooled solely by free convection. The final prototype assembly is shown in Fig. 1.

The volume distribution of the prototype is illustrated in Fig. 7 (light gray bars). It can be seen, that approx. one third of the total volume is used for the connections and spacing, which is similar to high compact converter systems as presented e.g. in [5]. As no heat sinks are required for the parallel connected power switches, the contribution to the total volume is small. The magnetic devices have together the highest volume share

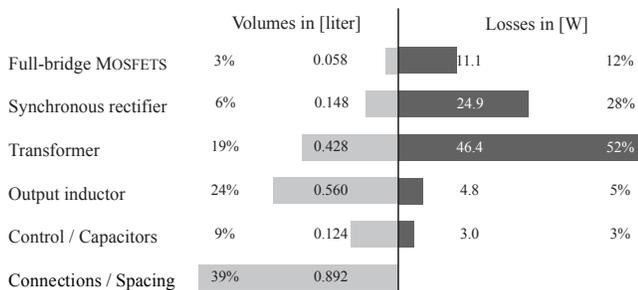


Figure 7. Loss and Volume distribution at full load (5 kW) for the prototype.

( $\approx 1$  liter, 43% of the total volume). The resulting power density (bounding box around the system) of the prototype design as presented in Fig. 1 is  $\rho = 2.2$  kW/liter ( $36$  W/in<sup>3</sup>).

The calculated loss distribution at full load conditions is shown in Fig. 7 (dark gray bars). The turn-off energy  $E_{off}$  in the synchronous rectifier, which has not been considered in the optimization procedure, are modeled for the calculations in Fig. 7 by

$$E_{off} = Q_{rr} \cdot V_{Drr}, \quad (2)$$

where  $Q_{rr}$  represents the total switching charge and  $V_{Drr}$  the blocking voltage. The calculation with (2) is only a simple approximation, as the current is not considered. The charge consisting of the reverse recovery charge and output capacitor charge was measured (cf. Fig. 11), as the recovery charge given in the data sheet is measured under different conditions. The resulting losses in the synchronous rectifier are the second highest share in the distribution of the total power losses.

The highest share is the transformer losses (more than 50%), mainly caused by the high HF-winding losses  $P_{wind} \approx 42.8$  W due to high proximity losses, as the optimal litz wires have not been available.

The losses in the control electronic and auxiliary supply are almost constant over the entire load range. In the prototype, the Digital Signal Processor (DSP) TI TMS320F2808 [18] is clocked with a reduced frequency (20 MHz instead of 100 MHz), which reduces the DSP power consumption by 62% from approx. 550 mW to 210 mW [18]. In addition, the design of the control electronics for the DC-DC converter also focused on efficiency. The measured input power for the whole control electronics excluding the gate drive losses is 610 mW during operation.

## B. Measurement Results

In Fig. 8 the measured transformer primary current  $i_p$  and voltage waveforms  $v_p$  at full-load operation of the converter system are illustrated ( $V_{in} = 400$  V,  $V_{out} = 48$  V,  $P_{out} = 5065$  W). The converter is operating with zero voltage switching and no voltage-overshoot is present. The small overshoot of the primary transformer current  $i_p$  results from the reflected secondary transformer side recovery current of the synchronous rectifier. The characteristic current points  $I_{p1}$ ,  $I_{p2}$  and  $I_{p3}$ , which are illustrated in Fig. 8, are the important values calculated for the operation point determination in the optimization loop as explained in II.

A summary of the characteristic values of the operation point is presented in table V for validating the analytical models. The first column shows the values resulting from the optimization procedure. The characteristic values in the second column were determined with an electrical circuit simulation program (GeckoCIRCUITS [19]), where additional parasitic elements, e.g. output capacitors of the MOSFETs, have been considered. In the third column, the analysis of the measurement results in Fig. 8 is shown. All values shown in table V are in close agreement thereby validating the analytical converter model applied.

The measured converter efficiency as a function of the output power is presented in Fig. 9. The measurement shows

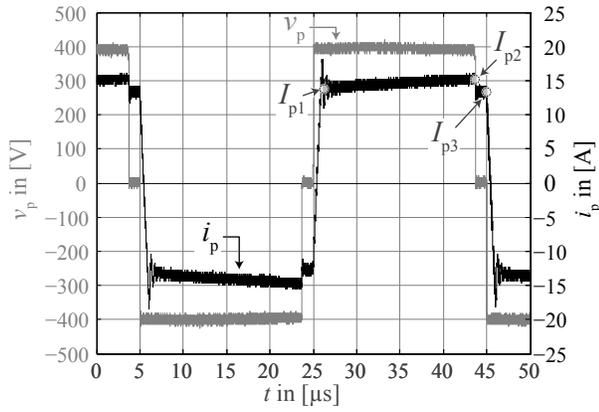


Figure 8. Measured transformer primary current  $i_p$  and voltage  $v_p$  at full-load operation ( $V_{out} = 48\text{ V}$ ,  $P_{out} = 5065\text{ W}$ ). The characteristic current points  $I_{p1}$ ,  $I_{p2}$  and  $I_{p3}$  are illustrated.

Table V  
COMPARISON OF THE CHARACTERISTIC OPERATION POINT VALUES RESULTING IN THE OPTIMIZATION PROCEDURE, SIMULATION (WITH/WITHOUT PARASITICS) AND MEASUREMENTS.

	Calculation	Simulation incl. parasitics	Measurement
$V_{in}$	400.0 V	400.0 V	399.7 V
$V_{out}$	48.0 V	48.0 V	48.1 V
$P_{out}$	5000 W	5000 W	5065 W
Duty cycle	0.903	0.908	0.933
$I_{P1}$	13.2 A	13.8 A	13.8 A
$I_{P2}$	15.3 A	15.2 A	15.2 A
$I_{P3}$	15.0 A	11.8 A	13.3 A
$I_{P,rms}$	14.2 A	13.9 A	14.1 A

that the required Energy Star<sup>®</sup>-efficiency is clearly exceeded in the entire load range and exhibit flat characteristics even at light load. The calculated efficiency for the applied components (cf. table IV) and the reference efficiency (optimization goal) are plotted as well. The influence of the synchronous rectifier switching losses is illustrated by the two efficiency curves which are based on calculations. The switching losses are not considered for the curve marked with "Calculation" in Fig. 9. The simple recovery-energy model in (2) for a single synchronous rectifier MOSFET has been applied for the second calculated curve "Calculation +switching losses". The latter calculated curve is almost identical with the measured efficiency curve above 40% load, slightly underneath between 20% and 40% load, and up to approx. 1.5% above the measured curve for light loads smaller 20%.

An initial estimate of the loss-distribution can be obtained from the thermal image of the converter system operating at full load (time > 30 min) as depicted in Fig. 10. In order to measure the temperature of the magnetic components, the acrylic glass-box of the prototype assembly as shown in Fig. 1 has been removed. Although the system components are cooled solely by free convection, the maximum temperature of the synchronous rectifier and full-bridge MOSFETs is approx. 60°C (ambient-temperature  $T_{amb} = 27^\circ\text{C}$ ).

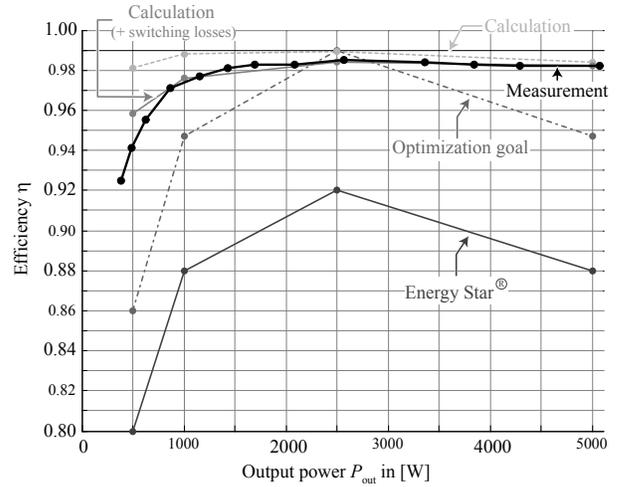


Figure 9. Measured efficiency for the converter system:  $V_{in} = 400\text{ V}$ ,  $V_{out} = 48\text{ V}$ ,  $P_{out} = 383..5065\text{ W}$ . The calculated and target efficiency are illustrated additionally.

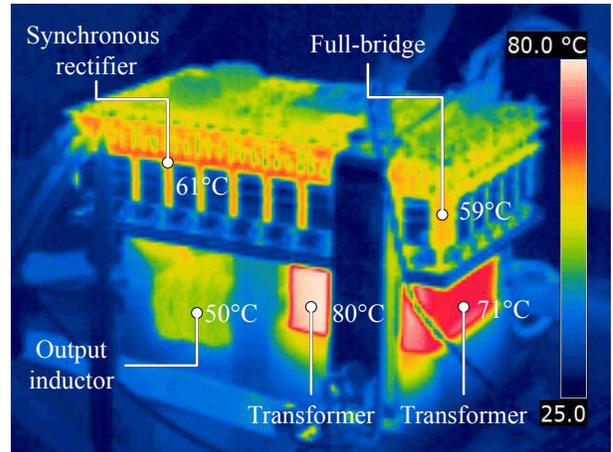


Figure 10. Infra-red image of the converter system operating for more than 30 min at full load ( $V_{in} = 400\text{ V}$ ,  $V_{out} = 48\text{ V}$ ,  $P_{out} = 5047\text{ W}$ , ambient temperature =  $27^\circ\text{C}$ ). The acrylic glass box as shown in Fig. 1 has been removed in order to measure the temperatures of the magnetic components.

In the next subsection, the transformer losses, the losses in the connections and synchronous rectifier are analyzed and discussed in more detail. As presented below, improvements in the assembly and synchronous rectifier result in an increase of the system efficiency.

a) *Transformer losses:* As shown in Fig. 10, the transformer exhibits the highest temperature ( $T_{trafo} \approx 80^\circ\text{C}$ ), which corresponds with Fig. 7, where the transformer has the major influence on the loss distribution. In order to validate the transformer loss-model a comparative measurement is performed: DC-current sources are connected to the transformer windings and increased in steps after a steady-state gain in temperature. The cooling conditions are almost identical to the operation conditions in the converter. The temperatures from the thermal images are compared with the temperatures in Fig. 10 (full load operation). An equivalent temperature was reached as the measured primary and secondary winding DC-losses were above 42W. Compared to the calculated losses

$P_{trafo} \approx 46$  W (including core and HF-winding losses), the difference is approx. 4 W.

By measuring the power during the comparison experiment, the DC winding resistance can be measured as well. These are only slightly higher than the calculated ones:

	Calc. $R_{DC}$	Meas. $R_{DC}$
Primary winding	$\approx 17.1$ m $\Omega$	$\approx 17.5$ m $\Omega$
Secondary winding	$\approx 0.94$ m $\Omega$	$\approx 1.1$ m $\Omega$

However, the difference between the calculated and measured resistance on the secondary winding (0.16 m $\Omega$ ) already causes approx. 2 W additional losses.

Further losses can be caused by parameter tolerances of the core. The measured core losses with the method as shown in [20] are approx. 1 W higher than calculated with Steinmetz-parameters gained from the data sheet.

b) *Connection losses*: One missing item in the loss calculation is the neglected resistance (DC and AC) in the interconnections, as this parameter is strongly dependent on the realization. The switches S11, S22, SR1 and S22 are closed, and current sources are connected to the input and output of the converter in order to determine the DC-resistance. The input-DC-current flows via S11 and S22 through the primary winding whereas the fed output current flows via SR1 and S22 through the secondary transformer windings and the output inductor winding. The resulting connection resistance, (measured resistance minus the calculated resistances for the semiconductors and windings) is only 0.1 m $\Omega$ , which results in approx. 1 W more losses at full-load conditions. However, the AC-resistance in the connections is not considered. An impedance-measurement is difficult due to the small resistance value.

c) *Synchronous rectifier*: As described before and presented in Fig. 9, the influence of the switching losses on the total converter efficiency can not be neglected. One possibility of reducing the switching losses in the synchronous rectifier is to determine the optimum switch-off point in time  $t_{off,SR}$  as presented below.

In Fig. 11, the drain current  $i_D$ , the drain-source voltage  $v_{DS}$  and the control signal of the rectifier switch  $SR2$  during the turn-off phase are shown. If the rectifier MOSFET is turned off at the same point of time as when the full-bridge switching state changes from the free-wheeling phase to the active phase ( $t_{off,SR} = 0$  in Fig. 11), the current commutates first from the MOSFET to the body diode and afterwards to the opposite synchronous rectifier MOSFET. This results in additional recovery losses, in forward conduction losses and for the prototype presented, to further losses due to avalanche effects, as shown in Fig. 11. The high voltage ringing, due to the resonance tank of the secondary winding leakage inductance and the output capacitance of the synchronous rectifier MOSFETs, can be reduced by a bifilar secondary winding implementation, resulting in a smaller stored leakage energy, which would prevent avalanche losses.

If a time delay for the turn-off-signal of the rectifier switch is implemented, i.e.  $t_{off,SR} > 0$ , the losses also change

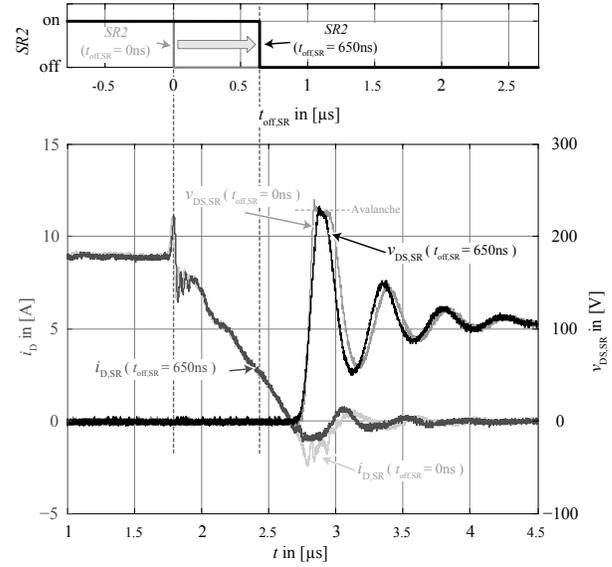


Figure 11. Measured drain current  $i_{D,SR}$  and drain-source voltage  $v_{DS,SR}$  waveform of a synchronous rectifier MOSFET when turning off for  $t_{off,SR} = 650$  ns and  $t_{off,SR} = 0$  ns (light gray curves). The control signal for MOSFET  $SR2$  is illustrated as well.

due to the reduced body diode conduction time. Due to that, the forward conduction losses are reduced, in the one hand. In the other hand, the recovery charge is reduced, which results in a decreased reverse-current peak  $I_{RRM}$  and the reduced over-voltage results in smaller or no avalanche energy, respectively. The improvements can be seen in Fig. 12, where the dependency of the system efficiency  $\eta$  on the switch-off-time  $t_{off,SR}$  is presented. At full-load operation of the converter ( $P_{out} \approx 5055$  W), the efficiency can be improved by approx. 0.35 %, i.e. the losses are reduced by over 18 W, which is almost 20 % of the measured total losses. The share of forward conduction losses to the total loss reduction is approx. 22 % ( $\approx 4$  W). The efficiency at 50 % load ( $P_{out} \approx 2050$  W) could be increased by 0.32 %, i.e. a loss-reduction of 8.6 W (again, almost 20 % of the measured total losses).

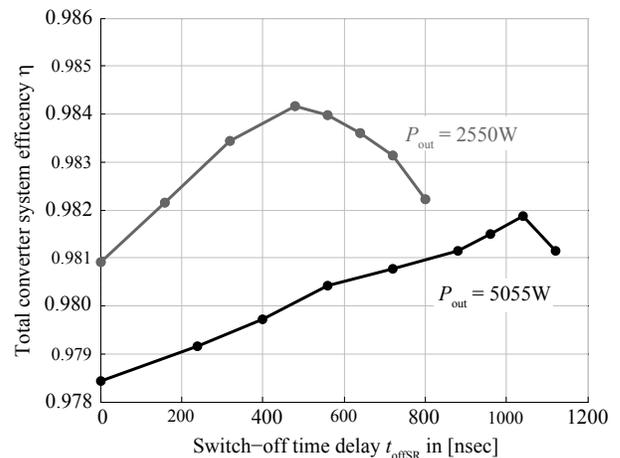


Figure 12. Measured efficiency for the converter system in dependency of the switch-time delay of the synchronous rectifier after the after the full-bridge changes from the free-wheeling to the powering state.

As presented in Fig. 12, there is an optimum switch-off-time. The losses will quickly increase and could destroy the MOSFETs, if the switch-off-time is chosen too high, i.e. the current has completely commuted to the opposite rectifier switch. A continued conduction of the (still) switched-on rectifier will cause a short circuit. The switch-off time, which is dependent on the output current, can be saved as a table in the DSP.

The recovery charge is small, if the MOSFET is switched off at the optimal  $t_{off,SR}$ , mainly caused by the relatively small  $\frac{di}{dt}$  ( $\approx 10 \frac{A}{\mu s}$ ) and the smaller current, which has to be switched off. However, due to the output capacitor charge  $Q_{oss}$ , the total measured charge is reduced from 392 nC at  $t_{off,SR} = 0$  to approx. 208 nC at full load and the optimal point of time  $t_{off,SR} = 650$  ns. The measured switching losses are reduced from 29.3 W at  $t_{off,SR} = 0$  to 16.5 W. The turn-off losses due to the output capacitor and the remaining recovery charge will be included in the optimization procedure.

If the number of parallel synchronous rectifier switches is reduced, the efficiency maximum can be further increased due to the reduced switching losses, e.g., if the conservative formula for the turn-off-energy in (2) is used, the minimum losses are obtained with 5 switches in parallel instead of 11 and the efficiency increases from 98.4% to 98.6% at 50% load. The full-load-losses, however, would increase by 5.73 W due to the increased conduction losses. The optimal number of parallel switches results in 4, if the optimization criteria as presented in section II is considered.

The analytical models have been validated by the measurement results. As some components considered in the optimization procedure have not been available, the realized prototype does not reach the targeted efficiency of 99%. In order to improve the efficiency, the following design parameters are changed:

- Primary winding litz wires 420x0.1 mm.
- Secondary winding litz wires 800x0.2 mm.
- Number of parallel sync. rectifier switches  $n_{sw,s} = 5$ .
- Losses in the control electronic are reduced to the measured value  $P_{aux} = 610$  mW.
- Output capacitor charge  $Q_{oss}$  is considered  $Q_{rr}$  in (2) for synchronous rectifier switching losses.
- Full-bridge MOSFETs are ST STY112N65M5.

With the adopted prototype design parameters, the resulting efficiency at 50% load is  $\eta = 99.0\%$  (24.4 W total losses).

## V. CONCLUSION

In this paper, the design process of an ultra high efficient, 5 kW, 400 V/48..54 V phase-shift PWM DC-DC converter with synchronous rectifier and LC-output filter for data center and telecom application is presented. An optimization procedure based on comprehensive analytical models, considering the part-load efficiency and with the goal of  $\eta \geq 99\%$  at 50% load, was applied to find the optimal design. First measurements with the prototype result in a maximum efficiency of  $\eta = 98.5\%$  at 50% load and a flat efficiency curve over almost the entire load range. The analytical models applied in the

optimization procedure have been validated by the measurement results. The goal of 99% is achievable with the presented prototype mainly enabled by changing the parameters of the transformer assembly and reducing the number of synchronous rectifier switches. The power density of the realized prototype is  $\rho = 2.3$  kW/liter (38 W/in<sup>3</sup>).

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