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***Abstract*—The operation and efficiency of on-chip switched-capacitor (SC) converters are highly affected by the parasitic bottom plate capacitor present in on-chip capacitor technologies. Existing modeling frameworks do not in a comprehensive manner take the effect of the bottom plate capacitor on converter operation and efficiency into account. This paper extends an existing SC state space modeling framework to include the bottom plate capacitor. The developed model is used in a Pareto optimization procedure to optimally select the component values of a 2:1 on-chip SC converter. Implemented in a 32 nm SOI CMOS technology that features the high-density deep trench capacitor, the on-chip converter achieves 86% maximum efficiency at 4.6 W/mm² power density while converting from a 1.8 V input voltage to 830 mV output voltage.**

***Index Terms*—Pareto optimization, power integrated circuits, switched capacitor circuits, state space methods.**

I. Introduction

HIGH-PERFORMANCE microprocessor systems could benefit significantly on critical aspects such as total energy consumption by incorporating on-chip voltage regulators (OCVR). An OCVR is a fully integrated voltage regulator that generates the microprocessor's desired supply voltage (e.g., 0.9 V [1]) from a higher-than-nominal supply voltage (e.g., 1.8 V). Furthermore, the OCVR is integrated on the same chip die as the microprocessor itself, thereby acting as a point of load (POL) converter.

From a package point of view, an OCVR can reduce the number of power/ground pins that carry the high supply currents required by modern high-performance microprocessors [2]–[4]. Reducing the number of power/ground pins is extremely attractive because more than half the total number of package pins in today's microprocessors are reserved for power/ground [1], and trend analyses confirm these characteristics also for future microprocessor systems [4]. Furthermore, OCVRs enable per-core regulation in multicore microprocessor. Having one dedicated OCVR per microprocessor core facilitates new power management architectures in which the supply voltage of each core can be regulated according to its independent needs. Applying ultrafast dynamic voltage and frequency scaling (DVFS), which extends traditional DVFS by capturing within-workload supply voltage variations, has the potential to reduce the overall microprocessor system energy by up to 21% [5].

Traditionally, buck converters are used as POL converters for microprocessor power delivery. Research in microfabricated inductors have focused on achieving high inductor quality factors at small footprints. The current state of the art targets 3D chip integration, where the buck converter is implemented on an interposer in close proximity to the microprocessor chip die [6]–[9]. However, buck converters are typically not integrated on the same deep submicron chip die as the microprocessor. Inductors using only metals available in the chip metal stack (air core inductors) achieve poor quality factors because of the small metal thicknesses defined by the fabrication process [10]. Furthermore, magnetic materials that increase the quality factor and the inductance typically are not readily available in deep submicron semiconductor technologies. In contrast, switched capacitor (SC) converters can be implemented using only switches and capacitors that are readily available in the deep submicron semiconductor technologies. For this reason, this paper focuses on on-chip SC converters.

A widely accepted model framework for SC converters is introduced in [11] and further developed in [12]. This model framework can be used to derive a switching frequency dependent equivalent output resistance R_{eq} that accounts for the converter's conduction losses. However, it has two disadvantages regarding OCVR applications: first, a quadratic approximation is used to calculate R_{eq}, and this approximation is least accurate when the SC converter is operated at its highest efficiency [13]. However, it should be noted that the work in [14] determines a fitting constant to overcome the issues with the approximation. Second, it does not include switching losses, which are mainly associated with the parasitic bottom plate capacitors of the flying capacitors. Switching losses due to the parasitic bottom plate capacitor may not be of major concern for discrete SC converters since the parasitic bottom plate capacitors of discrete capacitors can often be neglected. However, they cannot be neglected for on-chip SC converters and may have significant influence on the converter's output current and efficiency.

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In [15] and [16], the parasitic bottom plate capacitor is included in SC multiplier circuits, but the analyses carried out disregard the on-state resistances of the switches. The work in [17] includes the parasitic bottom plate capacitor in an analytical loss model, thereby providing direct insight into how various circuit parameters influence the efficiency. However, the analysis is based on a sum approximation to achieve the simple equations, but, similarly to [12], the sum approximation is least accurate when the SC converter is operated at its highest efficiency. In [13], a SC model framework based on conventional circuit analysis put into a state space model representation is used. Once all node equations have been put into matrix form, $R_{\rm eq}$ can be calculated accurately. However, this model framework does not account for switching losses.

This paper, which is based on [3], [18], and [19], extends the state space modeling framework in [13] to take the effect of the parasitic bottom plate capacitor (i.e., switching losses) on capacitor currents and converter efficiency into account. The model framework makes no approximations when determining the equivalent output resistance $R_{\rm eq}$ of the converter. The state space model is used in a Pareto optimization procedure for on-chip SC converters to optimally select the design parameters for a given converter specification [20].

Recent SC converter designs, which are implemented using integrated deep trench capacitors having high capacitance density and low parasitic bottom plate capacitance, have shown much improved efficiency and power density performance than SC converters using conventional MOS or MIM capacitors [2], [3], [18], [19], [21]–[23]. This paper presents an on-chip 2:1 SC converter implemented in a 32 nm SOI CMOS technology that features the deep trench capacitor for high efficiency and high power density.

In Section II, a basic analysis for a 2:1 SC converter is carried out. However, the analysis is challenging to apply for SC converters with conversion ratios other than 2:1. Therefore, a general model framework for SC converters is sought. In Section III, the SC converter state space model framework, which includes the effect of the parasitic bottom plate capacitor, is derived and verified with MATLAB Simulink simulations. In Section IV, the model framework is used in a Pareto optimization procedure to optimally select the SC converter design parameters. Section V details the implementation of a 2:1 converter, which furthermore incorporates a charge recycling circuit that reduces the switching losses associated with the parasitic bottom plate capacitor. The experimental results are presented in Section VI.

II. Basic 2:1 SC Converter Analysis

As depicted in Fig. 1, the 2:1 SC converter consists of a flying capacitor C and four switches having on-state resistances $R_{\rm on}$. For simplicity, all switches are assumed to have equal on-state resistances, however, the analysis applies for unequal on-state resistances as well. In steady state, the flying capacitor is switched with 50% duty cycle between 1) the charging state, where the flying capacitor is in series between the input and the output (switches S_1 and S_3 are on), and 2) the discharging state, where the flying capacitor is in parallel with the output (switches S_2 and S_4 are on), leaving the input disconnected. In [24], the SC converter analysis is extended to include the dead-time interval, which is present in practical implementations as the transition states between the charging state and the discharging state, and vice versa. From simulations in the 32 nm technology, these transition states are found to have negligible impact on the converter performance. Therefore, the transition states are left out in the following analyses for simplicity.

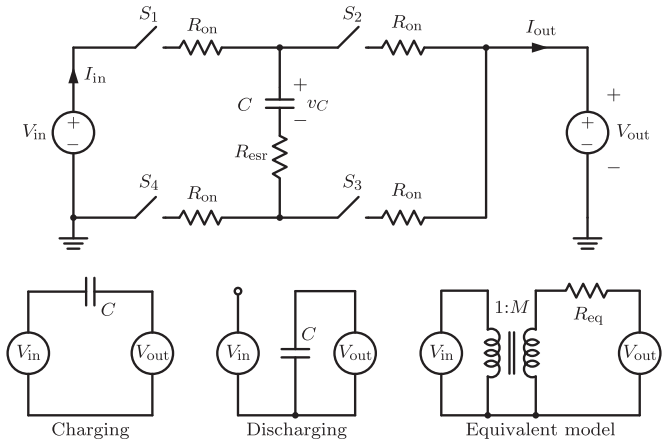


Fig. 1. 2:1 SC converter including the parasitic on-state resistances $R_{\rm on}$ of the switches and the equivalent series resistance $R_{\rm esr}$ of the flying capacitor. The capacitor is in series between the input and the output supplies in the charging state, and in parallel with the output supply in the discharging state. The basic equivalent model consists of an ideal transformer with conversion ratio $M = 1/2$ and equivalent output resistance $R_{\rm eq}$ that governs the conduction losses [11], [12].

To charge a capacitor with capacitance C through a resistor with resistance R, the capacitor voltage can be described as

$$v_C(t) = V_1 + (V_0 - V_1)\mathrm{e}^{-t/(RC)} \tag{1}$$

where V_1 is the voltage that the capacitor charges toward from its initial voltage V_0.

For the 2:1 SC converter in Fig. 1, the capacitor charges toward $V_{\rm in} - V_{\rm out}$ in the charging state, and it discharges toward $V_{\rm out}$ in the discharging state. The steady-state flying capacitor voltage $v_C(t)$ for constant $V_{\rm in}$ and $V_{\rm out}$ is depicted in Fig. 2. As seen, the capacitor charges and discharges toward $V_{\rm in} - V_{\rm out}$ and $V_{\rm out}$, respectively, and the voltages $V_{C,\max 1}$ and $V_{C,\min 1}$ denote the actual voltages that the capacitor charges or discharges to, respectively, within one switching period $T_{\rm sw} = 1/f_{\rm sw}$. Using (1), the expressions for $V_{C,\max}$ and $V_{C,\min}$ in the charging and discharging states, respectively, become

$$V_{C,\max} = V_{\rm in} - V_{\rm out} + (V_{C,\min} - V_{\rm in} + V_{\rm out})e^{-1/(2f_{\rm sw}R_{\rm tot}C)} \tag{2}$$

$$V_{C,\min} = V_{\rm out} + (V_{C,\max} - V_{\rm out})e^{-1/(2f_{\rm sw}R_{\rm tot}C)} \tag{3}$$

where $R_{\rm tot} = 2R_{\rm on} + R_{\rm esr}$ denotes the total resistance in series with the capacitor in both states, and $t = 1/(2f_{\rm sw})$ for 50% duty cycle.

Also shown in Fig. 2 is another steady-state flying capacitor voltage waveform at four times the switching frequency, but having the same input and output voltages. Again, the capacitor charges and discharges toward $V_{\rm in} - V_{\rm out}$ and $V_{\rm out}$, respectively. Applying (2) and (3) with four times the switching

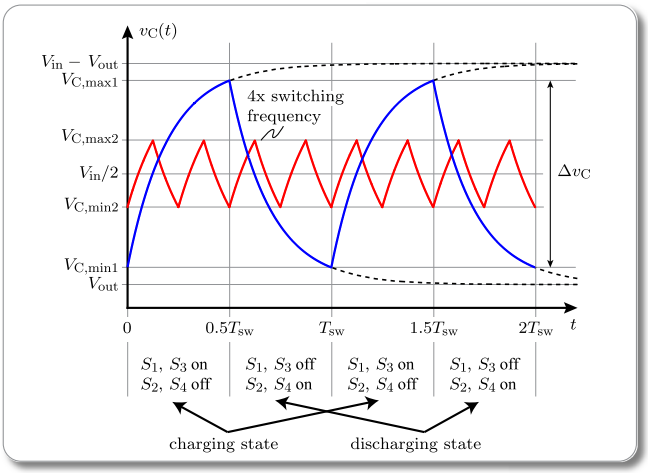


Fig. 2. Steady-state voltage $v_C(t)$ of the flying capacitor shown for two switching frequencies. The voltage difference Δv_C is used to determine the charge delivered to the output per switching period T_{sw}.

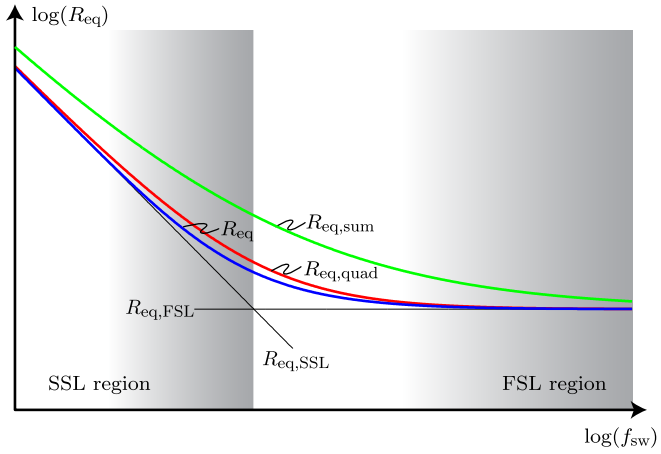


Fig. 3. Equivalent output resistance R_{eq} as function of the switching frequency. The R_{eq} has a $1/f_{sw}$ behavior in the SSL region and a frequency-independent behavior in the FSL region. The quadratic and sum approximated equivalent output resistances $R_{eq,quad}$ and $R_{eq,sum}$ can easily be derived using simple circuit analysis.

frequency compared to aforementioned, the capacitor charges and discharges to $V_{C,max2}$ and $V_{C,min2}$, respectively, as shown. As can be further noted, the capacitor voltage always switches around $V_{in}/2$ for the 2:1 SC converter.

Solving (2) and (3) for $V_{C,max}$ and $V_{C,min}$, the capacitor voltage difference Δv_C can be found to be

$$\Delta v_C = V_{C,max} - V_{C,min} = (V_{in} - 2V_{out})k \tag{4}$$

with

$$k = \frac{1 - e^{-1/(2f_{sw}R_{tot}C)}}{1 + e^{-1/(2f_{sw}R_{tot}C)}}. \tag{5}$$

The flying capacitor delivers an equal amount of charge $C\Delta v_C$ to the output in each state, so the total output charge per switching period is

$$Q_{out} = 2C\Delta v_C \tag{6}$$

and the output current becomes

$$I_{out} = Q_{out}f_{sw} = 2C(V_{in} - 2V_{out})kf_{sw}. \tag{7}$$

The efficiency of the 2:1 SC converter using the equivalent model in Fig. 1 is

$$\eta = \frac{V_{out}I_{out}}{V_{in}I_{in}} = \frac{V_{out}}{MV_{in}} = \frac{2V_{out}}{V_{in}} \tag{8}$$

since $I_{in} = MI_{out}$, where $M = 1/2$ for the 2:1 SC converter. Hence, the efficiency of the SC converter is 100% when $V_{out} = V_{in}/2$, but it drops linearly with decreasing output voltage for $V_{out} < V_{in}/2$. The linear decrease in efficiency at decreasing output voltage is similar to a linear regulator except for the voltage conversion ratio M defined by the converter topology. That the efficiency drop linearly from 100% will not hold true when the more accurate state space model, which includes the parasitic bottom plate capacitor, is derived and applied in the next section.

Using the output current expression in (7) with the equivalent model in Fig. 1, the equivalent output resistance of the SC converter becomes

$$R_{eq} = \frac{V_{in}/2 - V_{out}}{I_{out}} = \frac{1}{4Ckf_{sw}}. \tag{9}$$

As seen, R_{eq} is frequency dependent, and it contains the exponential terms governed by the factor k from (5).

The equivalent output resistance can be decomposed into two resistance contributions governing the slow switching limit (SSL) and the fast switching limit (FSL), respectively. As shown in [12], $k \to 1$ for $f_{sw} << 1/(2R_{tot}C)$, and $k \to 1/(4CR_{tot}f_{sw})$ for $f_{sw} >> 1/(2R_{tot}C)$. Hence, the equivalent resistance frequency asymptotes can be derived using (9) as

$$R_{eq,SSL} = \frac{1}{4Cf_{sw}} \tag{10}$$

$$R_{eq,FSL} = R_{tot}. \tag{11}$$

In [12], a model framework to derive $R_{eq,SSL}$ and $R_{eq,FSL}$ for any SC converter topology is developed. The model framework can be applied on any SC converter using simple circuit analysis techniques. A simple approximation to R_{eq} based on the aforementioned is the sum approximation

$$R_{eq,sum} \approx R_{eq,SSL} + R_{eq,FSL}. \tag{12}$$

However, a more accurate approximation is the quadratic approximation

$$R_{eq,quad} \approx \sqrt{R_{eq,SSL}^2 + R_{eq,FSL}^2}. \tag{13}$$

In [14] and [24], the quadratic approximation is fitted to the accurate curve by adjusting the exponent in (13) to equal 2.54 instead of 2.

The equivalent output resistance over switching frequency is shown in Fig. 3. As seen, R_{eq} in the SSL region asymptote dictates a $1/f_{sw}$ behavior at low switching frequencies, whereas the FSL is independent of frequency. The sum approximation

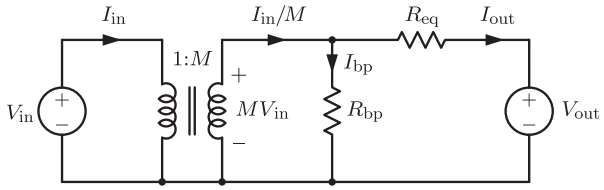


Fig. 4. Extended SC converter equivalent model, where the ideal transformer models the voltage conversion ratio M defined by the topology and the resistors $R_{\rm eq}$ and $R_{\rm bp}$ model conduction and switching losses, respectively.

$R_{\rm eq,sum}$ from (12) is seen to deviate from $R_{\rm eq}$. However, $R_{\rm eq,quad}$ from (13) is seen to match $R_{\rm eq}$ from (9) fairly well.

It is elaborated in [12] that $R_{\rm eq,SSL}$ and $R_{\rm eq,FSL}$ are comparably much simpler to derive than the exact expression of $R_{\rm eq}$ in (9), especially for other SC converter topologies having more switches and capacitors. Accordingly, the model framework in [12] is by many considered the preferred approach for SC converter modeling and design. The SSL region is typically used in applications where high efficiency is not a design target. The region between SSL and FSL is often preferred for high-efficiency operation since $R_{\rm eq}$ is low and $f_{\rm sw}$ is moderate. The FSL region is typically avoided due to high switching losses not accounted for in Fig. 3. Switching losses associated with the parasitic bottom plate capacitor may not be of major concern for discrete SC converters since the parasitic bottom plate capacitors of discrete capacitors can often be neglected. However, for on-chip implementations, switching losses associated with the parasitic bottom plate capacitor may influence the converter's steady-state operation and efficiency and can not be neglected. Besides, the parasitic output capacitors of the transistors add to switching losses as well. For these reasons, the next section develops a model framework that accurately captures the effect of the parasitic bottom plate capacitor and the associated switching losses.

III. State Space Model Framework

The extended SC converter equivalent model is shown in Fig. 4. It features $R_{\rm bp}$, which models the switching losses associated with the parasitic bottom plate capacitor. As seen, $R_{\rm bp}$ sinks a current $I_{\rm bp}$ that would otherwise have been delivered to the output. Switching losses affect both the steady-state converter behavior and the efficiency.

A. Model Derivation

The state space model derivation is based on [13] and [18]. Generally, there are n flying capacitors and n bottom plate capacitors, which are put as diagonal elements into a $2n$ diagonal matrix $\mathbf{C}$. The input and the output voltages are composed into vector $\mathbf{u}$. Vectors $\mathbf{v}(t)$ and $\mathbf{i}(t)$ collect all instantaneous capacitor voltages and currents, respectively, and they are related by

$$\mathbf{i}(t) = \mathbf{C}\dot{\mathbf{v}}(t) \tag{14}$$

where $\dot{\mathbf{v}}(t)$ is the time derivative of $\mathbf{v}(t)$.

For the charging state (state 1), Kirchhoff's voltage and current laws (KVL and KCL, respectively) are applied to determine $2n$ independent equations of the form

$$\mathbf{E}_1\mathbf{i}(t) + \mathbf{F}_1\mathbf{v}(t) + \mathbf{G}_1\mathbf{u} = \mathbf{0}. \tag{15}$$

When the KVL is applied, rows in $\mathbf{E}_1$ are resistances (transistor on-state resistances and / or flying capacitor equivalent series resistances), and rows in $\mathbf{F}_1$ and $\mathbf{G}_1$ are -1, 0, or 1. When the KCL is applied, rows in $\mathbf{E}_1$ are -1, 0, or 1 and rows in $\mathbf{F}_1$ and $\mathbf{G}_1$ are all 0. Letting $\mathbf{v}$ represent the system states, (14) and (15) can be combined into

$$\begin{aligned} \dot{\mathbf{v}}(t) &= \mathbf{A}_1\mathbf{v}(t) + \mathbf{B}_1\mathbf{u} \\ \mathbf{A}_1 &= -\mathbf{C}^{-1}\mathbf{E}_1^{-1}\mathbf{F}_1 \\ \mathbf{B}_1 &= -\mathbf{C}^{-1}\mathbf{E}_1^{-1}\mathbf{G}_1 \end{aligned} \tag{16}$$

where $\mathbf{C}$ is always invertible because it is a diagonal matrix and $\mathbf{E}_1$ is invertible when the KVL and KCL have been applied correctly [13]. The general solution to the system of differential equations in (16) is

$$\mathbf{v}(t) = \underbrace{e^{\mathbf{A}_1(t-t_0)}}_{\mathbf{\Phi}_1(t)}\mathbf{v}(t_0) + \underbrace{\left[\int_{t_0}^{t} e^{\mathbf{A}_1(t-\tau)}\mathbf{B}_1 \mathrm{d}\tau\right]}_{\mathbf{\Gamma}_1(t)}\mathbf{u} \tag{17}$$

where we have utilized that $\mathbf{u}$ is independent of τ. $\mathbf{\Phi}_1(t)$ is known as the state transition matrix. Using the same approach for the discharging state (state 2) results in $\mathbf{A}_2$ and $\mathbf{B}_2$, as well as $\mathbf{\Phi}_2(t)$ and $\mathbf{\Gamma}_2(t)$.

With 50% duty cycle, $t_1 = 1/(2f_{\rm sw})$ is the duration of the charging state, and $t_2 = 1/(2f_{\rm sw})$ is the duration of the discharging state. Hence, assuming the charging state begins at $t_0 = 0$, the system states (capacitor voltages) at the end of each switching state equal

$$\mathbf{v}(t_1) = \mathbf{\Phi}_1(t_1)\mathbf{v}(0) + \mathbf{\Gamma}_1(t_1)\mathbf{u} \tag{18}$$

$$\mathbf{v}(t_1 + t_2) = \mathbf{\Phi}_2(t_2)\mathbf{v}(t_1) + \mathbf{\Gamma}_2(t_2)\mathbf{u}. \tag{19}$$

In steady state, $\mathbf{v}(0) = \mathbf{v}(t_1 + t_2)$ applies, which, using (18) and (19), gives the initial condition

$$\mathbf{v}(0) = \mathbf{I} - \mathbf{\Phi}_2(t_2)\mathbf{\Phi}_1(t_1)^{-1}\mathbf{\Phi}_2(t_2)\mathbf{\Gamma}_1(t_1) + \mathbf{\Gamma}_2(t_2)\mathbf{u} \tag{20}$$

where $\mathbf{I}$ is the $2n$ identity matrix. The charge delivered by each capacitor per switching state is determined as

$$\mathbf{q}_1 = \mathbf{C}\mathbf{v}(t_1) - \mathbf{v}(0) \tag{21}$$

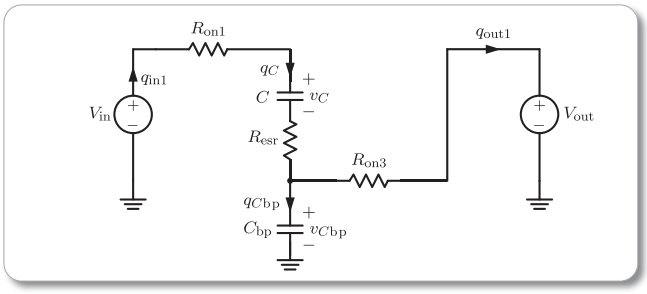
$$\mathbf{q}_2 = \mathbf{C}\mathbf{v}(t_1 + t_2) - \mathbf{v}(t_1) = -\mathbf{q}_1 \tag{22}$$

where the last equality holds because of charge conservation.

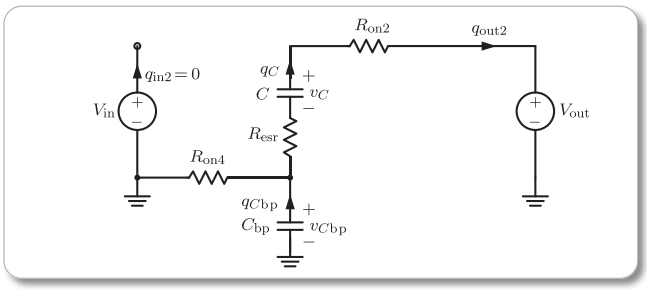
Knowing the capacitor charges in (21) and (22) for an SC converter topology, the input and output charges, and thereby the input and output currents in each switching state can be calculated. Finally, the input and output powers are determined to compute the efficiency. The following shows how the state space model framework can be applied on the 2:1 SC converter.

B. 2:1 SC Converter Model

The state space model framework is applied on the 2:1 SC converter from Fig. 1 with the equivalent circuits in the charging



(a)



(b)

Fig. 5. 2:1 SC converter equivalent circuits in (a) charging state and (b) discharging state include the switch on-state resistances $R_{\mathrm{on}1-4}$, the capacitor equivalent series resistance R_{esr}, and the parasitic bottom plate capacitor C_{bp}.

and the discharging states are shown in Fig. 5. In the equivalent circuits, each switch is replaced by an on-state resistance $R_{\mathrm{on}1-4}$ when on and an open circuit when off, and the flying capacitor model includes its equivalent series resistance R_{esr} and the bottom plate capacitor C_{bp} connected to the ground. The input and output nodes are modeled as ideal dc voltage sources.

The application of the KVL and KCL put into the form of (15) yields the system matrices

$$\mathbf{C} = \begin{pmatrix} C & 0 \\ 0 & C_{\mathrm{bp}} \end{pmatrix}, \qquad \mathbf{i} = \begin{pmatrix} i_C \\ i_{C\mathrm{bp}} \end{pmatrix}$$

$$\mathbf{v} = \begin{pmatrix} v_C \\ v_{C\mathrm{bp}} \end{pmatrix}, \qquad \mathbf{u} = \begin{pmatrix} V_{\mathrm{in}} \\ V_{\mathrm{out}} \end{pmatrix}$$

$$\mathbf{E}_1 = \begin{pmatrix} R_{\mathrm{on}1} + R_{\mathrm{esr}} & 0 \\ -R_{\mathrm{on}3} & R_{\mathrm{on}3} \end{pmatrix}$$

$$\mathbf{E}_2 = \begin{pmatrix} R_{\mathrm{on}2} + R_{\mathrm{esr}} & 0 \\ R_{\mathrm{on}4} & -R_{\mathrm{on}4} \end{pmatrix}$$

$$\mathbf{F}_1 = \begin{pmatrix} 1 & 1 \\ 0 & 1 \end{pmatrix}, \quad \mathbf{F}_2 = \begin{pmatrix} 1 & 1 \\ 0 & -1 \end{pmatrix}$$

$$\mathbf{G}_1 = \begin{pmatrix} -1 & 0 \\ 0 & -1 \end{pmatrix}, \quad \mathbf{G}_2 = \begin{pmatrix} 0 & -1 \\ 0 & 0 \end{pmatrix}.$$

Now the state space model can be applied to calculate the capacitor charges in (21) and (22). Using Fig. 5, the output and input charge in each state for the 2:1 SC converter can be found as

$$q_{\mathrm{out}1} = q_C - q_{C\mathrm{bp}} \tag{23}$$

$$q_{\mathrm{in}1} = q_C \tag{24}$$

$$q_{\mathrm{out}2} = q_C \tag{25}$$

$$q_{\mathrm{in}2} = 0 \tag{26}$$

and the total average output current over a full switching period becomes

$$I_{\mathrm{out}} = \frac{q_{\mathrm{out}1} + q_{\mathrm{out}2}}{t_1 + t_2} = (2q_C - q_{C\mathrm{bp}}) f_{\mathrm{sw}}. \tag{27}$$

Note that if $q_{C\mathrm{bp}} = 0$, the output current expression in (27) reduces to the expression derived in (7). Likewise, the total average input current is

$$I_{\mathrm{in}} = \frac{q_{\mathrm{in}1} + q_{\mathrm{in}2}}{t_1 + t_2} = q_C f_{\mathrm{sw}}. \tag{28}$$

Hence, only the output current in (27) is affected by the parasitic bottom plate capacitance through the dependence on $q_{C\mathrm{bp}}$, whereas the input current in (28) is unaffected since it does not depend on $q_{C\mathrm{bp}}$.

Using (27) and (28), the total efficiency of the 2:1 SC converter can be calculated as

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{V_{\mathrm{out}} I_{\mathrm{out}}}{V_{\mathrm{in}} I_{\mathrm{in}}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} \left(2 - \frac{q_{C\mathrm{bp}}}{q_C}\right). \tag{29}$$

As can be seen, if C_{bp} is neglected, then $q_{\mathrm{Cbp}} = 0$, and the efficiency in (29) reduces to the ideal SC converter efficiency in (8) for $M = 1/2$. Additionally, it is seen from (29) how $q_{C\mathrm{bp}}$ directly influences the efficiency of the 2:1 SC converter.

To port this analysis to the equivalent model from Fig. 4, the resistances can directly be determined as

$$R_{\mathrm{eq}} = \frac{MV_{\mathrm{in}} - V_{\mathrm{out}}}{I_{\mathrm{out}}} = \frac{\frac{1}{2}V_{\mathrm{in}} - V_{\mathrm{out}}}{(2q_C - q_{C\mathrm{bp}}) f_{\mathrm{sw}}} \tag{30}$$

$$R_{\mathrm{bp}} = \frac{MV_{\mathrm{in}}}{\frac{1}{M} I_{\mathrm{in}} - I_{\mathrm{out}}} = \frac{\frac{1}{2}V_{\mathrm{in}}}{q_{C\mathrm{bp}} f_{\mathrm{sw}}} \tag{31}$$

where $M = 1/2$ is the voltage conversion ratio.

To demonstrate the model framework's successful application to more complex conversion ratios, the state space model is in [19] applied on a 3:2 voltage conversion ratio SC converter. Furthermore, although the transition states (deadtimes) between the charging and the discharging states are left out of the analysis, [13] shows how the state space model can be extended to more states. To include the transition states would require the circuit in Fig. 1 to be analyzed in those states similarly as is done in Fig. 5. The outcome would be two additional sets of matrices along with additional matrix multiplication operations similar to (18)–(20). This additional analysis is, as stated earlier, left out for simplicity.

C. Model Verification

The state space model framework of the 2:1 SC converter is verified against simulations using the MATLAB Simulink

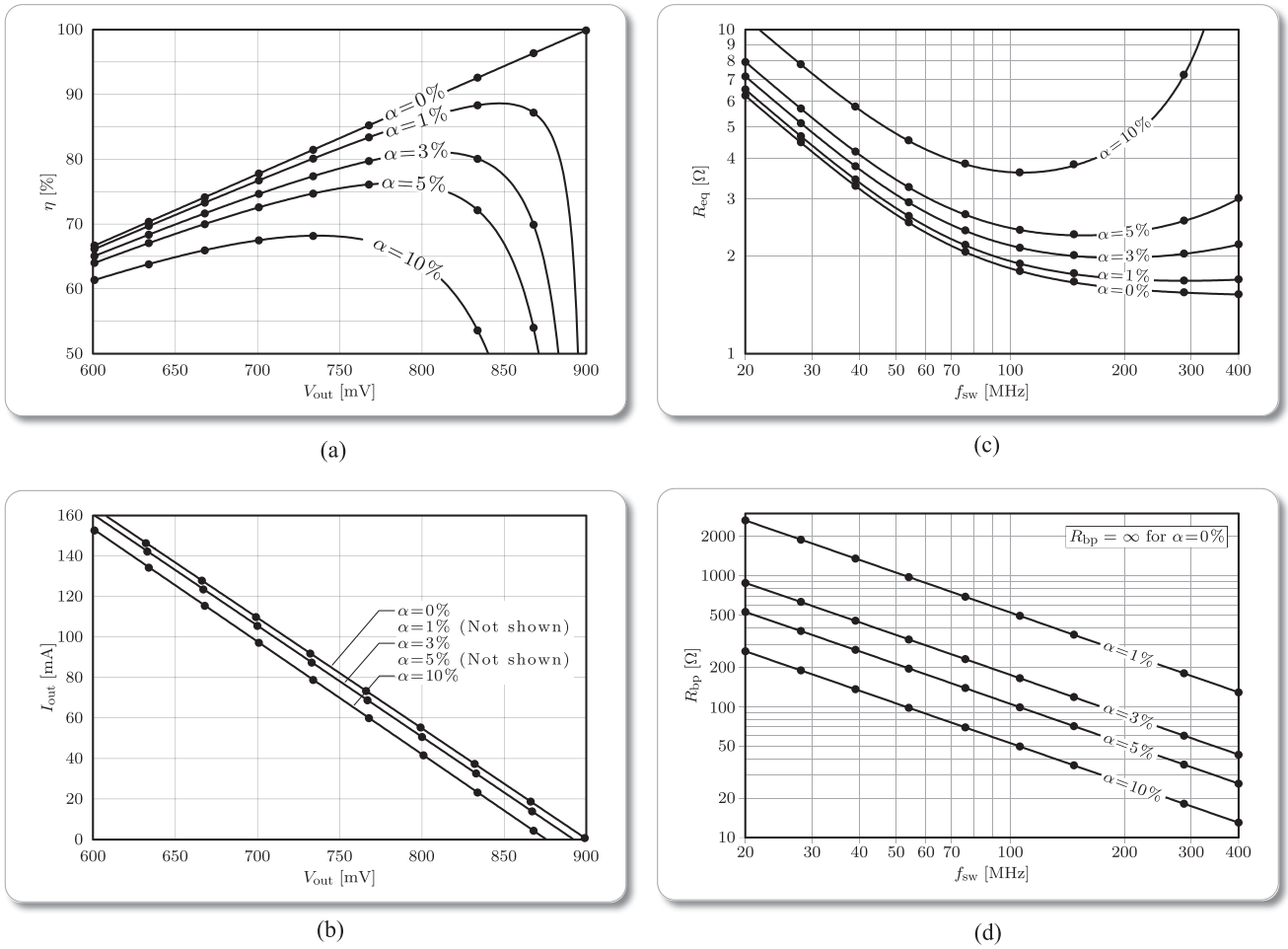


Fig. 6. Verification of (a) efficiency, (b) output current, (c) equivalent output resistance, and (d) equivalent bottom plate resistance resulting from the state space model framework. The MATLAB Simulink simulation results (dots) match the model results (lines) for various values of $\alpha = C_{\rm bp}/C$. The switching frequency is 100 MHz for (a) and (b), the output voltage is 850 mV for (c) and (d). The input voltage is 1.8 V for all plots.

environment. For the verification, an example design with $V_{\rm in} = 1.8\,{\rm V}$, $R_{\rm on1-4} = R_{\rm esr} = 0.5\,\Omega$, and $C = 2\,{\rm nF}$ is selected. For output voltage sweeps, the switching frequency is arbitrarily chosen to equal $f_{\rm sw} = 100\,{\rm MHz}$, and for switching frequency sweeps, the output voltage is arbitrarily chosen to equal $V_{\rm out} = 850\,{\rm mV}$.

Typically, the ratio of the bottom plate capacitance to the flying capacitance is denoted as

$$\alpha = \frac{C_{\rm bp}}{C}. \tag{32}$$

The value of α depends both on the semiconductor process and the on-chip capacitor technology.

The model results for various values of α are shown as solid lines in Fig. 6. The MATLAB Simulink simulation results are shown as dots to verify the model results. As can be seen, the state space model framework is able to accurately capture the influence of the bottom plate capacitor on the converter's steady-state operation and efficiency. In the following, the model results excluding ($\alpha = 0\%$) and including ($\alpha > 0\%$) the switching losses associated with $C_{\rm bp}$ are discussed. Although the discussion focuses on the 2:1 SC converter, the key learnings apply to other SC converter topologies as well.

1) Model Results for $\alpha = 0\%$: When $\alpha = 0\%$, the ideal efficiency shown in Fig. 6(a) approaches 100% as the output voltage approaches $V_{\rm in}/2 = 900\,{\rm mV}$. However, at this output voltage, the output current shown in Fig. 6(b) approaches $0\,{\rm mA}$. Hence, the SC converter theoretically has 100% efficiency at $V_{\rm out} \to V_{\rm in}/2$ but with $I_{\rm out} \to 0\,{\rm mA}$. For output voltages below half the input voltage, the ideal efficiency decreases linearly with decreasing output voltage following (8), and current is delivered to the load, i.e., $I_{\rm out} > 0\,{\rm mA}$ for $V_{\rm out} < 900\,{\rm mV}$.

The equivalent output resistance $R_{\rm eq}$ shown in Fig. 6(c) exhibits the well known $1/f_{\rm sw}$ behavior at low switching frequencies and a constant behavior at high switching frequencies. These switching frequency regions are the SSL and FSL shown in Fig. 3. When disregarding $C_{\rm bp}$, $R_{\rm bp}$ in Fig. 6(d) is an open.

2) Model Results for $\alpha > 0\%$: When $\alpha > 0\%$, the efficiency shown in Fig. 6(a) drops when the output voltage approaches $V_{\rm in}/2 = 900\,{\rm mV}$. This is because the switching losses associated with the parasitic bottom plate capacitor become comparable to the output power for output voltages close to the ideal voltage ratio. The output current is shown in Fig. 6(b),

and it is low for output voltages approaching 900 mV. Furthermore, for any given output voltage, the overall efficiency and the output current are reduced when switching losses are included.

For the equivalent output resistance $R_{\rm eq}$ shown in Fig. 6(c), the inclusion of switching losses has a direct impact on the minimum resistance, and thereby highest efficiency, achievable. The upward bend at high switching frequencies is a result of taking the parasitic bottom plate capacitor into account. For the equivalent resistance in (9), the charge $q_{C\rm bp}$ of the bottom plate capacitor subtracts from the charge of the flying capacitor q_C. Hence, $q_{C\rm bp}$ affects $R_{\rm eq}$ for $\alpha > 0\%$ by 1) an overall increase at any switching frequency and 2) an upward bend at high switching frequencies where $q_{C\rm bp}$ become comparable to q_C. These effects are not captured by existing modeling frameworks [12], [13], [17]. Furthermore, Fig. 6(d) shows that there exists an optimum switching frequency (minimum $R_{\rm eq}$) to operate the SC converter, and that this optimum switching frequency is a function of α.

The bottom plate resistance $R_{\rm bp}$ is shown in Fig. 6(d). From the equivalent circuit in Fig. 4, $R_{\rm bp}$ sinks a current ($I_{\rm bp}$) that would otherwise have been delivered to the output, thereby, affecting both the efficiency and the output current of the converter.

D. Device Models

To prepare the SC converter state space model framework presented previously for a Pareto optimization, the device models for the transistors and the capacitor must be defined. A32 nm SOI CMOS technology, which features the deep trench capacitor, is used for this design. The deep trench capacitor can facilitate high efficiency and high power density on-chip SC converters [2], [3], [18], [22]. Although it has a low bottom plate capacitance compared to other integrated capacitor technologies, the bottom plate is still there and should be accounted for by applying the model framework developed above. This especially applies for applications, such as the target application of high-performance microprocessor power delivery, where high efficiency and high power density are primary concerns.

The simplified transistor model, which is equivalent for both NMOS and PMOS transistors, and the deep trench capacitor model are shown in Fig. 7. The transistor model consists of the on-state resistance $R_{\rm on}$ and the input and output capacitances $C_{\rm iss}$ and $C_{\rm oss}$, respectively. Only the width for the thin-oxide transistors is considered, since the transistor length is fixed in this semiconductor technology. The transistor on-state resistance and input and output capacitors depend on several parameters and are generally nonlinear with voltage and temperature. Although the nonlinear voltage dependence plays a role, it is disregarded in the parameter extractions for simplicity. Having the extracted parameters tabulated, an expression is found using least-square fitting. The capacitor model consists of the capacitance C, equivalent series resistance $R_{\rm esr}$, and parasitic bottom plate capacitor $C_{\rm bp}$. To accurately capture the nonlinear dependences of both the transistors and the capacitor, the converter is later simulated using hardware-correlated models in the Cadence design environment.

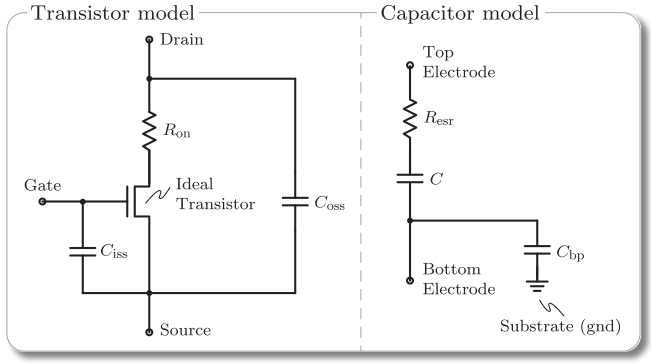


Fig. 7. Simplified transistor and deep trench capacitor models used for the Pareto optimization procedure.

A simple thermal model is considered for the parameter extractions. For the application of 2D microprocessor power delivery, the converter is integrated on the same die as the microprocessor load. Therefore, assuming a high converter efficiency, the microprocessor, and not the converter losses, dictates the die temperature, and thereby the operating temperature of the converter. For this reason, the parameters are extracted for one temperature corresponding to the maximum allowable temperature of 85°C for a microprocessor core.

For the transistor on-state resistance, a drain current of $I_{\rm d} = 20$ mA with a gate–source voltage of $V_{\rm gs} = 900$ mV is applied. The extracted on-state resistance is then least-mean-square fitted using

$$R_{\rm on}(T_w) = \frac{1}{p_1 T_w} \tag{33}$$

where T_w is the transistor width, and p_1 is a fitting coefficient [25]. Using an ac analysis, the input capacitance $C_{\rm iss}$ is extracted with the drain and source terminals shorted. Similarly, the output capacitance $C_{\rm oss}$ is extracted with the gate and source terminals shorted. The two capacitances are then least-mean-square fitted using

$$C_{\rm iss}(T_w) = p_2 T_w \tag{34}$$

$$C_{\rm oss}(T_w) = p_3 T_w \tag{35}$$

where p_2 and p_3 are fitting coefficients.

The extracted parameters and the resulting fitted expressions as a function of transistor width T_w are shown in Fig. 8. Note that although T_w is given in millimeters, the transistor layout uses an array of many smaller sized transistor units in parallel to form the actual transistor.[1] As seen, the fitted functions are able to accurately capture the transistor parameters over a wide range of transistor widths. The fitting parameters p_{1-3} used in the extracted transistor parameter functions (33)–(35) are listed in Table I.

For the deep trench capacitor, the model is linear, so the capacitance scales linearly with the number X_C of unit capacitors

[1]This is equivalent to having a transistor with a large number of fingers.

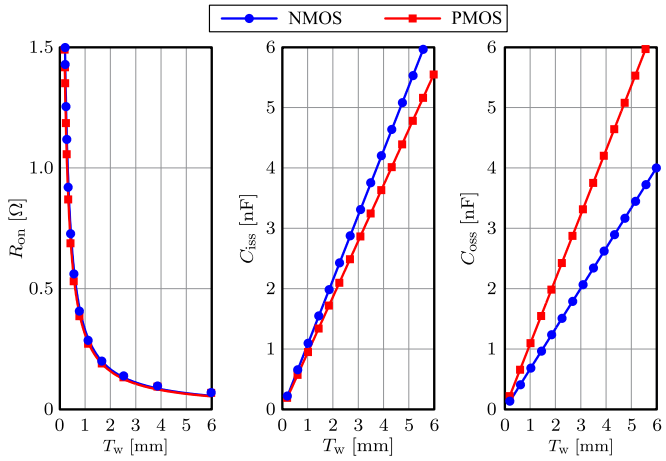


Fig. 8. Extracted transistor parameters (dots) and resulting fitting functions (lines) for both NMOS and PMOS thin-oxide transistors at 85 °C in the 32 nm semiconductor technology.

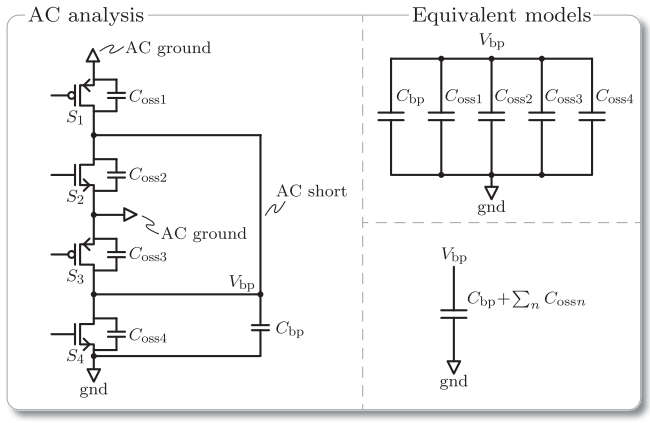


Fig. 9. Applying an ac analysis to the 2:1 SC converter power stage allows to determine the modified bottom plate capacitance, which includes both C_{bp} and the $C_{\mathrm{oss},1-4}$ of the transistors.

TABLE I
FITTING COEFFICIENTS FOR THE EXTRACTED TRANSISTOR PARAMETER FITTING FUNCTIONS

	p_1 [$\mathrm{m^{-1}\,\Omega^{-1}}$]	p_2 [$\mathrm{m^{-1}\,F}$]	p_3 [$\mathrm{m^{-1}\,F}$]
NMOS	3002	$1.07 \cdot 10^{-9}$	$0.67 \cdot 10^{-9}$
PMOS	3165	$0.93 \cdot 10^{-9}$	$1.07 \cdot 10^{-9}$

TABLE II
EXTRACTED PARAMETERS FOR THE DEEP TRENCH CAPACITOR

	C_{unit} [pF]	$R_{\mathrm{esr,unit}}$ [Ω]	α [%]
Deep trench	1.94	288	1.57

considered. Hence

$$C(X_C) = C_{\mathrm{unit}} X_C \tag{36}$$

where C_{unit} is the capacitance of a deep trench capacitor unit. Likewise, the equivalent series resistance R_{esr} of the deep trench capacitor is

$$R_{\mathrm{esr}}(X_C) = \frac{R_{\mathrm{esr,unit}}}{X_C}. \tag{37}$$

The extracted parameters for the deep trench capacitor are listed in Table II. Since X_C is an integer number, the parameters of the deep trench capacitor are discretized. However, as will be seen in Section V, X_C is large enough that the discretization is not an issue.

In an ac analysis, the output capacitances of the transistors connecting to a flying capacitor are effectively in parallel with the parasitic bottom plate capacitor C_{bp}. Hence, the modified parasitic bottom plate capacitance ratio α', which includes the output capacitances of the connecting transistors, needs to be determined and used in the state space model framework from the aforementioned. In Fig. 9, an ac analysis is applied to the 2:1 SC converter power stage. The input and output nodes are ac ground, and the flying capacitor is assumed to be large enough to be considered an ac short. Hence, all transistor output capacitances are effectively in parallel with the bottom plate capacitor. From Fig. 9, the modified bottom plate capacitance ratio becomes

$$\alpha' = \frac{C_{\mathrm{bp}} + \sum_n C_{\mathrm{oss}n}}{C} \tag{38}$$

where index n refers to the transistors S_n that connect to the flying capacitor C. For more complex SC converter topologies containing several flying capacitors and transistors, the transistor output capacitors can be added to the corresponding flying capacitors based on a similar ac analysis of the converter topology. Whether a general framework for adding the transistor output capacitors to the corresponding flying capacitors for any SC converter topology exists is left for future work.

IV. PARETO OPTIMIZATION PROCEDURE

Pareto optimization is a method to identify the best performing converter in a given design space [20]. The specifications together with a model of the converter are required. Each parameter within the limits of the design space is swept individually, resulting in a dataset where each point represents a full converter design and its performance. Analyzing the dataset can reveal the efficiency and power density Pareto front, representing the highest achievable efficiency for a given power density.

A flowchart of the SC converter Pareto optimization procedure is depicted in Fig. 10. The inputs to the procedure are the SC converter topology governed by M and the electrical specifications V_{in}, V_{out}, and I_{out}. For a given SC converter topology, the design space $\boldsymbol{X}$ contains m SC converter designs. Each set $\boldsymbol{x}_i \in \boldsymbol{X}$, where $i = \{1, 2, \ldots, m\}$ consists of 1) the number $\boldsymbol{X_C}$ of unit capacitors for each flying capacitor and 2) the transistor width $\boldsymbol{T_w}$ for each transistor in the power stage. The design space is shown in vectorial form to allow for different sizes of capacitors and/or transistors in the power stage. However, both the capacitors and transistors, respectively, may all be of equal size. Furthermore, a range $f_{\mathrm{sw}} = [f_{\mathrm{sw},1}, f_{\mathrm{sw},2}, \ldots f_{\mathrm{sw,max}}]$ of

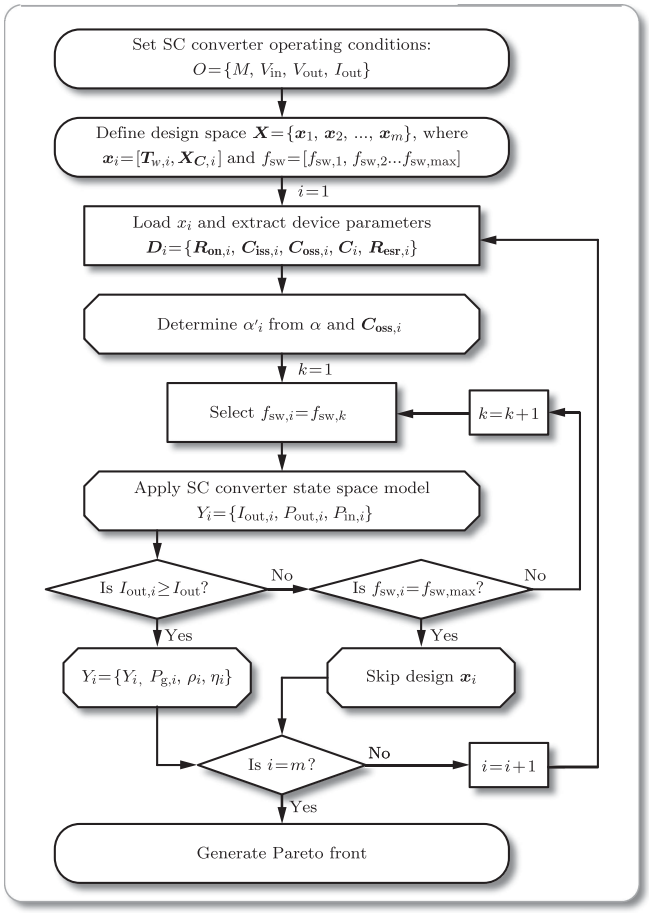


Fig. 10. Flowchart of the SC converter Pareto optimization procedure, which is based on the state space model framework presented in this paper.

allowable switching frequencies is specified. Finally, the area A_C per unit capacitor and the area A_T per unit transistor width are determined from the device layouts. They, together with a fixed area for the gate driver circuit, are used to estimate the power density for a design.

To begin the Pareto optimization procedure, the first set $\boldsymbol{x}_1$ $(i = 1)$ is loaded and the extracted device parameters are determined using the fitting functions presented in Section III-D. The modified parasitic bottom plate capacitance ratio α' is then estimated using (38). Thereafter, the first $f_{\mathrm{sw},1}$ $(k = 1)$ switching frequency is selected from the predefined switching frequency range, and the state space model is used to evaluate the electrical performance of the i'th design. If the evaluated output current $I_{\mathrm{out},i}$ meets (or, due to the discretization of the design space parameters, slightly exceeds) the output current specification I_{out}, the design and its performance are stored and further processed in the subsequent step in the flowchart. However, if $I_{\mathrm{out},i}$ does not meet the output current specification I_{out}, the next $k = k + 1$ switching frequency in the range is selected and the design is reevaluated using the state space model framework. This inner switching frequency loop continues until $I_{\mathrm{out},i} \geq I_{\mathrm{out}}$ is satisfied. If the maximum switching frequency is reached, i.e., if $f_{\mathrm{sw},i} = f_{\mathrm{sw,max}}$, and the design still does not satisfy $I_{\mathrm{out},i} \geq I_{\mathrm{out}}$, the i'th design is skipped and the next design $i = i + 1$ is loaded and evaluated.

TABLE III
ELECTRICAL SPECIFICATIONS AND DESIGN SPACE FOR THE 2:1 SC CONVERTER DESIGN

Parameter	Value
M	$1/2$
V_{in}	1.8 V
V_{out}	830 mV
I_{out}	20 mA
X_C	$100 \ldots 5000$
T_w	$100\ \mu\mathrm{m} \ldots 5000\ \mu\mathrm{m}$
f_{sw}	$10\ \mathrm{MHz} \ldots 300\ \mathrm{MHz}$
A_C	$5.129 \cdot 10^{-6}\ \mathrm{mm}^2$
A_T	$0.322 \cdot 10^{-6}\ \mathrm{mm}^2 / \mu\mathrm{m}$

Since the transistor gate losses are not included in the state space model, the gate losses for the transistors in the power stage of the i'th design, which satisfies $I_{\mathrm{out},i} \geq I_{\mathrm{out}}$, are estimated using

$$P_{\mathrm{g},i} \approx \sum_n C_{\mathrm{iss}n,i} V_{\mathrm{gs}n,i}^2 f_{\mathrm{sw},i} \tag{39}$$

where index n refers to each transistor in the power stage, $C_{\mathrm{iss}n,i}$ the input capacitance, and $V_{\mathrm{gs}n,i}$ the gate–source voltage of the n'th transistor, respectively. The efficiency and power density of the i'th converter, therefore, becomes

$$\eta_i = \frac{P_{\mathrm{out},i}}{P_{\mathrm{in},i} + P_{\mathrm{g},i}} \tag{40}$$

$$\rho_i = \frac{P_{\mathrm{out},i}}{A_i} = \frac{P_{\mathrm{out},i}}{N_T A_T T_{w,i} + N_C A_C X_{Ci}} \tag{41}$$

where N_T and N_C are the number of transistors and capacitors in the power stage, respectively.

The Pareto front is generated when all designs in the design space have been evaluated. The optimal design can then be selected based on a tradeoff between efficiency and power density. The chosen design is thereafter implemented in the Cadence design environment, which features hardware-correlated device models, for fine tuning of the design.

V. 2:1 SC CONVERTER DESIGN

The electrical specifications and parameter design space for the 2:1 SC converter design are listed in Table III. The transistor area A_T includes the last stage of the gate driver buffer (to be discussed in Section V-B) and power grid margin to give a more realistic transistor area estimation than simply the active transistor area. Although T_w represents the width of each transistor in the power stage, PMOS transistors are 15% wider than NMOS transistors following a design rule recommendation, but this is not a strict requirement.

The SC converter Pareto optimization procedure developed previously is applied on the 2:1 SC converter. The resulting Pareto front is shown in Fig. 11. A design with a reasonable tradeoff between efficiency and power density is selected and

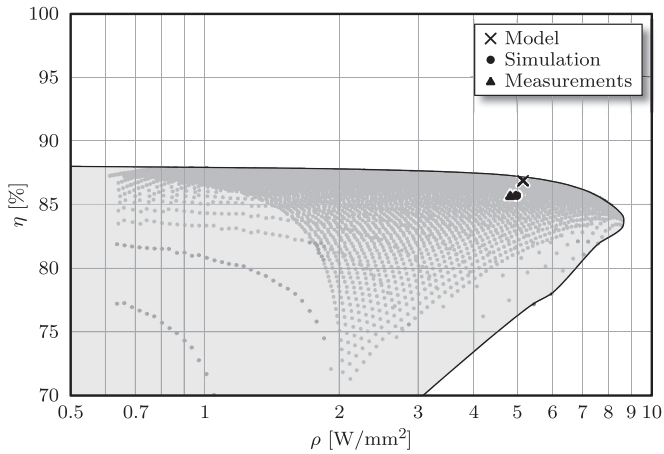


Fig. 11. Resulting Pareto fronts of the optimization procedure for 2:1 SC converter. The cross represents chosen design point, the dot marks the simulated results of the complete converter schematic, and the triangle marks the measurement results.

TABLE IV
SELECTED PARETO-OPTIMIZED DESIGN FOR THE SC CONVERTER HARDWARE IMPLEMENTATION

Parameter	2:1 SC Design
X_C	400
T_w	650 µm
f_{sw}	100 MHz
I_{out}	19.6 mA
η	86.9%
ρ	5.1 W/mm²

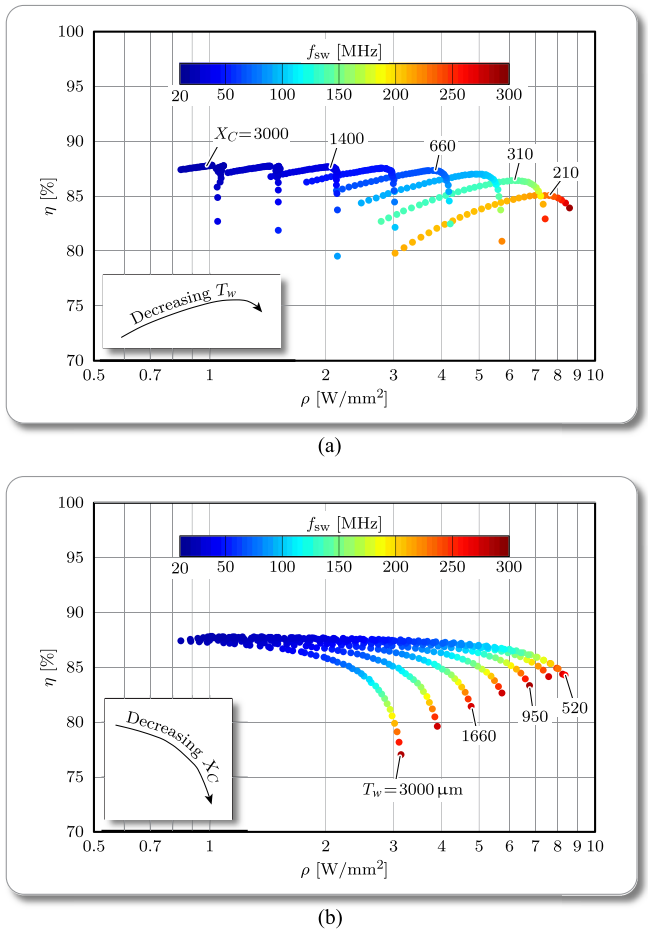


Fig. 12. Design space investigation showing how the design space parameters X_C, T_w, and f_{sw} affect the efficiency and power density of the 2:1 SC converter.

marked by the cross on the Pareto front. The design and its performance are listed in Table IV.

The selected design is implemented in the Cadence design environment for simulations using hardware-correlated models and for layout of the final converter. The simulated efficiency and power for the complete converter schematic are shown as the dot in Fig. 11. As seen, there is good agreement between the modeled and simulated performances. The slightly lower efficiency is attributed to the losses of the gate driver (discussed in Section V-B), which have not been included in the model. The slightly lower power density result is attributed to the fact that the converter area estimation is based on a 100% area utilization of the transistors and capacitors. However, the final layout has a lower area utilization due to layout constraints, thereby affecting the area estimation. The measured results, which are presented and discussed in Section VI, are seen to be in good agreement with the in Cadence simulated results.

In Fig. 12, the design space, which is used to generate the Pareto front in Fig. 11, is investigated in more detail. This investigation is used to get insight into how the design space parameters affect the efficiency and power density of the converter. Compared to the analytical equations from [17] [obtained by applying the R_{eq} sum approximation in (12)], the state space model does not result in simple equations that can provide direct insight into how the circuit parameters (X_C, T_w, f_{sw}) influence the converter performance simply by expecting the expressions. However, by analyzing the resulting data sets of the Pareto optimization procedure, these insights can anyhow be investigated, and this without applying any approximation to R_{eq}. From Fig. 12, the following is concluded.

1) The flattening of the efficiency at low power densities can be attributed to the decrease in switching frequency, and thereby decreasing switching losses. For low switching frequencies, switching losses are low, and the converter losses are primarily governed by conduction losses, which from (8) follow directly from the specified input and output voltages, i.e., independent of switching frequency.
2) The increase in switching frequency allows for the highest power density results, but the efficiency bends downwards due to increased switching losses.
3) It can be seen that the maximum power density is achieved with the lowest transistor width T_w. The minimum transistor width of 520 µm is higher than the minimum value of 100 µm from the design space in Table IV. The designs having $T_w < 520$ µm are not shown, since they result in lower efficiency designs that are not part of the Pareto front.

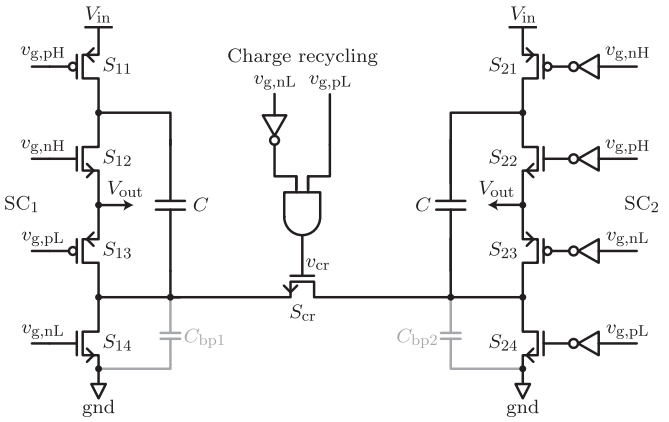


Fig. 13. Implemented 2:1 SC converter power stage with charge recycling. The power stage is split into two power stages, $\rm SC_1$ and $\rm SC_2$, that enable the implementation of the charge recycling circuit to reduce the switching losses associated with the parasitic bottom plate capacitors, $C_{\rm bp1}$ and $C_{\rm bp2}$, shown in gray.

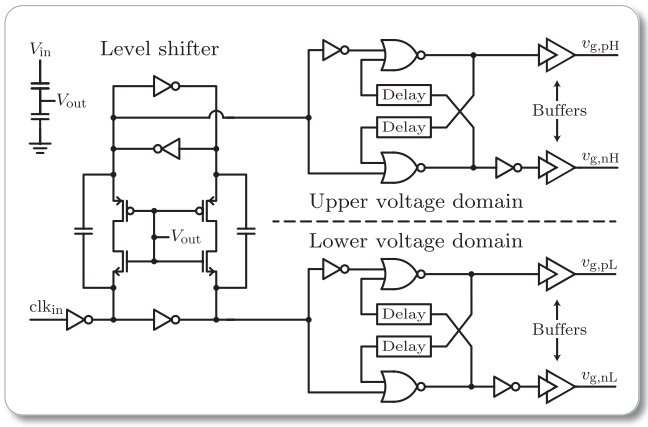
4) It can be seen that the maximum power density is achieved with the lowest number of unit capacitors X_C. The minimum number of capacitors of 210 is higher than the minimum value of 100 from the design space in Table IV. The designs having $X_C < 210$ do not fulfill the output current specification.

A. Power Stage With Charge Recycling

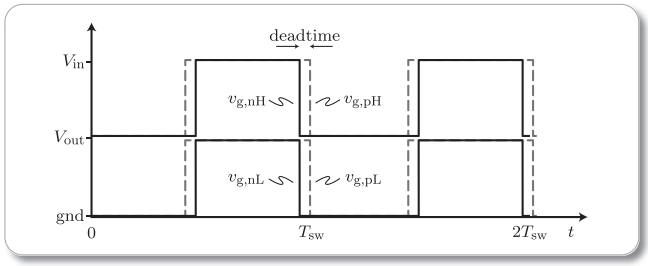
As discussed in Section III, the parasitic bottom plate capacitor significantly influences both the output current and efficiency of the converter. However, techniques to recycle the charge on the parasitic bottom plate capacitor before it is discharged to ground exist [12], [26]. For this reason, the implemented SC converter power stage features a charge recycling circuit that reduces switching losses associated with the parasitic bottom plate capacitor.

The implementation of the 2:1 SC converter power stage with charge recycling is shown in Fig. 13. To design the charge recycling circuit, the power stage is split into two power stages, $\rm SC_1$ and $\rm SC_2$. The two power stages are, as seen by the swapping of the gate signals, interleaved such that $\rm SC_1$ is in the charging state when $\rm SC_2$ is in the discharging state, and vice versa. By the end of $\rm SC_1$'s charging state, $C_{\rm bp1}$ is charged to $V_{\rm out}$ and $C_{\rm bp2}$ is discharged. During the following deadtime interval, the charge recycling transistor $S_{\rm cr}$ is turned on, and charge from $C_{\rm bp1}$ is recycled to $C_{\rm bp2}$. When $\rm SC_2$'s charging state ($\rm SC_1$'s discharging state) begins, it will require less energy to charge $C_{\rm bp2}$ to $V_{\rm out}$ and less energy is lost when $C_{\rm bp1}$ is discharged to ground. In the next deadtime interval, which occurs after $\rm SC_2$'s charging state, charge is recycled from $C_{\rm bp2}$ to $C_{\rm bp1}$.

Simulations show that the efficiency gain when using the charge recycling circuit in this technology is in the order of 0.5 to 1 percentage points. Although this is not a huge efficiency improvement, the efficiency boost comes at a very simple circuit design and a small additional chip area.



(a)



(b)

Fig. 14. The gate driver is designed in a stacked voltage domain since the 1.8 V input voltage is higher than the 1.2 V maximum allowable blocking voltage of the transistors in the 32 nm technology: (a) gate driver transistor level schematic, which consists of a level shifter and two identical nonoverlapping clock circuits (latches) that generate the deadtime interval in each voltage domain, (b) output level-shifted gate signals with deadtime.

B. Stacked Voltage Domain Gate Driver

Since the thin-oxide transistors in the 32 nm SOI CMOS technology cannot tolerate a voltage higher than 1.2 V, special care has to be taken considering an input voltage of 1.8 V. Hence, the gate driver, which generates the gate signals for the power transistors in Fig. 13, has to ensure that no single transistor is exposed to overvoltage.

The gate driver implementation and its output gate signals are shown in Fig. 14. The transistor level schematic, which is shown in Fig. 14(a), employs a stacked voltage domain, where the upper voltage domain driving S_{x1} and S_{x2} is supplied between $V_{\rm in}$ and $V_{\rm out}$ and the lower voltage domain driving S_{x3} and S_{x4} is supplied between $V_{\rm out}$ and ground (gnd). The input clock $\rm clk_{in}$ is externally supplied in the lower voltage domain. Therefore, a level shifter circuit is implemented to shift the input clock to the upper voltage domain. In each voltage domain, the clock signal is passed through a latch with built-in delay (nonoverlapping clock) to generate a deadtime interval between the clock edges to avoid shoot-through currents in the power stage transistors. The delay units, which determine the duration of the deadtime interval, consist of an even number of logic inverters. Tapered buffers are inserted after the deadtime circuits to provide sufficient drive strength to turn the power transistor on and off. The output waveforms of the gate driver are shown in Fig. 14(b). The

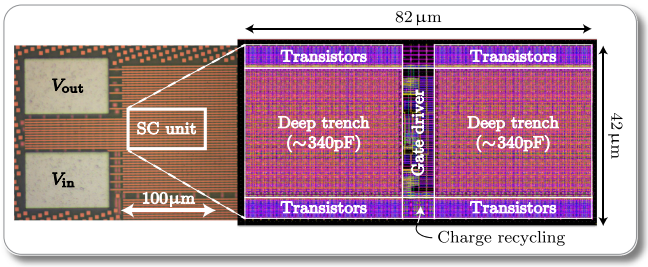


Fig. 15. Chip photo with magnified layout view of the implemented 2:1 SC converter. The input clock and ground pads are not shown. The total active converter area is $0.00344\,\text{mm}^2$.

deadtime is designed to match the requirements of the charge recycling circuit discussed in the previous subsection.

Special care has to be taken to ensure start-up of the stacked voltage domain gate driver. If the output voltage is not sustained, some transistors may be exposed to the full input voltage. Simulations show that the converter starts up without overvoltage when the load is disconnected. The reason is that the impedances of the power stage in Fig. 13 and gate driver in Fig. 14 in both voltage domains are very similar, thereby providing a close to equal voltage divider. If needed, decoupling the input voltage with stacked capacitors that are tapped at the output voltage, as shown top left in Fig. 14(a), provides extra margin for a safe startup.

VI. Experimental Results

The system overview of the implemented 2:1 SC converter directly follows the transistor level schematics of the 2:1 SC converter power stage with charge recycling shown in Fig. 13 and the stacked voltage domain gate driver shown in Fig. 14. Discrete resistors, which are attached external to the chip, act as load for the converter. Since there is no on-chip output decoupling capacitor in this design, the output decoupling is also connected external to the chip, and a larger than required capacitance of 33 nF is added to the measurement setup to ensure a negligible output voltage ripple. This enables a good characterization of the on-chip SC converter performance. However, it should be noted that the required output decoupling capacitance can be drastically reduced, or even omitted, by employing interleaving [21], [22], [27]–[29]. For this reason, the output decoupling capacitor is excluded in the power density estimations.

A chip photo of the on-chip 2:1 SC converter design with magnified layout view is shown in Fig. 15. From the converter design listed in Table IV, the two deep trench capacitors are laid out using $X_C = 400$ deep trench capacitor units. The four zones with transistors each contain an NMOS and PMOS transistor pair having a total transistor width of $T_w = 650\,\mu\text{m}$. Each transistor is laid out with 1300 fingers (small transistor units in parallel), resulting in $0.5\,\mu\text{m}$ width per finger. Furthermore, the converter is laid out in a symmetrical fashion, which is compatible with the possibility of interleaving several SC converter units to lower the output voltage ripple and increase output power. The total active converter area, which includes the gate driver and the charge recycling circuits, is $0.00344\,\text{mm}^2$. The

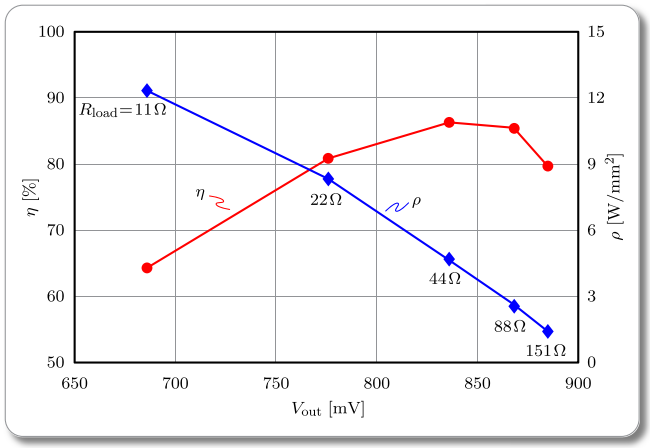


Fig. 16. Efficiency and power density over output voltage measured with the annotated load resistances. The switching frequency is 100 MHz and the input voltage is $V_{\text{in}} = 1.8\,\text{V}$.

flying capacitors accounts for 65%, the power stage transistors and charge recycling for 26%, and the gate driver for 9% of the total converter area.

A. Measured Efficiency and Power Density

Measurements are carried out using GBB PicoProbe needles on the unpackaged chip die mounted on a probe station. The input and output currents are measured using Keithley 2400 series Sourcemeters, and the on-chip input and output voltages are measured on Kelvin contacts using an Agilent 34970 Data Acquisition/Switch Unit.

In Fig. 16, the measured efficiency and power density over output voltage at $f_{\text{sw}} = 100\,\text{MHz}$ are shown. The maximum efficiency point is 86% at $4.6\,\text{W/mm}^2$ power density. Operating the converter at voltages below the minimum efficiency point (830 mV) results in a linear decrease in efficiency, but at the same time an increase in power density. These characteristics are in agreement with the modeling results discussed in Section III-C. There is seen to be a good match when comparing the efficiency and power density results with the estimated performance from the Pareto optimization procedure shown in Fig. 11.

In Fig. 17, the corresponding efficiency and power density for each measurement point acquired are mapped to the $\eta - \rho$ plane. Each point, therefore, represents a different output voltage, switching frequency, and load resistance value, and all points for a given input voltage illustrate the entire performance landscape of the converter. The performance landscape for three different input voltages are shown in gray scale. Fig. 17 serves to illustrate the tradeoff between efficiency and power density. For instance for $V_{\text{in}} = 1.8\,\text{V}$, power densities of more than $10\,\text{W/mm}^2$ can be achieved at below 75% efficiencies, whereas efficiencies above 85% can be achieved at power densities below $5\,\text{W/mm}^2$. The maximum efficiency can be seen to be independent of the input voltage, since also the output voltage at the maximum efficiency point changes leading to a constant ratio $V_{\text{out}}/V_{\text{in}}$, which from (8) results in a constant efficiency. However, the maximum power density that can be achieved

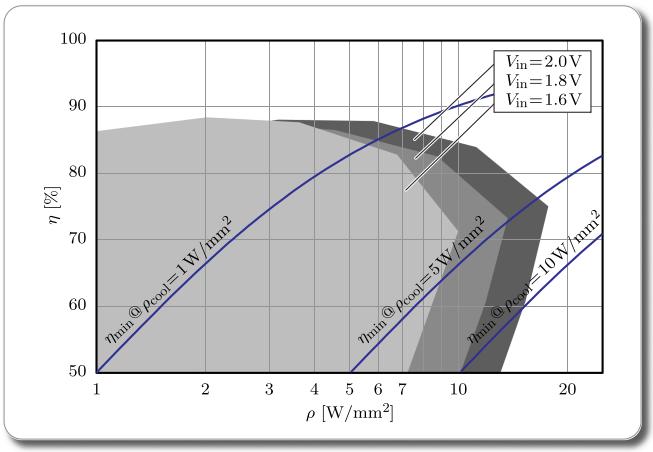


Fig. 17. Envelope of the highest efficiency per power density measured with different input voltages. The minimum efficiency required to fulfill cooling requirements are superimposed for three different cooling power densities illustrating that cooling must be taken into account for high power density on-chip SC converters.

increases with the input voltage since the higher output voltage over the fixed load resistor results in a higher output power for the same converter area. The decrease in efficiency at low power density levels is a result of limited parameter ranges of the measurement setup.

Cooling requirements may become an issue for very high power density designs since also the power loss density will be high, especially when operated in high power density regions of the performance landscape where efficiency is low. With a cooling power density of $\rho_{\mathrm{cool}} = P_{\mathrm{loss}}/A$ that can be effectively cooled by the chosen cooling technology, the minimum converter efficiency η_{min} can be expressed as

$$\eta_{\mathrm{min}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{loss}}} = \frac{P_{\mathrm{out}}/A}{P_{\mathrm{out}}/A + P_{\mathrm{loss}}/A} = \frac{\rho}{\rho + \rho_{\mathrm{cool}}} \quad (42)$$

where P_{loss} is the total power loss and A is the area of the converter. Evaluating the aforementioned expression, the minimum efficiency requirements for three different cooling power densities are added to Fig. 17. For $V_{\mathrm{in}} = 1.8\,\mathrm{V}$, it is seen that a cooling power density of minimum $5\,\mathrm{W/mm^2}$ is required to operate the converter in the entire operating region of interest. If the cooling power density is below $5\,\mathrm{W/mm^2}$, the converter's allowed operating region must be limited accordingly. From [30], a cooling power density of more than $7\,\mathrm{W/mm^2}$ can be achieved using ultrathin manifold microchannel heat sinks. Hence, cooling of the on-chip SC converter is considered manageable using this or similarly performing cooling technologies.

VII. Conclusion

Existing model frameworks for SC converters do not take the effect of the parasitic bottom plate capacitance C_{bp} into account. Therefore, a state space model framework that accurately accounts for the switching losses associated with the parasitic bottom plate capacitance is presented. The model framework can be applied to any SC converter topology. The state space model framework is verified with MATLAB Simulink simulations, and it is investigated how C_{bp} directly impacts both the operation and the efficiency of the converter.

A Pareto optimization procedure for SC converters based on the state space model framework is developed. The Pareto optimization procedure uses extracted device parameters from hardware-correlated models in the design space. A model of the 2:1 SC converter is developed, and the Pareto optimization procedure is carried out to select the optimum converter parameters.

With the availability of high-density deep trench capacitors, a 2:1 SC converter with charge recycling is implemented. A stacked voltage domain gate driver is designed to support the 1.8 V input voltage since the maximum allowable blocking voltage of the thin-oxide transistors in the 32 nm SOI CMOS technology is $1.2\,\mathrm{V}$. A maximum efficiency of 86% at $4.6\,\mathrm{W/mm^2}$ power density is measured, thereby proving the feasibility of on-chip SC converters for granular microprocessor power delivery.

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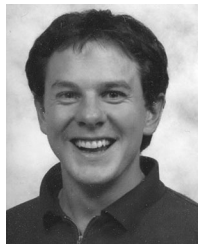

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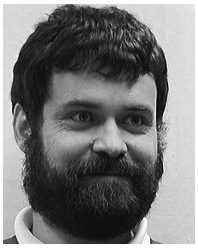

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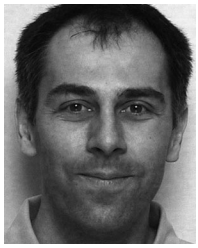

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