3-Φ SiC/GaN Converter Systems

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3-Φ SiC/GaN Converter Systems ... There is No Boogeyman Under the Bed

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3-Φ SiC/GaN Converter Systems

... BUT Lots of Opportunities & Some Challenges ;-)
Outline

- Introduction
- Performance Trends
- 10x – Technologies / Concepts
- Research Results
- Conclusions

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3 Research Fellows

ETH Zürich

Power Electronic Systems Laboratory
Research Scope

- Explore the Limits / Create New Concepts / Push the Envelope
- Maximize Technology Utilization
- Enable New Applications
Market Pull / Technology Push
Required Performance Improvements

- Power Density \([\text{kW/dm}^3]\)
- Power per Unit Weight \([\text{kW/kg}]\)
- Relative Costs \([\text{kW/} \$]\)
- Relative Losses \([\%]\)
- Failure Rate \([\text{h}^{-1}]\)

Environmental Impact...

- \(\text{kg}_{\text{Fe}} / \text{kW}\)
- \(\text{kg}_{\text{Cu}} / \text{kW}\)
- \(\text{kg}_{\text{Al}} / \text{kW}\)
- \(\text{cm}^2_{\text{Si}} / \text{kW}\)

State-of-the-Art

- Weight
- Volume
- Losses
- Failure Rate
- Costs
- Time-to-Market

- Connected Cognitive Power Electronic Systems \(\rightarrow\) Power Electronics 4.0
S-Curve of Power Electronics

- Power Electronics 1.0 → Power Electronics 4.0
- Identify “X-Concepts” / “Moon-Shot” Technologies
- 10x Improvement NOT Only 10% !

Performance

- Super-Junct. Techn. / WBG
- Digital Power Modeling & Simulation
- Power MOSFETs & IGBTs
- Circuit Topologies
- Microelectronics
- Modulation Concepts
- Control Concepts

SCRs / Diodes
Solid-State Devices

1958

2015

2025
3-Φ Variable Speed Drive Inverter Systems

State-of-the-Art Future Requirements

Source: PowerAmerica
Variable Speed Drive (VSD) Systems

- Industry Automation / Robotics
- Material Machining / Processing – Drilling, Milling, etc.
- Compressors / Pumps / Fans
- Transportation
- etc., etc.

... Everywhere!

• 60...70 % of All Electric Energy Used in Industry Consumed by VSDs
State-of-the-Art

- Mains Interface / 3-Φ PWM Inverter / Cable / Motor — Large Installation Space / Complicated
- Conducted EMI / Radiated EMI / Reflections on Long Motor Cables / Bearing Currents

- High Performance @ High Level of Complexity / High Costs (!)

Source: FLUKE
Surge Voltage Reflections

- Long Motor Cable $l_c \geq \frac{1}{2} t_r v$
- Short Rise Time of Inverter Output Voltage
- Impedance Mismatch of Cable & Motor $\rightarrow$ Reflect. @ Motor Terminals / High Insul. Stress

$\rightarrow \ dv/dt- \ OR \ Full$-Sinewave Filtering / Termination & Matching Networks etc.
Motor Bearing Currents

- Switching Frequency CM Inverter Output Voltage → Motor Shaft Voltage
- Electrical Discharge in the Bearing (“EDM”)

Cond. Grease / Ceram. Bearings / Shaft Grndg Brushes / dv/dt- OR Full-Sinewave Filters

Source: www.est-aegis.com

Source: BOSCH
VSD Inverter - Future Requirements

- “Non-Expert” Installation / “Sinus-Inverter” OR Motor-Integrated Inverter
- Low Losses & Low HF Motor Losses
- Low Volume & Weight
- Wide Output Voltage Range
- High Output Frequencies

Main “Enablers” → SiC/GaN Power Semiconductors & Adv. Inverter Topologies
X-Technology #1

Wide Bandgap Power Semiconductors
Si vs. SiC

- Si-IGBT / Diode → Const. On-State Voltage, Turn-Off Tail Current & Diode Reverse Recovery Current
- SiC-MOSFET → Massive Loss Reduction @ Part Load BUT Higher $R_{th}$

6x Si-IGBT 6x Si-Diode

6x SiC-MOSFET

1200V 100A
Die Size: 98.8mm$^2$ + 39.4mm$^2$

1200V 100A
Die Size: 25.6mm$^2$

Space Saving of >30% on Module Level (!)
**Low $R_{\text{DS(on)}}$ High-Voltage Devices**

- **Higher Critical E-Field of SiC → Thinner Drift Layer**
- **Higher Maximum Junction Temperature $T_{J,\text{max}}$**

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>GaAs</th>
<th>4H/6H-SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$ (eV)</td>
<td>1.12</td>
<td>1.4</td>
<td>3.0-3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>$E_C$ (M/V/cm)</td>
<td>0.25</td>
<td>0.3</td>
<td>2.2-2.5</td>
<td>3</td>
</tr>
<tr>
<td>$\mu_n$ (cm²/Vs)</td>
<td>1350</td>
<td>8500</td>
<td>1000-1000</td>
<td>1000</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>11.9</td>
<td>13</td>
<td>10</td>
<td>9.5</td>
</tr>
<tr>
<td>$V_{\text{sat}}$ (cm/s)</td>
<td>$1 \times 10^7$</td>
<td>$1 \times 10^7$</td>
<td>$2 \times 10^7$</td>
<td>$3 \times 10^7$</td>
</tr>
<tr>
<td>$\lambda$ (W/cmK)</td>
<td>1.5</td>
<td>0.5</td>
<td>3-5</td>
<td>1.3</td>
</tr>
</tbody>
</table>

$R_{\text{on}} = \frac{4V_n^2}{\varepsilon \mu_n E_C^3}$

For 1kV:

<table>
<thead>
<tr>
<th>Material</th>
<th>$W$ ($\mu$m)</th>
<th>$N_D$ ($\text{cm}^{-3}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>100</td>
<td>$10^{14}$</td>
</tr>
<tr>
<td>SiC</td>
<td>10</td>
<td>$10^{16}$</td>
</tr>
</tbody>
</table>

$R_{\text{on,SiC}} \approx \frac{1}{300} R_{\text{on,Si}}$

- **Massive Reduction of Relative On-Resistance → High Blocking Voltage Unipolar Devices**
Si vs. SiC Conduction Behavior

- Si-IGBT → Const. On-State Voltage Drop / Rel. Low Switching Speed,
- SiC-MOSFETs → Resistive On-State Behavior / Factor 10 Higher Sw. Speed

1200V 100A
Die Size: 98.8 mm² + 39.4 mm²
Source: Infineon

1200V 100A
Die Size: 25.6 mm²
Source: Cree

- Efficiency Characteristic Considering Only Conduction Losses
Si vs. SiC Switching Behavior

- **Si-IGBT**  →  Const. On-State Voltage Drop / Rel. Low Switching Speed,
- **SiC-MOSFETs**  →  Resistive On-State Behavior / Factor 10 Higher Sw. Speed

**Si-IGBT**
- Const. On-State Voltage Drop
- Rel. Low Switching Speed

**SiC-MOSFETs**
- Resistive On-State Behavior
- Factor 10 Higher Sw. Speed

1200V 100A
Die Size: 98.8mm² + 39.4mm²

Source: Infineon

1200V 100A
Die Size: 25.6mm²

Source: Cree

**Extremely High** \(\frac{di}{dt}\) & \(\frac{dv}{dt}\)  →  Challenges in Packaging / EMI / Motor Insulation / Bearing Currents

Source: Cree
Challenges
Circuit Parasitics

- Extremely High $di/dt$
- Commutation Loop Inductance $L_s$
- Allowed $L_s$ Directly Related to Switching Time $t_s$ →

$$L_s \leq \frac{\alpha U_i}{I_L} = \alpha t_s \frac{U_i}{I_L}$$

- Advanced Packaging & Parallel Interleaving for Partitioning of Large Currents
Si vs. SiC EMI Emissions

- Higher $dv/dt$ → Factor 10
- Higher Switching Frequencies → Factor 10
- EMI Envelope Shifted to Higher Frequencies

$f_s = 10\text{kHz}$ & $5\text{kV/\mu s}$ for (Si IGBT)

$f_s = 100\text{kHz}$ & $50\text{kV/\mu s}$ for (SiC MOSFET)

- Higher Influence of Filter Component Parasitics & Couplings → Advanced Design
Inverter Output Filters

dv/dt-Filters
Full-Sinewave Filters
Passive | Hybrid | Active dv/dt-Limitation

- **Passive** – Damped LC-Filter $f_C > f_S$
- **Hybrid** – Undamped LC-Filter & Multi-Step Sw. Transition
- **Active** – Gate-Drive Based Shaping of Sw. Transients

- $f_{sw} = 16\text{kHz}$
- $t_F = t_d = 130\text{ns}$
- $f_C = 2.4\text{ MHz}$

- Connection to DC-Minus & CM Inductor $\rightarrow$ Limit CM Curr. Spikes / EMI / Bearing Currents
Comparison of $dv/dt$-Filtering Techniques (1)

- **Passive Concept**
  1. LCR-Filter
  2. Clamped LC-Filter

- **Hybrid Concept (3f$_S$)**
  1. LC-Filter
  2. Multi-Step Switching

- **Active Concept**
  1. Miller Capacitor
  2. Gate Curr. Control

**Output Voltage Waveforms**
- $V_{DC} = 800V$, $P_{out} = 10kW$, $6kV/us$

**Example Waveforms**
- $L = 3.8\mu H$
  - $C = 2.7nF$
  - $R = 19\Omega$
- $L = 4.1\mu H$
  - $C = 1.3nF$

**1200V SiC / 16mΩ**
- $C_M = 120pF$
Comparison of dv/dt-Filtering Techniques (2)

- **Comparative Evaluation of Passive & Active Concept**

  - **Losses / Power Density** – $V_{DC} = 800V$, $P_{out} = 10kW$, $f_{sw} = 16kHz$, 1200V SiC-MOSFETs (16mΩ)
Inverter Systems w/ Sinusoidal Output Voltages
ZVS/TCM Operation

- Sinusoidal Output Voltage
- ZVS of Inverter Bridge-Legs
- High Sw. Frequency & TCM \(\rightarrow\) Low Filter Inductor Volume

- Only 33% Increase of Transistor Conduction Losses Compared to CCM (!)
- Very Wide Switching Frequency Variation
TCM $\rightarrow$ B-TCM

- Very Wide Switching Frequency Variation of TCM $\rightarrow$ B-TCM

- TCM $\rightarrow$ B-TCM — 10% Further Increase of Transistor Conduction Losses
B-TCM → S-TCM

- Sinusoidal Switching Boundaries → S-TCM
- Adaption for Low Output Power Considering $f_{sw,max} = 140$ kHz

- $TCM \rightarrow S-TCM \approx 10\%$ Further Increase of Transistor Conduction Losses
**Remark**

**Residual ZVS Losses**

- Overlap of $u_{gs}$ & Channel Current $i_{ch}$ @ High $I_{sw} > I_k$
- Temporary Turn-on Due to $u_{gs,i} > u_{th}$

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- "Kink" Current $I_k$ Dependent on Inner & Outer Gate Resistance & $u_{g,n}$

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There are graphs showing voltage and current profiles, and a diagram illustrating the conditions and calculations for residual ZVS losses.
CCM & 2-Stage Full-Sinewave Output Filter (1)

- Sinewave Output & IEC/EN 55011 Class-A
- Low-Loss Active Damping of 1st Filter Stage — Neg. Cap. Current Feedback
- 2kW / 400V DC-Link 3-Φ 650V GaN Inverter ($I_{M}=5A$), $f_{out,\text{max}} = 500\text{Hz}$
- Sw. Frequency $f_s = 100\text{kHz}$

$\Rightarrow$ Evaluation of Optimized Inductors — Soft Sat. Toroidal Iron Powder Cores

$L_1=200\mu\text{H (OD57S)} / C_1=2.5\mu\text{F} / L_2=25\mu\text{H (OD20S)} / C_2=2.5\mu\text{F} / L_d=33\mu\text{H} / R_d=5.6\Omega$

$\Rightarrow$ Low-Loss Active Damping of 1st Filter Stage — Neg. Cap. Current Feedback

Sw. Frequency $f_s = 100\text{kHz}$

$f_{c,1}=7\text{kHz}$

$f_{c,2}=20\text{kHz}$
CCM & 2-Stage Full-Sinewave Output Filter (2)

- **Exp. Verification** — 650V E-Mode GaN Systems Transistors (50mΩ)
- **Sw. Frequency** $f_S = 100$kHz, **Efficiency** ≈98%
- **200mm x 250mm**

- Stationary Motor Phase Curr. /Voltage @ 2.5Nm & $f_{out} = 250$Hz
- Speed Increase from Standstill to $n = 3000$rpm in 60ms
CCM & 2-Stage Full-Sinewave Output Filter (3)

- Modification of Output Filter Structure
- Elimination of Direct Cap. Coupling Between Output and Noisy (!) DC+ (Due to $R_{DC}$)
- For Opt. $i_C$-Feedback $C_1$ Realized Using $\approx$Linear Kemet KC-Link

- Modified Filter $\rightarrow$ Compliance to EMI Standard EN55011 Class-A
X-Technology #2

Multi-Level / -Cell Converters & Modularity
Multi-Level (ML) Converter Scaling

- 1/N Reduction of Blocking Voltage → Lower $R_{DS(on)}$ Semiconductors ($R_{on} \sim U_B^2$)
- Eff. Increase of Sw. Frequency → $f_{sw,eff} = N f_{sw}$ (f_{sw} ... Individual Device)
- Larger Chip Area and/or Smaller $L_o$

$N = \# \text{ of Levels } -1$

$D-FOM = D-FOM(U_{dc}/N) \rightarrow \text{Results in } ML-\text{Performance (X-FOM) Dependent on } N$
Functional Principle of ML-Converters

- 3-Level Flying Cap. (FC) Converter Requires No Connection to DC-Midpoint
- Involves All Switches in Voltage Generation → Eff. Doubles Device Sw. Frequency
- FC Voltage Balancing Possible also for DC Output

- Risk of Transistor Overvoltage for Steep $U_{dc}$ Changes
Scaling of ML Bridge-Leg Concepts

- Reduced Ripple @ Same (!) Switching Losses
- Lower Overall On-Resistance @ Given Blocking Voltage $\rightarrow 1+1=2$ NOT $2^2=4$ (!)
- Application of LV Technology to HV

\[ \Delta i_{\text{max},N} = \frac{1}{N^2} \Delta i_{\text{max},N=1} \]

\[ \frac{\Delta U_{\text{c,max},N}}{U} = \frac{\pi^2 (f_0)^2}{32 f_s} \frac{1}{N^3} \]

- Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy
X-FOM of ML-Bridge-Legs

- Quantifies Bridge-Leg Performance of N-Level FC Converters

$N = \# \text{ of Levels} - 1$

- Compared to 2-Level Benchmark @ Same Filter Ind. Volt-Seconds

$D - \text{FOM}(U_b) = \frac{1}{R_s(U_b)C_{\text{med}}(U_b)}$

$X - \text{FOM}(U_b, N) = N \cdot D - \text{FOM}(\frac{1}{2}U_b)$

$P_{\text{semi,min,ML}} \approx \frac{1}{N^{1.2}} P_{\text{semi,min,2L}}$

$A_{\text{chip,ML}} \approx N^{1.2} A_{\text{chip,2L}}$
7-Level Flying Cap. 200V GaN Inverter (1)

- DC-Link Voltage: 800V
- Rated Power: 2.2 kW / Phase
- 99% Efficiency → Natural Convection Cooling (!)

- High Effective Sw. Frequency (6 x 30kHz = 180kHz) → Small Filter Inductor $L_o$
**7-Level Flying Cap. 200V GaN Inverter (2)**

- **DC-Link Voltage**: 800V
- **Rated Power**: 2.2 kW / Phase
- **99% Efficiency** → Natural Convection Cooling (!)

- **High Effective Sw. Frequency** (6 x 30kHz = 180kHz) → Small Filter Inductor $L_0$

---

**Efficiency (%)** vs. **$P_{rated}$ (%)**

- 7L, 800 V$_{dc}$
- 3L, 800 V$_{dc}$

**Details:**

- DC-Link Voltage: 800V
- Rated Power: 2.2 kW / Phase
- Efficiency: 99%
- Natural Convection Cooling
- High Effective Switching Frequency (6 x 30kHz = 180kHz)
- Small Filter Inductor $L_0$

---

**Notes:**

- 260 W/in$^3$
3-Φ Hybrid Multi-Level Inverter Demonstrator

- Realization of a 99%+ Efficient 10kW 3-Φ 400V rms Inverter System
- 7-Level Hybrid Active NPC Topology / LV Si-Technology

200V Si → 200V GaN Technology Results in 99.5% Efficiency
Quasi-2L/3L Flying Capacitor Inverter
Quasi-2L & Quasi-3L Inverters (1)

- Operation of N-Level Topology in 2-Level or 3-Level Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

- Schweizer (2017)

- Reduced Average dv/dt $\rightarrow$ Lower EMI / Lower Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}$/Low $S$ MOSFETs $\rightarrow$ High Efficiency / No Heatsinks / SMD Packages
Quasi-2L & Quasi-3L Inverters (2)

- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

- Schweizer (2017)

3.3kW @ 230V_{rms}/50Hz
Equiv. f_S ≈ 48kHz

3.5kW/dm³
Eff. ≈ 99%

- Reduced Average dv/dt → Lower EMI / Lower Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}$/Low $S$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages
Quasi-2L & Quasi-3L Inverters (3) - Schweizer (2017)

- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

Operation @ 3.2kW

- Conv. Output Voltage
- Sw. Stage Output Voltage
- Flying Cap. (FC) Voltage
- Q-FC Voltage (Uncntrl.)
- Output Current
- Conv. Side Current

- Reduced Average dv/dt → Lower EMI / Lower Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}$/Low $\$$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages
Ultra-Compact Power Module with Integrated Filter

650V GaN E-HEMT Technology

$f_{S,eff} = 4.8\,\text{MHz}$

$f_{out} = 100\,\text{kHz}$
Integrated Filter GaN Half-Bridge Module

- Minimization of Filter Volume by Series & Parallel Interleaving & Extreme Sw. Frequency
- Handling of DC Output Requires Flying Capacitor Approach for Series Interleaving

\[ f_{S,\text{eff}} = (M-1) \cdot f_s \]

\[ f_{S,\text{eff}} = N \cdot f_s \]

\[ M = 5 \]

\[ N = 4 \]

\[ f_{\text{out}} = f_{\text{on}} = (M-1) \cdot f_{\text{on}} \]

\[ f_{\text{on}} = N \cdot f_{\text{on}} \]

\[ v_{\text{on}} = \frac{V_{\text{in}}}{N} \]

\[ v_{\text{out}} \]

\[ V_{\text{in}} \]

\[ T_{\text{on}} \]

\[ T_{\text{off}} \]

\[ C_{\text{on}} \]

\[ C_{\text{off}} \]

\[ L \]

\[ V_{\text{in}}/\text{M} \]

\[ V_{\text{out}} \]

\[ V_{\text{out}}/\text{N} \]

\[ V_{\text{on}} \]

\[ V_{\text{off}} \]

\[ f_{\text{on}} \]

\[ f_{\text{off}} \]

\[ f_{\text{out}} \]

\[ f_{\text{in}} \]

\[ f_{\text{eff}} \]

Target: Best Combination of Multiple Levels (M) & Parallel Branches (N)
4.8MHz GaN Half-Bridge Phase Module

- **Combination of Series & Parallel Interleaving**
  - 600V GaN Power Semiconductors, $f_{sw} = 800kHz$
  - Volume of $\approx 180cm^3$ (incl. Control etc.)
  - $H_2O$ Cooling Through Baseplate

- Operation @ $f_{out}=100kHz$, $f_{S,eff}=4.8MHz$, $10kW$, $U_{dc}=800V$
**Remark**

High-BW High-CMRR Current Measurement

- **Extension of Commercial Hall Sensor** DC... $f_{Hall} = 500$kHz $\rightarrow$ DC...20MHz
- **Low-Pass & High-Pass Filter Network** Combining HF-Sensor & LF Hall-Sensor

- **Hall Sensor Bandwidth** $f_{Hall} = 1.6$MHz
- **Rogowski Coil High-Pass Corner Frequency** $f_{int} = 1$kHz
- **Low/High-Pass Filter Cross-Over Network** $f_{filter} = 24$kHz
Motor-Integrated Inverter Systems
Stacked-Multi-Cell (SMC) Inverter

- **Fault-Tolerant VSD**
- **Low-Voltage Inverter Modules**
- **Very-High Efficiency / Power Density**
- **Automated Manufacturing**

- **Rated Power** $45kW$ / $f_{out} = 2kHz$
- **DC-Link Voltage** $1kV$

- **Smart Motor / Plug & Play** $|$ **Connected / Intelligent VSD 4.0**
Motor-Integrated SMC 200V GaN-Inverter

- Rated Power: 9kW @ 3700rpm
- DC-Link Voltage: 650V...720V
- 3-Φ Power Cells: 5+1
- Outer Diameter: 220mm

- Axial Stator Mount
- 200V GaN e-FETs
- Low-Capacitance DC-Links
- 45mm x 58mm / Cell

Main Challenge — Thermal Coupling/Decoupling of Motor & Inverter
Double-Bridge (DB) Inverter

- **Comparison to Conv. 2-Level Inverter + Front-End DC/DC Boost-Stage**

  - $U_b = 40V...120V$
  - $P = 1.0kW$
  - $f_s = 300kHz$ (200V EPC GaN)
  - $f_o = 5kHz$

- **Advantages** — Lower Sw. Losses & Lower # of Filter Inductors

- $210 \text{ W/in}^3$

- $98 \text{ W/in}^3$
Turbo-Compressor-Integrated DB GaN-Inverter

- E-Mobility 5…15kW Fuel Cell Pressurized Air Supply
- 1kW Rated Power, $f_{sw}=300\mathrm{kHz}$  $| n= 280'000\text{rpm} / f_{out}= 4.6\mathrm{kHz}$
- Low EMI / Low Cabling Effort

- Integration $\rightarrow$ 2x System Power Density $| 97\% \rightarrow 98.5\%$ Inverter Efficiency
3-Φ 650V GaN Motor-Integrated Inverter

- Sigma-7F Servo Drive — Motor Integration of DC/AC Stage (TO-220 GaN)
- Distributed DC-Link System — Single AC/DC Converter / Smaller Cabinet
- 0.1 – 0.4kW / 270...324V Nominal DC-Link Voltage

- Small Size (0.4 kW @ 70 x 70x 170mm)
- Massive Saving in Cabling Effort / Simplified Installation

Source: YASKAWA
Remark: Overload Capability

- Highly Dynamic Robotics VSDs → 3x ... 5x Rated Torque for Seconds
- Small Chip Area → Low Thermal Time Constant of GaN HEMTs
- Trade-Off Between Overload Rating & Rated Power Efficiency

- 200V GaN vs. Si (Multi-Level Inverter) Comparison
X-Technology #3

Functional Integration & Synergetic Association
Motivation

- General / Wide Applicability
  - Adaption of (Load-Dependent) Supply Voltage & Motor Voltage
  - Wide Speed Range → Wide Output Voltage Range

- No Add. Converter for Voltage Adaption → Single-Stage Energy Conversion

Source: magazine.fev.com
Derivation of Buck-Boost Y-Inverter

- **Generation of AC-Voltages Using Unipolar Bridge-Legs**

- **Switch-Mode Operation of Buck OR Boost Stage** ⇒ Single-Stage Energy Conversion (!)
- **3-Φ Continuous Sinusoidal Output / Low EMI** ⇒ No Shielded Cables / No Insul. Stress
- **Standard Bridge-Legs / Building Blocks** ⇒ 1.2kV SiC MOSFETs

![Diagram of Buck-Boost Y-Inverter with unipolar bridge-legs and switch-mode operation]
Sinusoidal Modulation

- **Y-Inverter**

- **Motor Phase Voltages**

- **Const. DC Offset → Strictly Positive Output Voltages** $u_{anN}$, $u_{bnN}$, $u_{cnN}$
- **Mutually Exclusive Operation of the Half-Bridges → Low Switching Losses**
**Boost-Operation**  \( u_{an} > U_i \)

- **Phase-Module**
  
- **Motor Phase Voltages**

- **Current-Source-Type Operation**
- **Clamping of Buck-Bridge High-Side Switch** → **Quasi Single-Stage Energy Conversion**
**Buck-Operation** $u_{an} < U_i$

- **Phase-Module**

- **Motor Phase Voltages**

- **Voltage-Source-Type Operation**
- **Clamping of Boost-Bridge High-Side Switch** → **Quasi Single-Stage Energy Conversion**
Discontinuous Modulation

- **Y-Inverter**

- **Motor Phase Voltages**

- Clamping of Each Phase for 1/3 of the Fund. Period ⇒ Low Switching Losses (!)
- Non-Sinusoidal Module Output Voltages / Sinusoidal Line-to-Line Voltages
Control Structure

- Motor Speed Control

- Cascaded Current / Voltage / Current Control Loops
- Seamless Transition between Boost- & Buck-Mode → “Democratic” Control
Y-Inverter VSD

- **Demonstrator Specifications**
  - Wide DC Input Voltage Range \(\Rightarrow 400...750\)\(V_{DC}\)
  - Max. Input Current \(\Rightarrow \pm 15A\)

- Max. Output Power \(\Rightarrow 6...11\) kW
- Output Frequency Range \(\Rightarrow 0...500\)Hz
- Output Voltage Ripple \(\Rightarrow 3.2\)V Peak @ Output of Add. LC-Filter
Y-Inverter Demonstrator

- DC Voltage Range: 400...750V\textsubscript{DC}
- Max. Input Current: ± 15A
- Output Voltage: 0...230V\textsubscript{rms} (Phase)
- Output Frequency: 0...500Hz
- Sw. Frequency: 100kHz
- 3x SiC (75mΩ)/1200V per Switch
- IMS Carrying Buck/Boost-Stage Transistors & Comm. Caps & 2\textsuperscript{nd} Filter Ind.

Dimensions → 160 x 110 x 42 mm\textsuperscript{3} (245W/in\textsuperscript{3})
Y-Inverter - Measurement Results

- **Stationary Operation**

  \[ U_{DC} = 400V \]
  \[ U_{AC} = 400V_{rms} \text{ (Motor Line-to-Line Voltage)} \]
  \[ f_O = 50Hz \]
  \[ f_S = 100kHz / \text{Discontinuous PWM} \]
  \[ P = 6.5kW \]

- **Line-to-Line Output Voltage Ripple < 3.2V**
Efficiency Measurements

- **Dependency on Input Voltage & Output Power Level**

\[ U_{DC} = 400V / 600V \]
\[ U_{AC} = 230V_{\text{rms}} \text{ (Motor Phase-Voltage)} \]
\[ f_S = 100kHz \]

→ **Multi-Level Bridge-Leg Structure** for Increase of Power Density @ Same Efficiency
EMI-Limits (VSD Product Standard)

- **IEC 61800-3** → Product Standard for Variable-Speed Motor Drives
- **EMI Emission Limits** → Grid Interface (GI) and Power Interface (PI)
- **Application** → Residential (C1) or Industrial (C2)

**Grid Interface (GI)**
- Conducted EMI Limits
  - (dBμV)
  - C1: Residential (CISPR Class B)
  - C2: Industrial (CISPR Class A)

**Power Interface (PI)**
- Conducted EMI Limits
  - (dBμV)
  - C1*: C1 & Unshielded Cables > 2m (CISPR Class A + 1dBμV)

**Radiated EMI Limits**
- (dBμV/m)
- C1: Residential (CISPR Class B)
- C2: Industrial (CISPR Class A)

- **EMI-Filter Design for Unshielded Cables > 2m and Resid. Applications (Cond. & Rad.)**
**Conducted EMI-Filter**

- Separate Cond. DM & CM EMI-Filter on DC-Side & DC-Minus Ref. EMI-Filter on AC-Side

- Low Add. EMI Filter Volume — 74cm³ for Each Filter (incl. Toroid. Rad. EMI Filter)
- Total Power Density Reduces — 15kW/dm³ (740cm³) → 12kW/dm³ (890cm³)
Conducted EMI - Experimental Results

- Measurements of the Cond. EMI Noise on the AC-Side (QP, with 50Hz AC-LISN)

→ Small 80uH CM-Ind. Added on AC-Side - (3cm³ of Add. Volume = 0.5% of Converter Vol.)
→ Conducted EMI with Unshielded Motor Cable Fulfilled
Measurement of Radiated EMI-Noise (1)

- Equipment Under Test (EUT) Placed on Wooden Table with Specified Arrangement
- CM Absorption Devices (CMAD) Terminate All Cables on AC- & DC-Side (Total \( l_{\text{cable}} \approx 1.5\) m)
- Measurement of Radiated Noise with Antenna in 3m Distance

Either Open-Area Test Site (OATS) or Special Semi-Anechoic Chamber (SAC) Needed

Alternative Pre-Compliance Measurement Method
Measurement of Radiated EMI-Noise (2)

- CM-Currents NOT Returning IN THE CABLE are Dominant Source of Radiation
- Relation Between Radiated Electric Field and CM-Currents (!)

\[
E = \begin{cases} 
\frac{\mu_0 \cdot f \cdot I_{\text{cable}} \cdot I_{\text{cm}}}{r} & \frac{\lambda}{4} \leq l_{\text{cable}} \\
\frac{\mu_0 \cdot c_0}{4} \cdot \frac{I_{\text{cm}}}{r} & \frac{\lambda}{4} > l_{\text{cable}} 
\end{cases}
\]

[Fischer FCC F-33-1] up to 250MHz
\( Z_{\text{nom}} = 6.3\Omega \)

- Max. Allow. El. Field Strength of 40dBuV/m \( \rightarrow \) Max. CM-Current of 3.5μA (11dBuA)
- Current Probe Impedance of 6.3Ω (F-33-1) \( \rightarrow \) Max. Noise Volt. of 26dBuV @ Test Receiver
Radiated EMI-Filter Design

- Single-Stage HF CM-Filter on DC-Side and AC-Side
- Plug-On CM-Cores (NiZn-Ferrites) \(\rightarrow\) Low Parasitics & Good HF-Att. up to 1GHz

\[ C_{Y2,DC} \text{ (on the back)} \]

\[ L_{HF} \]

\(\rightarrow\) Additional EMI Filter Volume Already Considered with Conducted EMI Filter

\(\rightarrow\) Total Power Density Slightly Reduces — 15kW/dm\(^3\) \(\rightarrow\) 12kW/dm\(^3\)
Experimental Results - Radiated EMI

- Y-Inverter Placed in Metallic Enclosure → Emulate Housing, but UNshielded Cables (!)
- Measurement Setup → According IEC 61800-3
- Alternative Measurement Principle → Conducted CM-Current Instead of Radiation

→ Already Noticeable Noise Floor
→ HF-Emissions Well Below Equivalent EMI-Limit → Next Step: Verification Using Antenna
Current Source Inverter (CSI) Topologies

- **Phase Modular Concept** → **Y-Inverter** (Buck-Stage / Current Link / Boost-Stage)
- **3-Φ Integrated Concept** → **Buck-Stage & Current DC-Link Inverter**

→ **Low Number of Ind. Components** & **Utilization of Bidir. GaN Semicond. Technology**
3-Φ Integrated Buck-Boost CSI

- **Bidirectional/Bipolar Switches** → **Positive DC-Side Voltage for Both Directions of Power Flow**

- **Monolithic Bidir. GaN Switches** → **Factor 4 Reduction of Chip Area Comp. to Discrete Realization**

Source: Panasonic Ideas for Life
600V GaN Monolithic Bidir. Switch (M-BDS)

- **Power America Project** — Based on Infineon’s CoolGaN™ HEMT Technology ($R_{DS(on)} = 70\,\Omega$)
- **Dual-Gate Device** / **Controllability of Both Current Directions**
- **Bipolar Voltage Blocking Capability** | Normally On or Off

- Analysis of 4-Quadrant Operation of $R_{DS(on)} = 140\,\Omega$ Sample @ ±400V
3-Φ-Integrated Buck-Boost CSI

- "Synergetic" Control of Buck-Stage & CSI Stage
- 6-Pulse-Shaping of DC Current by Buck-Stage → Allows Clamping of a CSI-Phase

- Switching of Only 2 of 3 Phase Legs → Reduction of Sw. Losses by \( \approx 86\% \) (!)
3-Φ Integrated Buck-Boost CSI

- “Synergetic” Control of Buck-Stage & CSI Stage
- 6-Pulse-Shaping of DC Current by Buck-Stage → Allows Clamping of One CSI-Phase

- Operation for 30° Phase Shift of AC-Side Voltage & Current
**Future Research**

- Advanced DC/AC Topologies incl. CM-Filtering
- Extension of 2/3-PWM to Bipolar DC-Link Voltage 3-Φ AC/AC Converter
- Multi-Objective Design & Comparative Evaluation

- Partial Use of “Normally-On” Switches for Freewheeling in Case of Auxiliary Power Loss
Remark

3-Φ AC/AC Matrix Converter

- **Indirect Matrix Converter (IMC)**
  - CSI GaN M-BDS AC/DC Front-End
  - ZCS Commutation of CSI Stage @ $i_{DC}=0$
  - No 4-Step Commutation

- **Direct Matrix Converter (CMC)**
  - 4-Step Commutation
  - Exclusive Use of GaN M-BDSs

- Higher # of Switches Compared to CMC
- Lower Cond. Losses @ Low Output Voltage
- Thermally Critical @ $f_{out} \rightarrow 0$

- Thermally Critical @ $f_{out} \approx f_{in}$
3-Φ PFC Rectifier System

Synergetic Control
Matrix-Type Isolated Topology

Source: Porsche Mission E Project
Selected EV Charger Topology

- Isolated Controlled Output Voltage
- Buck-Boost Functionality & Sinusoidal Input Current
- Applicability of 600V GaN M-BDSs
- High Power Density / Low Costs

→ Conventional / Independent OR “Synergetic Control” of Input & Output Stage
Conventional vs. “Synergetic” Control

- **1/3-Modulation** → Significant Red. of Losses of the Power Switches Comp. to 3/3-PWM

- **Conduction Losses** ≈ -80%
- **Switching Losses** ≈ -70%

→ Operating Point Dependent Selection of 1/3-PWM OR 3/3-PWM for Min. Overall Losses
AC/DC Stage Transition to Full-Boost Operation

- Different Operating Regimes → Synergetic Partial-Boost Full-Boost

→ Intermediate 2/3-Operation for Limiting DC-Link Center Point Current (Low DC-Cap.)
Isolated Matrix-Type Rectifier
Isolated 3-Φ Matrix-Type PFC Rectifier (1)

- Based on Dual Active Bridge (DAB) Concept
- Opt. Modulation \( t_1 \ldots t_4 \) for Min. Transformer RMS Curr. & ZVS or ZCS
- Allows Buck-Boost Operation

- Equivalent Circuit
- Transformer Voltages / Currents
Isolated 3-Φ Matrix-Type PFC Rectifier (2)

- Efficiency $\eta = 98.9\%$ @ 60% Rated Load (ZVS)
- Mains Current $THD_i \approx 4\%$ @ Rated Load
- Power Density $\rho \approx 4kW/dm^3$

$P_0 = 8 \text{ kW}$
$U_{IN} = 400V_{AC} \rightarrow U_O = 400V_{DC}$
$f_s = 36kHz$

$\approx 99\%$

$900V / 10m\Omega$ SiC Power MOSFETs
Opt. Modulation Based on 3D Look-Up Table
3D-Packaging / Heterogeneous Integration

- **System in Package (SiP) Approach**
- **Minim. of Parasitic Inductances / EMI Shielding / Integr. Thermal Management**
- **Very High Power Density (No Bond Wires / Solder / Thermal Paste)**
- **Automated Manufacturing**

- **Future Application Up to 100kW (!)**
- **New Design Tools & Measurement Systems (!)**
- **University / Industry Technology Partnership (!)**

Source: VICOR

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**ETH Zürich**
Monolithic 3D-Integration

- GaN 3x3 Matrix Converter Chipset with Drive-By-Microwave (DBM) Technology
  - 9 Dual-Gate GaN AC-Switches
  - DBM Gate Drive Transmitter Chip & Isolating Couplers
  - Ultra Compact → 25 x 18 mm² (600V, 10A – 5kW Motor)

Source: Panasonic ISSCC 2014
- **Future Experimental Analysis**

- No Access to Inner Details / Only Terminal Waveforms Available for Measurement (!)

- Convergence of Measurement & Simulation → “Augmented Reality” Oscilloscope
  - Measured Signals & Simulated Inner Voltages/Currents/Temp. Displayed Simultaneously
  - Automatic Tuning of Simulation Parameter Models for Best Fit of Simulated/Measured Waveforms
PCB-Based 3-Port Resonant GaN DC/DC Converter

- Single Transformer & Decoupled Power Flow Control
- Charge Mode PFC → HV (250...500V) SRC DCX / Const. $f_{sw}$, Min. Series Inductance / ZVS
- Drive Mode HV → LV (10.5...15V) 2 Interleaved Buck-Converters / Var. $f_{sw}$ / ZVS
- $P = 3.6kW$

![Diagrams illustrating the converter's components and operation]

- Peak Efficiency of 96.5% in Charge Mode / 95.5% in Drive Mode

$\approx 16 \text{ kW/dm}^3$
X-Technology #5

Ceramic Capacitors
HF (NiZn) Magnetics
HF Magnetic Materials & Ceramic Capacitors

- **High Performance Factor of Low Permeability Magnetic Materials for 2...20MHz**
- **Volumetric Efficiency (\(\mu F/cm^3\)) Improvement of MLCCs Exceeds Moore's Law (!)**
- **Hybrid Ind./Cap. Converter Concepts for Min. Magnetic Energy Storage Requirements**

- **Performance Factor** \(B \cdot f\) Indicates Power Handling Capability @ Const. Loss Density & Core Volume

Source: A.J. Hanson, 2016

Source: R. Pilawa, 2017
X-Technology #6

Automated Design
Digital Twin / Industry 4.0
Digital Signal & Data Processing

- Exponentially Improving uC / Storage Technology (!)
- Extreme Levels of Density / Processing Speed
- Software Defined Functions / Flexibility
- Cont. Relative Cost Reduction

Moore's Law

- Fully Digital Control of Complex Systems
- Massive Computational Power → Fully Automated Design & Manufacturing / Industrial IoT (IIoT)
Automated Design Roadmap

- **State-of-the-Art**
  - User Defined Models and Simulation / Fragmented

- **Augmented Design**
  - Suggestion of Design Details Based on Previous Designs

- **Assisted Design**
  - Support of the User with Abstracted Database of Former Designs

- **Autonomous Design → Design 4.0**
  - Independent Generation of Full Designs for Final Expert Judgement

- **End-to-End Horizon of Modeling & Simulation**
- **Design for Cost / Volume / Efficiency Target / Manufacturing / Testing / Reliability / Recycling**

- **AI-Based Summaries → No Other Way to Survive in a World of Exp. Increasing # of Publications (!)**
Scaling Law – Power Electronics 4.0

- Metcalfe's Law
  - Moving from Hub-Based Concept to Community Concept Increases Value Exponentially (\(\sim n(n-1)\) or \(\sim n \log(n)\))
  - Automated Design / Digital Control / Digital Twin
Conclusion
Summary

- S-TCM Full ZVS Inverters
- Multi-Level/Cell Inverter Topologies
- Buck-Boost Inverter w/ Integrated Output Filter
- Inverter Motor Integration

- Low On-Resistance & High Sw. Speed SiC / GaN
- Monolithic Bidirectional GaN
- Integration of Switch / Gate Drive / Sensing / Monitoring
- SiC/GaN 4.0
S-Curve of Power Electronics

- **Power Electronics 1.0 → Power Electronics 4.0**
- Identify “X-Concepts” / “Moon-Shot” Technologies
- **10x Improvement NOT Only 10%!**

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**Key Concepts (Waves):**

1. **WBG Semiconductors**
2. **Multi-Cell/Level Concepts**
3. **Functional Integration**
4. **3D-Packaging/Integration**
5. **MLCC & HF Mag. Materials**
6. **Digitalization / IIoT**

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**Timeline:**

- **1958:** SCR / Diodes
- **2015:** Solid-State Devices
- **2025:** Super-Junct. Techn. / WBG

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**Technologies Evolution:**

- **Power MOSFETs & IGBTs**
- **Circuit Topologies**
- **Microelectronics**
- **Modulation Concepts**
- **Control Concepts**

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**Effort / Time:**

- **Emerging**
- **Established**
- **Mature**

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**Ethzürich**

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**PowerAMerica**
Comparison to “Moores Law”

- “Moore’s Law” Defines Consecutive Techn. Nodes Based on Min. Costs per Integr. Circuit (!)
- Complexity for Min. Comp. Costs Increases approx. by Factor of 2 / Year

Definition of “η*, ρ*, σ*, f_P* – Node” Must Consider Conv. Type / Operating Range etc. (!)
Future Development

- Commoditization / Standardization
- Extreme Cost Pressure (!)

“There is Plenty of Room at the Top” → Medium Voltage/Frequency Solid-State Transformers

Power-Supplies on Chip ← “There is Plenty of Room at the Bottom”

- Key Importance of Technology Partnerships of Academia & Industry
Thank you!
Appendix A

Accurate Measurement of SiC/GaN Power Semiconductor On-State & Switching Losses
On-State Voltage Measurement (1)

- **Device / Load Current / Gate Voltage / Junction Temp. → On State-Resistance $R_{DS(on)}$**

$R_{DS(on)} = \frac{v_{DS(on)}}{i_L}$

- **Decoupling High Blocking Voltage and (Very) Low On-State Voltage ($\approx 1V \ll BV_{DS}$)**
On-State Voltage Measurement (2)

- **High Accuracy** → Compensation of Decoupling Diode Forward Voltage
- **Fast Dyn. Response** → Valid Measurement 50ns After Turn-On

*Example — Dyn. $R_{DS(on)}$ of GaN HEMTs → 2x $R_{DS(on)}$ @ 100kHz - 0.6BV$_{DS}$*
Switching Loss Measurement

- **Heat-Sink Temp.-Based Transient Calorim. Method → 15 min / Measurement**

- **Case Temp.-Based Ultra-Fast Method → 15 sec / Measurement**
Example Measurement Results

- **650V GaN (ZVS)**

  - 200V Si vs. GaN (Hard-Sw. & ZVS)

- **1.2kV SiC (Hard-Sw.)**

- **200V Si vs. GaN (Hard-Sw. & ZVS)**

![Graph of Switched Voltage Slope vs. Current]

![Graph of Switching Losses vs. Current]

![Graph of Switching Losses vs. Voltage]

![Graph of Switching Losses vs. Time]
Appendix B

T-Type M-BDS Topology
Integr. Active Filter PFC Rectifier
Swiss Rectifier
Remark

T-Type PFC Rectifier Topology

- Application of 600V M-BDSs @ $U_{pn} = 800V$ in Combination w/ 1200V SiC MOSFETs
- Hard-Switching Cont. Cond. Mode (CCM) or ZVS TCM Operation

- Max. Power Density | 98.4% Efficiency @ CCM w/ $f_{sw} = 550kHz$
Non-Sinusoidal Mains Current

\( P_0 = \text{const. Required} \)

\( 3\Phi \) Unfolder Front End

\( 3^{\text{rd}} \) Harmonic Injection in Middle Phase

Basic Idea: M. Jantsch, 1997 (for PV Inv.)
IAF Rectifier Demonstrator

- Efficiency $\eta > 99.1\%$ @ 60% Rated Load
- Mains Current $THD_i \approx 2\%$ @ Rated Load
- Power Density $\rho \approx 4\text{ kW/dm}^3$

$P_D = 8$ kW
$U_N = 400\text{V}_{AC} \rightarrow U_0 = 400\text{V}_{DC}$
$f_S = 27\text{kHz}$

► SiC Power MOSFETs & Diodes
► 2 Interleaved Buck Output Stages
IAF Rectifier → Swiss Rectifier

- Controlled Output Voltage
- Sinusoidal Mains Current
- $i_y$ Def. by KCL: E.g. $i_a - i_c$

► Low Complexity
Swiss Rectifier Demonstrator

- Efficiency $\eta = 99.26\%$ @ 60% Rated Load
- Mains Current $THD_I \approx 0.5\%$ @ Rated Load
- Power Density $\rho \approx 4\text{ kW/dm}^3$

$P_0 = 8 \text{ kW}$

$U_{N} = 400\text{V}_{AC} \rightarrow U_O = 400\text{V}_{DC}$

$f_S = 27\text{kHz}$

- SiC Power MOSFETs & Diodes
- Integr. CM Coupled Output Inductors (ICMCI)
— The END —