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Full-ZVS Modulation for All-SiC ISOP-Type Isolated Front End (IFE) Solid-State Transformer

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***Abstract*—Thanks to their comparatively low system complexity, SSTs based on an isolated front end (IFE) approach are suitable for space and weight-constrained medium voltage (MV) AC to low voltage (LV) DC power supply applications, e. g., in future traction, naval, subsea or aerospace systems. The IFE approach connects series resonant isolation stages operating in the half-cycle discontinuous-conduction-mode (HC-DCM) directly to the MV AC grid in an input-series, output-parallel (ISOP) configuration, but the entire control, i. e., the shaping of the grid current for unity power factor and output voltage regulation, is carried out by a second, non-isolated conversion stage on the LV side. However, since the isolation stages do not operate with a DC but with an AC or |AC| input voltage, the transformer magnetizing current available for ZVS as well as the voltage to be switched vary over the grid period. Taking into account also component tolerances among the cascaded converter cells, this paper provides an in-depth analysis of the ZVS behavior under these conditions, and of the associated losses and EMI considerations, presenting a loss-optimal choice of the magnetizing inductance value and of the dead time (interlock time) of the isolation stages' bridge legs. A time-dependent variation of the latter to achieve ZVS over the entire grid period without an increase of the isolation stage losses is proposed. The considerations are verified at the example of the Swiss SST (S^{3}T), an all-SiC 25 kW, 6.6 kV MVAC to 400 V LVDC converter system, using a detailed simulation model, including non-linear MOSFET capacitances.**

I. Introduction

There are various high-power applications with a low-voltage (LV) DC interface that should be connected to the medium-voltage (MV) power grid. Such applications include, e. g., future rack-level power supplies for datacenters with power flow from the AC to the DC side [1], or larger PV installations, where the power flow is from the DC to the AC side, or also battery storage systems that require bidirectional power exchange with the grid. Power electronic systems that provide such MVAC to LVDC and/or LVDC to MVAC conversion by employing medium-frequency (MF) transformers for galvanic isolation are commonly referred to as solid-state transformers (SSTs). SSTs are especially well suited for applications that require an interface between a MV and a LV system in a weight and/or volume restricted environment [2], such as, e. g., in traction applications [3], but also in future naval or marine on-board MVAC or MVDC distribution systems [4], and possibly even in future all-electric aircraft [5]. In such applications, where the main motivation to employ SSTs might be to meet volume and/or weight constraints, and where added features such as reactive power compensation or active filtering are not necessarily required, SST solutions with low overall complexity are particularly interesting.

A. The IFE Approach

An SST providing these characteristics can be based on an isolated front end (IFE) approach, where a large share of the system complexity, e. g., semiconductors, measurement and control electronics, and large capacitors, can be moved to the LV side (cf. **Fig. 1** as an example) or avoided altogether when compared with the vast majority of SST topologies described in literature, which are based on an isolated back end (IBE) approach (cf., e. g., [3], [6]). Please refer to [7] for a detailed comparative analysis of the IFE and IBE approaches.

The IFE concept has been proposed first in 1985 for a traction application [8], and has then recently been applied again to traction applications [9], and in a three-phase ISOP converter system with a multi-winding transformer [10]. However, these realizations use hard-switched, non-resonant isolation stages. In contrast, already McMurray proposed the application of a series resonant converter (SRC) operated in the half-cycle discontinuous-conduction-mode (HC-DCM) in an AC-AC application using bidirectional switches back in 1969 [11], a concept that has more recently been extended to an ISOP configuration of several such isolation stages for low-complexity AC-AC SST applications by GE [12]. Finally, the combination of the two ideas has been published in 2013, where IGBT-based resonant isolation stages were arranged in an IFE ISOP configuration, similar to the topology shown in **Fig. 1**, however, with individual filter elements at each cell's AC side, and combined with a LV-side boost converter stage to provide current control and regulation of an LV DC bus voltage, which was then used to feed an inverter stage interfacing the LV AC grid [13], [14].

B. The Swiss SST (S^{3}T)

In the scope of a research program funded by the Swiss government [15], an all-SiC realization of a 25 kW IFE SST as an interface between a 6.6 kV MVAC grid and a 400 V DC load or source is investigated—the Swiss SST (S^{3}T) [7], [16]. **Fig. 1** shows the considered topology, corresponding key waveforms, and the main specifications.

The S^{3}T features an ISOP configuration of converter cells, i. e., autonomous isolation (front end) stages (aIFE). Such an aIFE stage is realized as a SRC operated in HC-DCM, which has the property of tightly coupling its terminal voltages in open-loop operation (cf. [11], [17], [18] for details). On their MV side, these aIFE cells feature a half-bridge with bidirectional switches to enable an AC input voltage, i. e., direct connection to the grid, by combining the folding of the grid voltage and the switching for the SRC operation, while the second, capacitive leg consists of two (small) resonant capacitors, C_{r1} and C_{r2}. Hence, the envelope of the transformer voltage, v_{T}, is proportional to the grid voltage, and a scaled and rectified version of the grid voltage, v_{lv}, is obtained after rectification on the secondary side—the aIFE is essentially acting as an isolated AC-|AC| converter. The input current, i_{b}, of a non-isolated |AC|-DC boost converter connected to the common LV bus of the aIFE cells can be controlled such as to be in phase with v_{lv} and of appropriate magnitude to maintain the output DC voltage at a given value. Since the aIFE does not contain significant energy storage elements, the power flow impressed by the |AC|-DC converter is directly translated to the grid, ensuring unity power factor operation. Thus, the local average value of the resonant

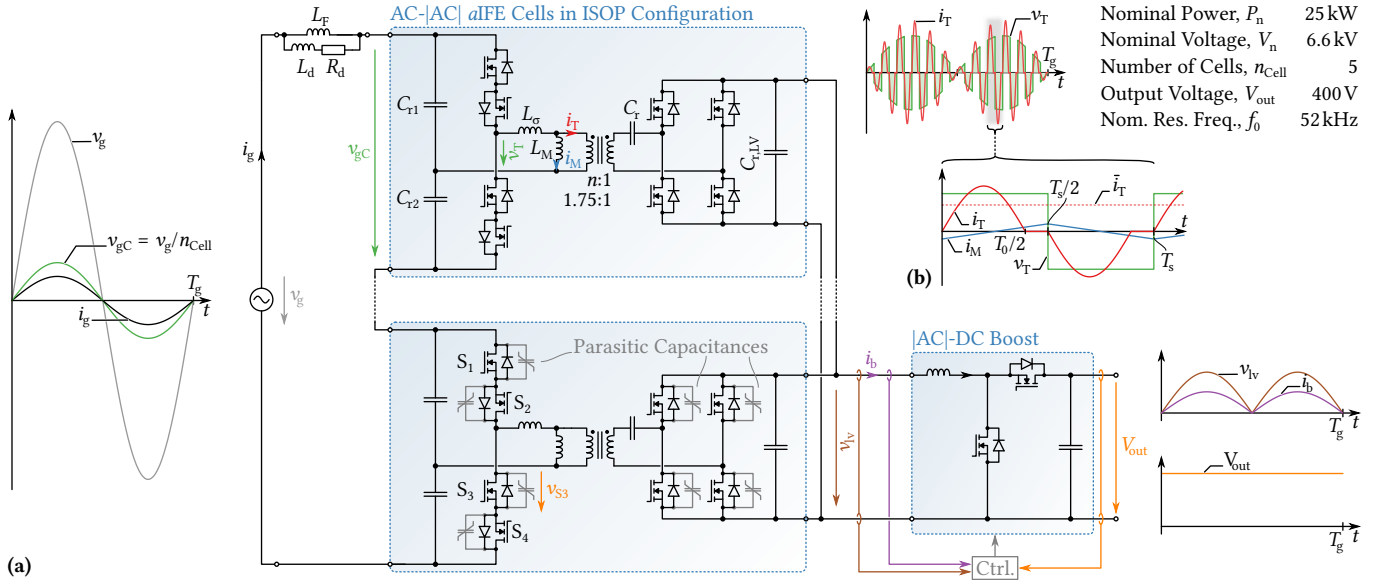

Fig. 1. Topology and key waveforms of the Swiss SST (S^{3}T), an all-SiC IFE-based solid-state transformer (SST) capable of providing bidirectional power flow with unity power factor at reduced system complexity. Note that no measurements on the MV side are required, and that C_{r1} and C_{r2}, i. e., the capacitors on floating potential, are only small resonant capacitors. Remark: only two cascaded cells of the full system comprising five cells in an input-series output-parallel arrangement (ISOP) are shown.

current pulses, $\bar{i}_T$, is proportional to the instantaneous boost inductor current, i_b (and hence also to the grid current, i_g), which can be assumed to be constant during a switching period.

C. Zero-Voltage Switching in the S^{3}T

There are two reasons to aim for zero-voltage switching (ZVS) transitions in a converter: first, switching losses can be reduced to a minimum, and second, EMI noise generated by fast (partially) hard-switched transitions can be avoided. The HC-DCM operating mode of the SRC facilitates to achieve ZVS independent of the load level, since the magnetizing current of the transformer is used to discharge and charge the switches' parasitic output capacitances during the dead time, t_d, at changes of the bridge legs' switching states (cf. **Fig. 1b**).

In conventional IBE systems, the isolation stage is operating as a DC-DC converter between two (almost) constant DC voltages. Accordingly, the envelope of the transformer voltage is (almost) constant, and thus a combination of a magnetizing inductance, L_M, (and hence a peak magnetizing current, $\hat{i}_M$) and a dead time, t_d, can be chosen such as to result in suitable ZVS performance, which has been, e. g., discussed for an IGBT-based design in [19]. In a practical realization, L_M can be adjusted by the transformer design (air gap), or an external shunt inductor may be used. This is then sufficient to ensure ZVS over the entire grid period.

However, this is quite different in the case of an IFE system, where the envelope of the switched voltage applied to the transformer is proportional to the grid voltage (cf. **Fig. 1**). Thus, the amount of magnetizing current available for ZVS varies over the grid period—but so does the voltage to be switched. Considering the non-linearity of the parasitic capacitances of power semiconductors (C_{oss} in the case of MOSFETs), which strongly increase at lower voltages, it needs to be investigated whether it is at all possible to achieve ZVS over the entire grid period, and how to choose the magnetizing inductance and the dead time accordingly. An initial analysis considering IGBTs has been presented in [13], [14], where for given magnetizing inductance and dead time a range of the grid period in which ZVS can be achieved has been identified. However, a more detailed analysis and optimization, considering not only the magnetizing inductance, but also advanced techniques such as variable dead times has not been mentioned.

Therefore, as a complement to [7], this paper provides a detailed analysis of the ZVS behavior of the S^{3}T's isolation stage, considering an optimum choice of L_M and t_d but also proposing a time-dependent variation of the dead time. First, a basic configuration consisting of only the MV side bridge leg and the magnetizing inductance is used to illustrate the basic principles in Section II, before then a full analysis and optimization based on detailed simulations of the switching transitions, including non-linear capacitance characteristics as well as the impact of tolerances of the individual converter cells' resonant tank components, is presented in Section III.

For the sake of completeness, note that similar considerations regarding dual-active bridge (DAB) converters [20] in AC-DC applications [21], i. e., with varying input voltages, have been carried out, e. g., in [22], however, relying not only on the magnetizing current but utilizing the more complex control possibilities of a DAB. Note also that literature describes various concepts of how to operate a boost converter such as used in the S^{3}T with full ZVS by using, e. g., triangular current mode [23] or clamp switches [24], [25]. Hence, a detailed description of the boost stage ZVS operation is not in the scope of this paper.

II. Basic ZVS Considerations

First, a simplified circuit consisting of only the MV side bridge leg and the magnetizing inductance, i. e., the circuit shown in **Fig. 2a**, is considered, and, without loss of generality, a switching transition from S_1 to S_3 (i. e., for $v_g > 0$ V where S_2 and S_4 are gated on permanently). The available magnetizing current and also the switched voltage vary with the input voltage of the converter cell, $v_{gC} = v_g/n_{Cell}$, as can be seen in **Fig. 3a**. In combination with a given (constant) dead time, t_d, this results in different switching transitions over the grid period as shown in **Fig. 3b-e**: in case **(b)**, the dead time is too short, i. e., $v_{S3}(t_d)$

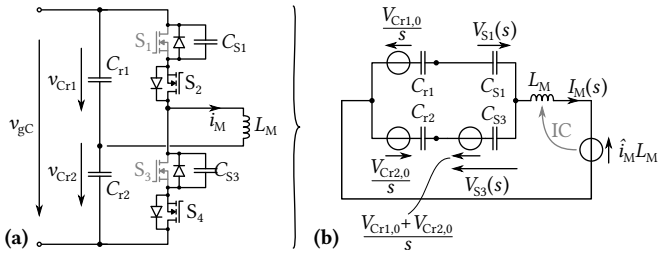

Fig. 2. **(a)** MV side bridge leg during commutation from S_1 to S_3 and **(b)** corresponding Laplace equivalent circuit, where the voltage source $\hat{i}_M L_M$ represents the initial condition of the magnetizing inductor current. Note that this circuit is valid for a simplified analysis only, because the parasitic capacitances of the LV side switches are not yet considered.

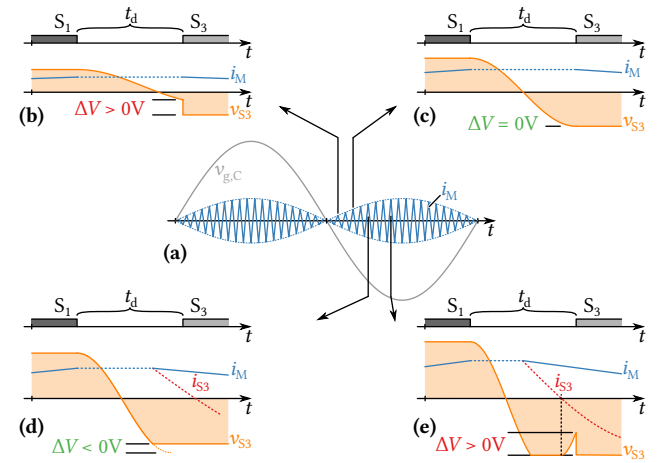

Fig. 3. **(a)** Available magnetizing current over a grid period, and **(b-e)** exemplary switching transitions with ZVS ($\Delta V \leq 0\,\mathrm{V}$) or partial ZVS ($\Delta V > 0\,\mathrm{V}$).

is still larger than zero and an incomplete ZVS transition with the remaining voltage step $\Delta V = v_{S3}(t_d)$ occurs, generating additional switching losses. Case **(c)** is the borderline case, where the ZVS transition fully completes within the dead time ($\Delta V = 0\,\mathrm{V}$), and in case **(d)**, the voltage across S_3 would swing below zero (theoretically $\Delta V < 0\,\mathrm{V}$) if it was not clamped by the anti-parallel diode of S_3. Typically, such a design with $\Delta V < 0\,\mathrm{V}$ over the entire grid period would be aimed for if ZVS operation should be guaranteed.

Finally, the ZVS transition shown in case **(e)** is so fast that the load current of the next resonant pulse, which begins to flow as soon as the anti-parallel diode of S_3 starts to conduct and therefore the MV bridge is applying a fixed voltage to the resonant tank again, reaches the magnetizing current and hence the current through S_3/D_3 changes its sign before S_3 is gated on. Consequently, the parasitic capacitance C_{S3} is charged again until finally S_3 turns on with $\Delta V > 0\,\mathrm{V}$, i. e., only a partial ZVS transition occurs.

Note that which type of transition occurs during what parts of the grid period in general depends on the chosen L_m and t_d, but also on component tolerances, etc., which will then be discussed in more detail in Section III.

Increasing the dead time and/or reducing the magnetizing inductance (and hence increasing the peak magnetizing current) would speed up the switching transitions, reducing the region within the grid period where case **(b)** appears, but on the other hand the region where case **(e)** appears could be increased (note, however, that case (e) does not necessarily appear). Also, a larger dead time corresponds to a reduction of the switching frequency, which in turn increases the rms value of

TABLE I. Additional specifications of the S^3T (cf. also **Fig. 1**).

Nom. res. freq., f_0	52 kHz	Nom. sw. freq., $f_{s,n}$	50 kHz
MV res. cap., $C_{r1,2}$	2.5 µF	Stray inductance, L_σ	10 µH
Res. Cap., C_r	5 µF	LV res. cap., $C_{r,LV}$	3.5 µH
Transf. efficiency, η_T	99.6 %	Core to Cu loss at P_n	1 : 1

the resonant current and hence load-dependent conduction losses. A larger magnetizing current causes a load-independent increase of the conduction losses. Thus, the choice of the magnetizing inductance and the dead time has to be carried out carefully in order to meet the criteria of low losses (also in part load operation) and complete ZVS over a wide range of the grid period.

A. Loss Modeling

As mentioned above, the losses of the isolation stage (the aIFE) depend on the chosen L_m, t_d, etc. Note that even though for now only a reduced circuit (cf. **Fig. 2a**) is considered, the losses are calculated for a full aIFE, i. e., including the LV side semiconductors. The specifications of the S^3T are given in **Fig. 1** and in **Tbl. I**, and Wolfspeed's upcoming 1700 V/45 mΩ and 900 V/11.5 mΩ SiC FETs are considered [26] (no paralleling, 125 °C junction temperature). Transformer losses are estimated by assuming a full-load transformer efficiency of 99.6 % with a 1:1 distribution of winding and core losses, which yields a corresponding winding resistance that allows a load-dependent modeling of the winding losses.

1) Conduction Losses (Resonant Current): The grid current, i_g, consists of a component that is in phase with the grid voltage and corresponds to the processed power, but also of a reactive component because of the MV capacitances, i. e., $i_g(t) = \hat{i}_{g,A}\sin(2\pi f_g t) + \hat{i}_{g,R}\sin(2\pi f_g t + \pi/2)$, where $\hat{i}_{g,A}$ follows from the processed power and $\hat{i}_{g,R} = \hat{v}_g \cdot (2\pi f_g C_{r1,2}/(2n_{Cell}))$. As a consequence of the half-bridge configuration employed on the MV side, the local average value of the resonant current pulse, $\bar{i}_T$, must equal twice the local average value of the active component of the grid current, $i_{g,A}$. Assuming piecewise sinusoidal current pulses, the local RMS value of the resonant current pulses becomes (please refer to [7] for detailed derivations)

$$\tilde{i}_T = i_{g,A} \cdot \frac{\pi}{\sqrt{2}} \cdot \sqrt{\frac{f_0}{f_s}}, \tag{1}$$

where f_s denotes the *effective* switching frequency, i. e,

$$f_s = \frac{1}{T_{s,n} + 2 \cdot t_d} \quad \text{with} \quad T_{s,n} = \frac{1}{f_{s,n}}. \tag{2}$$

Loss-wise, a choice of $T_{s,n} = T_0$, i. e., operation at the border to the DCM mode, would constitute an optimum. However, typically $T_{s,n}$ has to be chosen sufficiently longer in order to ensure DCM mode even in the case of component value tolerances of the resonant tank elements, which cause deviations among the different cells' resonant periods ($T_{0,i}$) in a multi-cell system. For the same reason, the case $T_{s,n} < T_0$ is not considered here, because then the ZVS behavior would become strongly dependent on the load current, worsening the issues discussed in Section III. Note also that a very long t_d increases the rms current and hence conduction and winding losses.

The LV side switches can be operated with $T_{s,lv} = k \cdot T_{s,n}$ with $k < 1$ in order to reduce conduction losses by means of active rectification. To ensure DCM operation, $T_{s,lv}$ must be sufficiently shorter than $T_{s,n}$ in order to prevent the resonant current from crossing zero. Note that a negligibly short LV diode conduction interval is assumed for the conduction loss calculations, i. e. only the FETs' on-state resistances are considered.

2) Conduction Losses (Magnetizing Current): Considering an arbitrary switching period (cf. **Fig. 1b**), v_{gC} denotes the instantaneous value of the cell's AC input voltage, which is assumed to be constant during the switching period. This voltage is applied to the magnetizing inductance during the active interval, $T_{\mathrm{on}} = T_{\mathrm{s,n}}/2$, increasing the magnetizing current to

$$\hat{i}_{\mathrm{M}} = \frac{1}{2} \cdot \frac{1}{2} \frac{v_{\mathrm{gC}}}{L_{\mathrm{M}}} \cdot T_{\mathrm{on}} \tag{3}$$

at the switching instant. Then, the local rms value of the magnetizing current becomes

$$\tilde{i}_{\mathrm{M}} = \hat{i}_{\mathrm{M}} \cdot \sqrt{f_{\mathrm{s}} \cdot \left(\frac{T_{\mathrm{s,n}}}{3} + 2 \cdot t_{\mathrm{d}} \right)}, \tag{4}$$

generating load-independent conduction losses in the MV side MOSFETs as well as in the MV transformer winding.

3) Switching Losses: The losses of an incomplete ZVS transition can be estimated based on the MOSFET's output capacitance, C_{oss}, and the remaining voltage, $\Delta V > 0\,\mathrm{V}$, according to the procedure described in [27]. Switching losses for $\Delta V \leq 0\,\mathrm{V}$, i. e., for complete ZVS transitions, are neglected.

B. Analytical Modeling of Simplified ZVS Transitions

Considering the simplified circuit consisting only of the MV side bridge and the magnetizing inductance as shown in **Fig. 2a**, its behavior after the turn-off instant of S_1, i. e., during the dead time, can be modeled in the Laplace domain (cf. **Fig. 2b**), where the voltage across S_3, $V_{\mathrm{S3},0} = V_{\mathrm{Cr1},0} + V_{\mathrm{Cr2},0} = v_{\mathrm{gC}}$, and the current in L_{M}, $I_{\mathrm{M},0} = \hat{i}_{\mathrm{M}}$ as given in (3), appear as initial conditions. During the switching half period prior to the considered turn-off of S_1, only the grid current flows through C_{r2}, whereas the superposition of the grid current and the transformer current flows through C_{r1}. Thus, the two initial conditions $V_{\mathrm{Cr1},0}$ and $V_{\mathrm{Cr2},0}$ are unequal, and can be calculated using

$$V_{\mathrm{Cr1},0} \approx \frac{v_{\mathrm{gC}}}{2} - \frac{i_{\mathrm{g}} \cdot T_{\mathrm{on}}}{2 \cdot C_{\mathrm{r1}}} \quad \text{and} \quad V_{\mathrm{Cr2},0} \approx \frac{v_{\mathrm{gC}}}{2} + \frac{i_{\mathrm{g}} \cdot T_{\mathrm{on}}}{2 \cdot C_{\mathrm{r2}}}, \tag{5}$$

whereby the short dead time interval is neglected.

The non-linear output capacitances, $C_{\mathrm{oss}}(v_{\mathrm{ds}})$, of the SiC-MOSFETs depend on the applied voltage. Fitting a power function to the datasheet curves allows to express the charge-equivalent capacitance, C_{Qeq}, as a function of the total voltage, $v_{\mathrm{ds}} = v_{\mathrm{gC}}$, applied to the device:

$$C_{\mathrm{oss,fit}}(v_{\mathrm{ds}}) = a v_{\mathrm{ds}}^{b} \tag{6}$$

$$C_{\mathrm{Qeq}}(v_{\mathrm{ds}}) = \frac{1}{v_{\mathrm{ds}}} \cdot \int_0^{v_{\mathrm{ds}}} C_{\mathrm{oss,fit}}(v)\, dv = \frac{a v_{\mathrm{ds}}^{b+1}}{(b+1) \cdot v_{\mathrm{ds}}} \tag{7}$$

With that it is possible to describe the voltage across S_3 during the dead time analytically as

$$v_{\mathrm{S3}}(t) = \sqrt{\hat{i}_{\mathrm{M}}^2 Z_0^2 + V_{\mathrm{Cr1},0}^2}\, \cos\left(\omega_0 t + \varphi\right) + V_{\mathrm{Cr2},0}, \tag{8}$$

where

$$\varphi = \arctan \frac{Z_0 \hat{i}_{\mathrm{M}}}{V_{\mathrm{Cr1},0}}, \quad Z_0 = \sqrt{\frac{L_{\mathrm{M}}}{2 C_{\mathrm{Qeq}}}}, \quad \omega_0 = \frac{1}{\sqrt{2 L_{\mathrm{M}} C_{\mathrm{Qeq}}}}.$$

C. ZVS Optimization with Constant Dead Time

In order to identify a loss-optimum combination of L_{M} and t_{d}, both parameter values are swept over specific ranges. For each combination $\{L_{\mathrm{M}}, t_{\mathrm{d}}\}$, average aIFE losses considering five different operating points (20 %, 40 %, 60 %, 80 % and 100 % of the nominal power) can be calculated by applying the models discussed above at a number of equally spaced time instants along a quarter of a grid period.

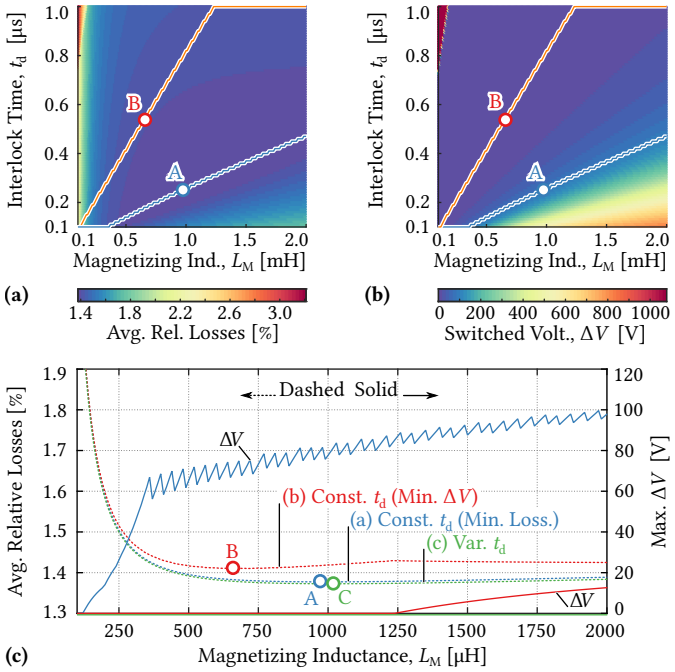

Fig. 4. Results for the basic ZVS considerations using the model from **Fig. 2**; **(a)** averaged relative losses (five power levels) and **(b)** maximum switched voltage, ΔV. **(c)** Averaged relative total aIFE losses for different magnetizing inductances, where the interlock time, t_{d}, is chosen (a) for minimum losses, (b) for minimum ΔV, and where it is variable in case (c). In addition, the corresponding maximum remaining voltages at turn-on, ΔV, are also indicated. If ZVS should be obtained over the entire grid period with a constant dead time, the minimum possible losses (design B) are higher than the minimum possible losses without full-range ZVS (design A). If the interlock time is variable, low losses *and* full ZVS can be obtained (design C).

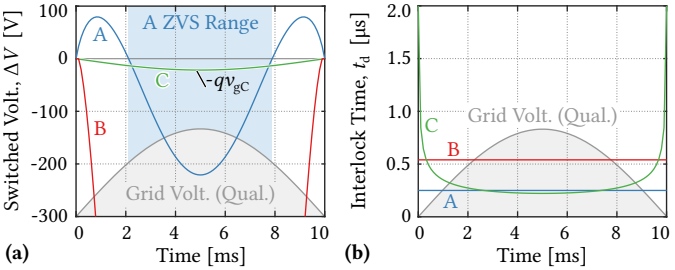

Fig. 5. (a) Switched voltage, ΔV, over half a grid period for the three example designs from **Fig. 4**, and **(b)** corresponding dead times.

Fig. 4a shows the resulting relative losses, and **Fig. 4b** shows the maximum ΔV in dependence of $\{L_{\mathrm{M}}, t_{\mathrm{d}}\}$. In both figures, the trajectories corresponding to either lowest losses (blue) or lowest ΔV (red) are indicated. Since the two trajectories do not coincide, it is not possible to obtain lowest losses *and* lowest ΔV for a given L_{M} using the same t_{d}.

This can also be seen in **Fig. 4c**, where the corresponding losses and ΔV values are shown as functions of L_{M}. The design with the lowest overall losses is marked as A—however, this design does not provide ZVS over the entire grid period, as can be seen from **Fig. 5a**, but only within a theoretical ZVS range, where $\Delta V \leq 0\,\mathrm{V}$. Note that this is no issue regarding losses, since the switching losses resulting from the incomplete ZVS transitions with a maximum residual voltage of only around 100 V are negligible for the considered SiC FETs

($< 0.5\,\mathrm{W}$). Nevertheless, the partial hard-switching during certain parts of the period might be a concern regarding potential EMI signature degradations. In contrast, design B (cf. **Fig. 4c**) is the design with lowest losses that in addition also achieves a maximum $\Delta V \leq 0\,\mathrm{V}$. As expected, it uses a lower magnetizing inductance and a larger dead time to achieve ZVS over the entire grid period (cf. **Fig. 5**). Therefore, its losses are higher than those of design A.

D. ZVS Optimization with Variable Dead Time

Apparently, it is not possible to obtain $\Delta V \leq 0\,\mathrm{V}$ over the entire grid period without an increase of the total losses if a constant dead time is used. This situation can be improved by introducing a time-varying dead-time. From (8), the dead time to provide guaranteed ZVS with a certain margin specified by q (i. e., $\Delta V^* \stackrel{!}{=} -q v_{\mathrm{gC}}$) can be calculated according to

$$t_{\mathrm{d}}^* = \frac{1}{\omega_0} \cdot \left[\pi - \arctan\left(\frac{Z_0 \hat{i}_{\mathrm{M}}}{V_{\mathrm{Cr1}}} \right) - \arccos\left(\frac{V_{\mathrm{Cr2}} + q v_{\mathrm{gC}}}{\sqrt{\hat{i}_{\mathrm{M}}^2 Z_0^2 + V_{\mathrm{Cr1}}^2}} \right) \right]. \tag{9}$$

Optimizing again by sweeping L_{M} yields design C with minimum losses (cf. **Fig. 4b**) and a variable t_{d}^* according to **Fig. 5b**. Note that design C features almost the same L_{M} as design A, and that the variable dead time of design C is similar to the constant dead time of design A over wide ranges of the grid period, which explains the similar (low) losses. However, in contrast to design A, design C provides complete ZVS over the entire grid period, as can be seen in **Fig. 5a**.

III. Advanced ZVS Analysis and Optimization

The above basic considerations exemplify the trade-offs regarding the ZVS-behavior of the aIFE. However, the situation is more complicated in reality, as can be seen from **Fig. 6**, which shows the full circuit of an aIFE stage with the initial conditions for a transition from S_1 to S_3 indicated—it is not sufficient to consider only the MV side bridge and the magnetizing current for the following reasons:

1) LV Side Parasitic Capacitances: First, the LV side bridge must be included, since its switches also feature parasitic capacitances, which affect the MV side switching transitions, because they provide an additional current path for the magnetizing current during the dead time.

2) Stray Inductance: Second, the stray inductance, L_σ, must be considered, too, because it forms a resonant circuit with the parasitic capacitances of both bridges, giving rise to a current oscillation that is superimposed on the magnetizing current and hence also affects the MV side switching transitions. Note that the superimposed oscillation can especially also cause an early rise of the voltage across S_3 (cf. **Fig. 3e** or curve a in **Fig. 7b**).

3) Diodes: It is important to highlight that, third, also the diodes of both bridges play an important role: as soon as the voltage across a certain diode/capacitance combination becomes higher than the junction voltage, the diode is forward biased an the behavior of the circuit changes. If it is a diode on the MV side, this initiates the start of the next resonant current pulse, which might cause a rise of the voltage across S_3 if the switch is not turned on in time (cf. **Fig. 3e**). If it is a diode on the LV side, the impedance of the current path on the LV side becomes lower, which means that less current is available to complete the switching transition on the MV side, possibly preventing a $\Delta V \leq 0\,\mathrm{V}$ even for a very long dead time (cf. **Fig. 7b**, curve c).

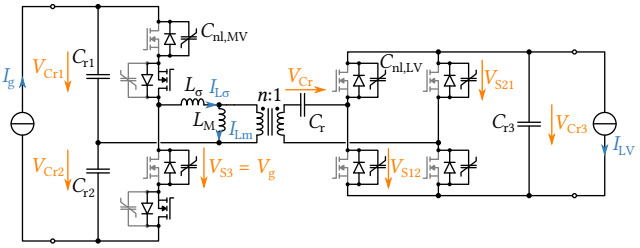

Fig. 6. Full aIFE circuit, including non-linear MOSFET capacitances, which is used to simulate the ZVS transitions for given initial conditions, which are also indicated in the figure.

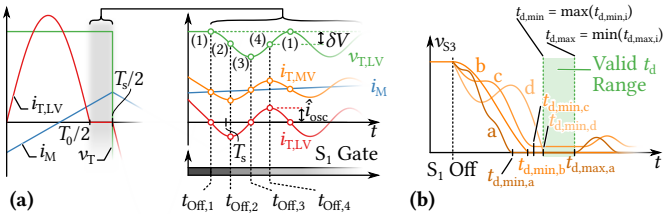

Fig. 7. (a) Parasitic oscillation during the current zero interval, where the switching transition occurs at an arbitrary point. The four extreme cases are marked with numbers (1)…(4), where (1) can be considered a "nominal" case. **(b)** Exemplary switching transitions for different initial conditions (e. g., (1…4) from (a)) and resulting tolerance band in which the dead time must be in order to ensure a ZVS transition.

4) Component Tolerances: As discussed above, typically $T_{\mathrm{s,n}} > T_0$ is chosen, resulting in an interval where the LV transformer current in theory equals zero while the MV bridge is still actively applying a voltage (cf. zoomed view in **Fig. 1b**). In reality, however, the stray inductance and the LV parasitic capacitances form an only very lightly damped resonant circuit once the LV diodes stop conducting, causing the current in L_σ and also the voltages across the LV parasitic capacitances, e. g., v_{S12}, to oscillate, which is illustrated in **Fig. 7a**. Therefore, the initial conditions of the actual switching transition depend on where relative to this high-frequency oscillation the actual switching occurs; the four extreme cases are indicated in the figure. In addition to the specific values of the involved components and hence the frequency of the parasitic oscillation, this is also influenced by the ratio $T_{\mathrm{s,n}}/T_0$, which depends on the specific values of the resonant tank components, e. g., L_σ. Whereas in a single cell system it would be possible to tune $T_{\mathrm{s,n}}$ such as to switch always under conditions of type (1) according to **Fig. 7a** (where the current in the stray inductance equals the magnetizing current and v_{S12} equals the LV voltage), this is not possible in multi-cell systems, where $T_{0,\mathrm{i}}$ may vary among the cells.

Therefore, in order to calculate the worst-case ΔV, and/or the required t_{d}, all four extreme initial conditions indicated in **Fig. 7a** must be considered for a single switching transition; each resulting in a specific variant of this switching transition—for example those corresponding to the four curves shown in **Fig. 7b**. Note that now, in order to obtain ZVS for all cells, the dead time has to be chosen in a window between a minimum and a maximum value, and note further that there might be situations where $\Delta V \leq 0\,\mathrm{V}$ cannot be achieved under all conditions, even with long dead times.

A. Detailed ZVS Modeling

The effects described above are very hard or even impossible (diodes) to capture with an analytical, Laplace-based model. Therefore, a simulation-based approach using GeckoCIRCUITS, which is capable of handling non-linear capacitances [28], and which can be scripted

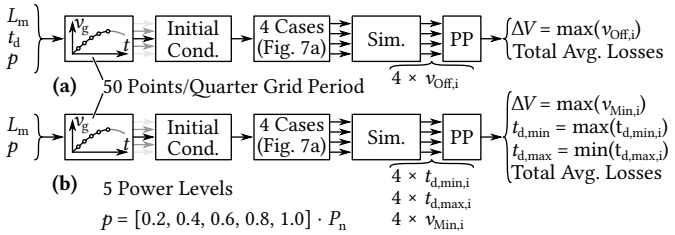

Fig. 8. Process of simulation-based evaluation of losses, ΔV, etc. for a given system (L_M, etc.) and a given power level, p, in case of **(a)** constant t_d, and **(b)** for variable t_d.

from MATLAB, is employed in the following to simulate ZVS transitions using the circuit shown in **Fig. 6**.

1) Initial Conditions: In addition to the initial conditions discussed already in Section II ($I_{\mathrm{M},0}$, $V_{\mathrm{Cr1},0}$ and $V_{\mathrm{Cr2},0}$) the simulation circuit from **Fig. 6** requires additional initial conditions, which can be found from similar considerations as before:

$$V_{\mathrm{Cr},0} \approx \frac{1}{2} \cdot \frac{1}{C_\mathrm{r}} \cdot \left(2 \cdot i_{\mathrm{g,A}} \cdot n \cdot \frac{T_{\mathrm{s,n}}}{2} \right) \tag{10}$$

$$V_{\mathrm{Cr},3} \approx \max \left(\frac{V_{\mathrm{Cr1},0}}{n} - 2 \cdot V_{\mathrm{f,LV}} \right) \tag{11}$$

The remaining ICs, i. e., $I_{\mathrm{L}\sigma,0}$ and $V_{\mathrm{S12},0} = V_{\mathrm{S21},0}$, vary for the four switching conditions (1)…(4) shown in **Fig. 7b**. The four cases can be approximated as follows: once the resonant current goes to zero, the high-frequency oscillation occurs between L_σ, the parallel connection of the two LV bridge legs' series-connected parasitic capacitances, the series resonant capacitor, C_r, and the MV side resonant capacitor, $C_{\mathrm{r},1}$. Combining the voltages of these capacitors results in an initial total voltage excitation of $\delta V = V_{\mathrm{Cr1},0}/n - V_{\mathrm{Cr3},0} - V_{\mathrm{Cr},0}$ (referred to the LV side). Since C_r and C_{r1} are much larger than the parasitic capacitance of the LV side, the characteristic impedance (also referred to the LV side) becomes $z_0 = \sqrt{L_\sigma/n^2 \cdot 1/C_{\mathrm{Qeq,LV}}(V_{\mathrm{Cr3},0})}$, and hence the amplitude of the oscillatory current can be estimated as $\hat{i}_\mathrm{osc} = \delta V / z_0$. The four points shown in **Fig. 7a** can be approximated by adding and/or subtracting δV and $\hat{i}_\mathrm{osc}$ from $V_{\mathrm{Cr3},0}$ and $I_{\mathrm{M},0}$, respectively. Note that the (small) change of the magnetizing current, etc. during this short oscillatory interval is neglected, as is also a damping of the high-frequency oscillation.

2) Optimization Procedure: Generally, the optimization procedure is very similar as for the simplified case above, however, the calculation of $\Delta V(t_\mathrm{d})$ in case of a constant t_d or the calculation of the required t_d in case of variable dead time is carried out based on the simulated voltage across S_3. As can be seen from **Fig. 8a** and **b**, again several operating points (power levels) are considered, and many switching instants during one quarter of a grid period are evaluated.

In case a constant t_d is used, the simulated waveform of $v_{\mathrm{S3}}(t)$ during the interlock time can be used to identify $\Delta V(t_\mathrm{d})$ (cf. **Fig. 8a**) and in case of a variable t_d, the time where $v_{\mathrm{S3}}(t)$ reaches its minimum (note that there might be cases where ZVS is not possible at all, cf. **Fig. 7b**, curve c), the corresponding ΔV, but also the maximum allowable t_d, after which $v_{\mathrm{S3}}(t)$ might swing back to positive values (**Fig. 7b**, curve a). All four extreme cases indicated in **Fig. 7a** are considered in order to find the worst-case ΔV, and, in case of a variable t_d, the most stringent boundaries for $t_{\mathrm{d,min}}$ and $t_{\mathrm{d,max}}$. The losses are calculated in the same way as before, however, considering always a switching transition under condition (1) according to **Fig. 7a**, i. e., for the "nominal" case that could be achieved by tuning $f_{\mathrm{s,n}}$. This is a feasible approximation since, considering a multi-cell system, it is anyway unknown with which initial conditions the individual cells actually switch.

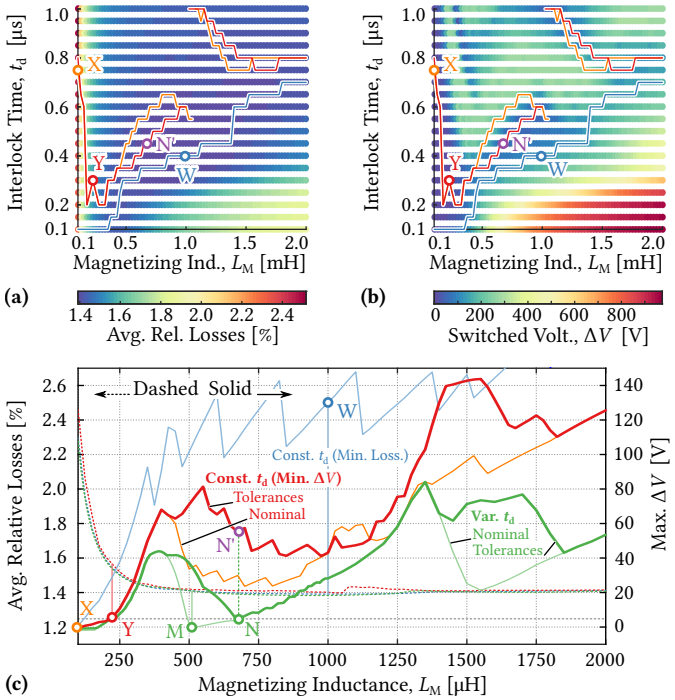

Fig. 9. Results from the full simulation model. **(a)** shows relative losses for combinations of L_M and t_d, **(b)** shows the corresponding worst-case ΔV (considering the four extreme switching instants shown in **Fig. 7b**). In addition, the trajectories corresponding to lowest losses (blue), lowest worst-case ΔV (red) and lowest ΔV considering only the nominal switching conditions (1) (orange) are indicated. Correspondingly, **(c)** shows the relative losses as well as ΔV in dependence of the magnetizing inductance. Please refer to the text for a detailed explanation of the different curves and design points.

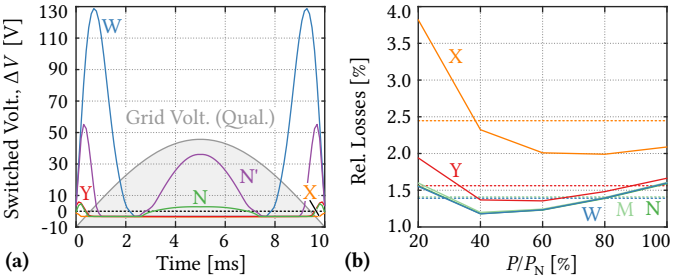

Fig. 10. **(a)** Switched voltage over half a grid period for different designs (W and X are for switching under nominal conditions (1), Y, N and N' include component tolerances, i. e., show the worst-case ΔV that is to be expected in a multi-cell system). **(b)** Calculated efficiency curves for specific designs. In addition, also the averaged relative losses (as, e. g., shown in **Fig. 9**) are indicated.

B. Results of Detailed ZVS Analysis

As for the simplified analysis from Section II, **Fig. 9a** and **b** show the losses and the worst-case ΔV for combinations of L_M and t_d. Three trajectories for minimum losses, minimum ΔV assuming nominal switching conditions (1), and minimum worst-case ΔV (i. e., considering conditions (1)…(4)) are indicated. The corresponding quantities are also plotted in **Fig. 9c** in dependence of L_M, where several designs are highlighted, and **Fig. 10** shows resulting ΔV over half a grid period as well as relative loss curves for these designs:

- Design W is the minimum loss design using a constant t_d, which, in contrast, still shows quite high maximum ΔV values in the

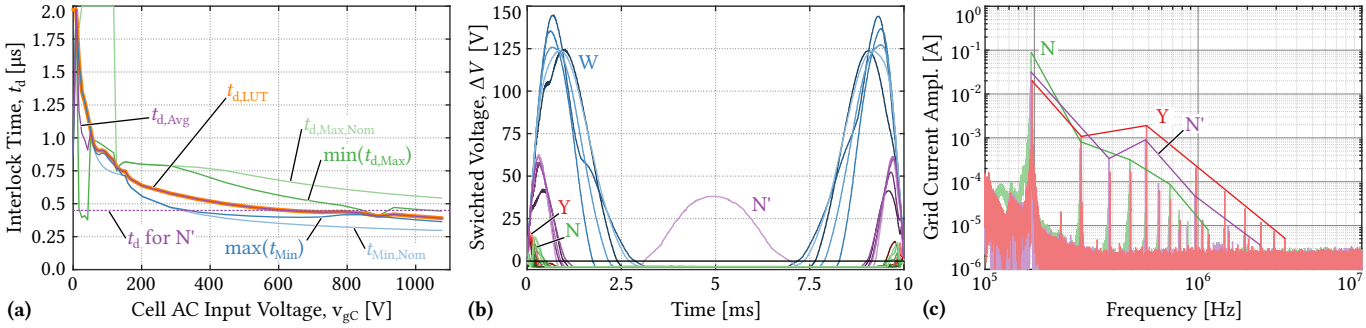

Fig. 11. **(a)** Valid t_d range for design N and chosen $t_{d,LUT}$ for the look-up table used in the full-system simulation; **(b)** shows the simulated ΔV of the five converter cells for different designs (cf. **Fig. 9**), and **(c)** shows corresponding grid current spectra.

vicinity of the zero-crossing of the grid voltage.

- Design X: also using a constant t_d, this design realizes a maximum ΔV of almost 0 V, however, with much higher losses as a consequence of its higher magnetizing current and the longer dead time. Since these losses are independent of the load, especially the part-load efficiency suffers.
- Design M: considering now a variable t_d, this is the design that achieves lowest ΔV if only switching at the nominal instant (1) is considered. i. e., it is the design that would be chosen in case a tuning of $f_{s,n}$ to achieve these conditions was possible, e. g., in a single-cell system. As design X, design M realizes also a maximum ΔV close to zero, however, with losses that are much lower and comparable to those of design W.
- Design N is the variable dead time design with the lowest worst-case ΔV considering tolerances, i. e., all four switching conditions, achieving $\Delta V \leq 10\,\mathrm{V}$, which is less than 1 % of $\hat{v}_{gC}$. Note again that the losses are comparable to those of design W.
- Design Y is a design with constant dead time that shows comparable worst-case ΔV values as design N, which results again in higher losses.
- Design N': finally, design N' is a design using the same L_M as design N, but a constant dead time such as to result in lowest worst-case ΔV, which is, as expected, significantly higher than that achievable with a variable t_d.

The basic trade-offs are thus similar to those identified for the simplified case discussed earlier. However, it can be seen that the range of suitable L_M values is quite constrained if low worst-case ΔV (to reduce EMI originating from partial hard switching) and low losses shall be achieved, even in case a variable dead time is used. One reason for this is that there are situations where the voltage across S_3 does not swing completely to zero at all, because the LV side diodes start to conduct early. This is an effect that could not be captured with the simplified, analytical model.

Considering design N, **Fig. 11a** shows the minimum and maximum boundaries for the dead time as a function of the cell AC input voltage, v_{gC}. Note that for low input voltages, the two curves intersect, i. e., $\min(t_{d,Max}) < \max(t_{d,Min})$, indicating that a certain dead time might be too short for switching at, e. g., instant (2), whereas it is already too long if the switching occurs at, e. g., instant (4) (cf. **Fig. 7a**). This is the reason why for many L_M values it is not easily possible to obtain $\Delta V < 0\,\mathrm{V}$, even with a variable dead time.

C. Verification

In order to implement the variable dead time of design N in a full system simulation consisting of five cascaded converter cells, each fully modeled with non-linear parasitic capacitances on the MV and on the LV side, a look-up table (LUT) is used that stores the required dead time as a function of the cell's input voltage. According to **Fig. 11a**, $t_{d,LUT}$ is obtained by taking a weighted average $t_{d,LUT} = 1/3 \cdot (2 \cdot \max(t_{Min}) + \min(t_{d,Max}))$ and limiting this value to $\max(t_{d,Min})$ in regions where $\max(t_{d,Min}) > \min(t_{d,Max})$, resulting in the orange curve shown in the figure.

In each of the five cascaded aIFE cells used in the simulation model, the value of L_σ is varied slightly (9.5 µH, 9.75 µH, 10 µH, 10.25 µH, 10.5 µH) in order to create non-equal resonant frequencies among the cells. **Fig. 11b** shows the simulated ΔV values (obtained by sampling the voltage across a MV switch when it is turned on) for various designs over half a grid period. A good agreement with the predictions from the optimization (cf. **Fig. 10a**) can be observed. It can also be seen how the ΔV values vary between the different cells; e. g. for design N' only one cell switches under conditions that cause a loss of ZVS in the middle of the grid period. Note that this has to be expected, considering that the constant t_d of design N' violates the limits (i. e., $\max(t_{Min})$ and $\min(t_{d,Max})$ not only for low but also for high voltages according to **Fig. 11a**.

In order to reduce the harmonic content of the grid current, the S^{3}T's aIFE stages are operated in an interleaved manner (details in [7]). Therefore, **Fig. 11c** shows the resulting spectra of the grid current for three designs. It can be seen that design N (variable dead time), has a higher peak at around 100 kHz, i. e., twice the individual aIFE switching frequency, indicating that a variable dead time compromises the interleaving of the cells (even though the dead time variation is the same for all cells). On the other hand, the higher order harmonics are spread over a wider frequency range, resulting in lower peaks. It is also interesting to notice that design Y, which achieves low ΔV by means of a large magnetizing current and long but constant t_d, suffers from even higher peaks at higher frequencies, which is a consequence of the magnetizing current distorting the voltages across the input capacitors to a degree that visibly worsens the harmonic content of the grid current.

D. Discussion

The above detailed analysis of the ZVS behavior of the HC-DCM SRC in |AC|-DC applications, e. g., IFE-based SSTs such as the S^{3}T, can be summarized in a few design guidelines. If EMI is not of concern, a combination of a magnetizing inductance and a dead time that results in low (or lowest) losses can easily be identified. However, such designs typically do not achieve complete ZVS over the entire grid period. If, in contrast, the maximum worst-case switched voltage should be limited to very low values, e. g., 10 V or ideally even 0 V (full ZVS), there are two options: first, another combination of

magnetizing inductance and dead time that fulfills this requirement can be found, however, increased losses and especially a massively reduced part-load efficiency are the price to pay; furthermore, the high-frequency harmonic content of the grid current is increased. Second, the dead time could be varied over the grid period, which allows to use a comparably large magnetizing inductance and hence results in low losses. On the other hand, the implementation of a variable dead time increases the complexity, and a variable dead time compromises the interleaved operation of the aIFE stages, resulting in a slightly higher harmonic at about twice the aIFE switching frequency, whereas in contrast, higher-frequency harmonic peak values are reduced.

Note that for applications where bidirectional power flow is required, the presented analysis could be repeated also for the case where the LV side bridge is actively switching in order to identify a suitable magnetizing inductance and, possibly variable, dead times for both bridges.

It is thus possible to achieve ZVS over the entire grid period, however, either at the price of increased complexity or increased losses. With the aim of low complexity solutions, another option could be to also use a constant dead time, causing a loss of ZVS in a sufficiently narrow region around the grid voltage zero crossings only, and then to simply stop switching the aIFE stages around these zero crossing, which is a concept employed, e. g., in low-voltage single-phase TCM PFC circuits [29]. This would basically trade EMI performance (no partial hard switching) against lower-frequency grid current distortions, and could be a pragmatic approach that would allow to keep control complexity low.

IV. Conclusion

This paper provides a detailed analysis of the ZVS behavior of the resonant isolation stages of an isolated front end (IFE) SST, using the example of the Swiss SST (S^3T), an all-SiC $25\,\mathrm{kW}$, $6.6\,\mathrm{kV}$ AC to $400\,\mathrm{V}$ DC IFE-based SST. Essentially, these resonant isolation stages are series resonant converters operated in the half-cycle discontinuous-conduction-mode (HC-DCM), however, not with DC but with grid-frequency $|\mathrm{AC}|$ input and output voltages. Thus, the magnetizing current available for ZVS varies over the grid period, as does the voltage that needs to be switched. The magnetizing inductance and the dead time can be chosen such as to result in lowest overall losses, however, without achieving complete ZVS over the entire grid period. If full-ZVS is required, e. g., to reduce EMI emissions, a larger magnetizing current and/or a longer dead time must be used, both increasing the losses. As an alternative, the dead time can be varied during the grid period, which allows to obtain both, (almost) full-ZVS and low losses, however, with a slightly more complicated modulation scheme including, e. g., a lookup table for the dead time. The analysis includes also the effects of component tolerances among the cascaded converter cells in a multi-cell IFE SST, and is finally verified using a very detailed simulation model, including non-linear MOSFET capacitances and component tolerances.

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