Power Electronic Systems
Laboratory

IEEE Transactions on Power Electronics, Vol. 32, No. 11, pp. 8800-8812, November 2017

Sinusoidal Input Current Discontinuous Conduction Mode Control of the VIENNA Rectifier

M. Leibl,
J. W. Kolar,
J. Deuringer

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Sinusoidal Input Current Discontinuous Conduction Mode Control of the VIENNA Rectifier

Michael Leibl, *Member, IEEE*, Johann W. Kolar, *Fellow, IEEE*, and Josef Deuringer

***Abstract*—During light load conditions unidirectional power factor correction rectifiers, such as the VIENNA rectifier, enter discontinuous conduction mode, causing the relationship between average half-bridge voltage and duty cycle to become nonlinear and synchronously sampled current measurements not equaling the switching period average. Combined, these measurement and actuation errors result in distorted input currents at light load if no additional measures are taken. This work presents a control scheme that leads to low total harmonic distortion of the input currents in discontinuous conduction mode without relying on current measurements. The analytic expressions for the duty cycles and the threshold between discontinuous and continuous conduction mode are derived, the capability of supplying asymmetric loads is investigated and the effect on the noise spectrum relevant for the electromagnetic interference filter design is studied. Measurements of efficiency, total harmonic distortion, and conducted electromagnetic interference in discontinuous and continuous conduction mode are obtained on a 65 kW prototype operating at 290 to 530 V line-to-line RMS mains voltage range and supplying 800 V dc output voltage. The prototype, which is optimized for pulse load applications, achieves a power density of 9.56 kW/dm^3 (157 W/in^3) and 97.2 % efficiency at full load using 650 V Si insulated gate bipolar transistor (IGBTs) with 28 kHz switching frequency.**

***Index Terms*—AC-DC converter, discontinuous conduction mode, light load, pulse load, three-phase rectifier.**

I. Introduction

MEDICAL X-ray system power supplies have to provide high dc voltages of up to 150 kV to the X-ray tube. Most of the power is dissipated as heat within the anode of the vacuum tube and only $\approx 1\%$ of the power is actually emitted as Bremsstrahlung, which is used for diagnostic and also for therapy purposes [1]. Since the vacuum tube only provides limited heat transfer to the ambient, the average power that can be supplied to the tube is given by the maximum temperature of the anode and its thermal resistance to the ambient and it typically amounts to less than 1 kW. The peak power, however, is only limited by the internal thermal resistance of the anode, which is typically a composite of tungsten and copper or molybdenum [2]. Therefore, it can be considerably higher reaching values up to 100 kW. The duration of such a full power pulse is limited by the total amount of energy, which can be stored in the thermal capacitance of the anode at its maximum temperature, thus usually full load pulses are limited to less than 10 s.

Therefore, power supplies of X-ray systems can be designed to take advantage of the relatively low average power. Also, due to the low amount of full load operating hours the primary objective is to reach lowest material cost instead of highest efficiency, while maintaining high reliability despite the thermal cycling [3]. For this reasons nowadays X-ray power supplies are using passive diode rectifiers supplying a dc voltage, which is depending on the mains voltage. In order to deal with 400 and 480 V mains voltages with 10% over- and 20% under-voltage tolerances, high-voltage generators connected to passive rectifiers, therefore, have to be able to cope with a wide input voltage range, while also providing a wide output voltage range of typically 100 to 150 kV at full power, limiting the overall system performance. Furthermore, six pulse diode rectifiers exhibit considerable harmonic current emissions, which may require additional low-frequency harmonic filtering depending on the utility grid regulations [4].

To relieve the stress on the high-voltage generator and to increase the input current quality an active rectifier shall be optimized for a given pulsed load scenario of 65 kW peak power for up to 10 s with 1 kW average power. Because only unidirectional power flow is required, the three-level three-phase rectifier often referred to as VIENNA rectifier (VR), is well suited since it provides stable dc-link voltage and sinusoidal input currents. Compared to the two-level six-switch rectifier [5], the power semiconductors only need to block half of the dc-link voltage, which can be as low as the line-to-line peak voltage. Therefore, low switching loss 650 V insulated gate bipolar transistor (IGBTs) in combination with low reverse recovery charge 650 V free-wheeling diodes can be employed, which match the low-cost, high-reliability design target. Due to the three-level topology, also the maximum voltage time product applied to the boost inductors is only half of the one of a two-level topology. Different circuit variants of the VR exist including the original three switch solution [6] and the T-type variant [7], however, the neutral point clamped (NPC) structure as shown in Fig. 1 is chosen since it includes only two semiconductors in the commutation loop, both subjected to only half the dc-link voltage and only two semiconductors in the current path of each phase. Additionally to the six free-wheeling diodes of the boost stages,

Manuscript received September 22, 2016; accepted December 5, 2016. Date of publication December 19, 2016; date of current version June 23, 2017. Recommended for publication by Associate Editor Richard Redl.

M. Leibl is with the Department of Information Technology and Electrical Engineering, ETH Zurich, Zurich 8092, Switzerland (e-mail: leibl@lem.ee.ethz.ch).

J. W. Kolar is with the Department of Electrical Engineering, ETH Zurich, Zurich 8092, Switzerland (e-mail: kolar@lem.ee.ethz.ch).

J. Deuringer is with the Clinical Products Division, Siemens Healthcare GmbH, Erlangen 91052, Germany (e-mail: josef.deuringer@siemens.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2641502

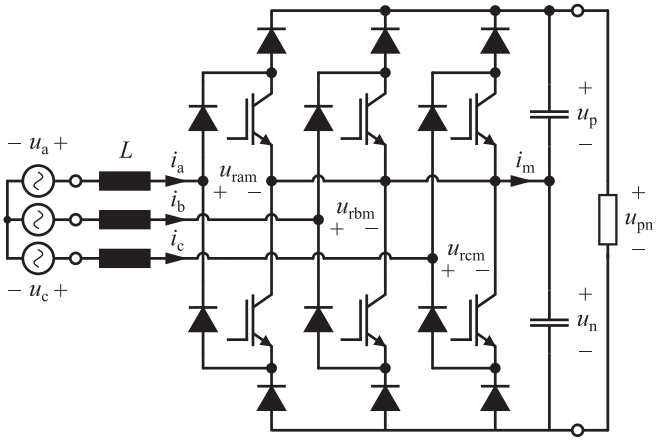


Fig. 1. VR NPC circuit topology. The currents in the boost inductors are guided through three of the six mains frequency commutated rectifier diodes into three of the six boost stages. By controlling the duty cycles of the boost stages the currents are closed loop controlled. Due to the split dc-link all semiconductors are subjected to only half the dc-link voltage.

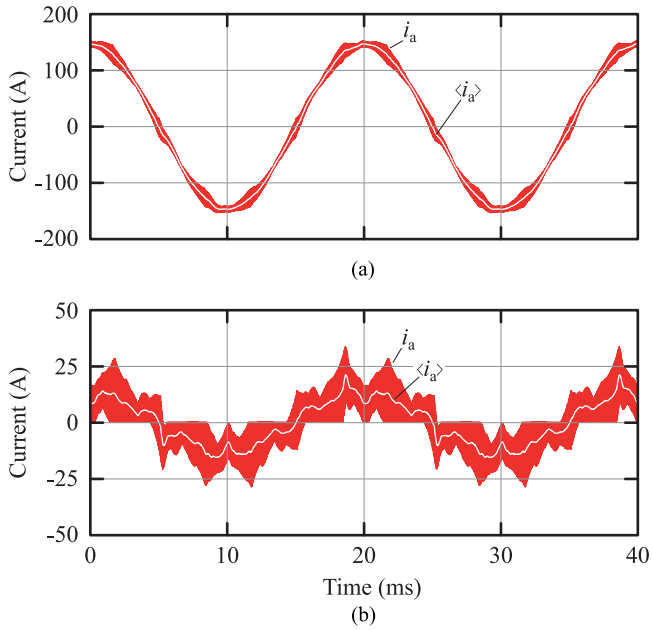


Fig. 2. Simulated current in one of the boost inductors of the VR and its local average with 400 V RMS line-to-line input voltage, 800 V dc output voltage, 50 μH boost inductance per phase, 28 kHz switching frequency, and 65 kW output power. (a) Reducing the power to 6.5 kW. (b) Results in a distorted shape of the local average due to DCM.

six rectifier diodes only commutating with mains frequency are used, which can be slow but in turn provide low forward voltage drop. As an option thyristors can be used instead of the rectifier diodes, allowing to include dc-link charging capability [8].

Inductive components show a strong tradeoff between power density and efficiency, i.e., between material cost and electricity cost. Therefore, a total cost of ownership (TCO) optimization [9] is carried out to determine the optimum size of the filter inductors. Due to the high-peak low-average load scenario, the number of full load operating hours is typically low, resulting in low material cost and extremely high power density of the filter inductors. Material temperature limits are not exceeded because of the low average power. Also, with high power density, the loss densities in core and winding of the boost inductors are high, and therefore, the high frequency (HF) flux density amplitude is high. Assuming that the air gap is set such that the peak flux density does not exceed the saturation flux density with some margin, high HF flux density results in relatively high current ripple of $\frac{\Delta i}{i} \approx 25\%$ for the considered system.

Unidirectional converter systems such as the VR exhibit a discontinuous conduction mode (DCM) at light load, i.e., when the input current local average is less than the ripple amplitude. In Fig. 2(a), the inductor current and its local average are shown for 65 kW load, the relative current ripple is in the range of 25% in this case. At 6.5 kW, which is considered light load, the absolute inductor ripple is still the same but the relative peak-to-peak inductor current ripple is already $> 200\%$ as shown in Fig. 2(b). Therefore, DCM occurs and the current measurement, which relies on synchronous sampling becomes inaccurate and the relationship between duty cycle of the switch and average half bridge voltage is changed. As a result, the local average of the current waveform is no longer sinusoidal. Solutions to this problem for single-phase rectifiers exist [10], however, they can not be directly applied to the VR due to the coupling of the three phases.

Two control schemes to operate the VR in DCM are already known. In the first control scheme [11], all switches are turned ON and OFF at the same time (single-switch rectifier control scheme, [12]). The currents have approximately triangular shape but their local average value is not varying sinusoidally. However, the control is simple because the duty cycle is directly set by the output voltage controller and no current sensors are required. Furthermore, the switch that carries the highest current can be turned OFF a little earlier or later than the other two switches. This allows us to actively balance the dc link voltages.

The second solution proposed in [13], extends the DCM control loop by an adaptive compensator. The currents in the boost inductors are modeled by using an observer and compared to the measured values. The error of the local average of each current is then fed into a PI-controller, whose integral part is inverted at each zero crossing of the according phase voltage. This way the error voltage of each phase, which is the difference between the voltage set according to the duty cycle and the actually applied voltage because of current discontinuity, can be compensated. However, after a load step the controller takes considerable time, approximately 10 ms, to adapt to the new error voltages. Furthermore, the control scheme relies on current measurements during DCM control, which are not as easy to obtain as in continuous conduction mode (CCM), since the time when the instantaneous value of the current equals its local average is not known in advance. However, it offers the advantage that no change between different control schemes occurs throughout the whole power range.

This work, which is based on [14], presents a control scheme that prevents this kind of input current distortion based on the exact analytic solution for the duty cycles of the VR in DCM. In Section II, the solution for setting the duty cycles in DCM for sinusoidal currents is derived, the capability of balancing the

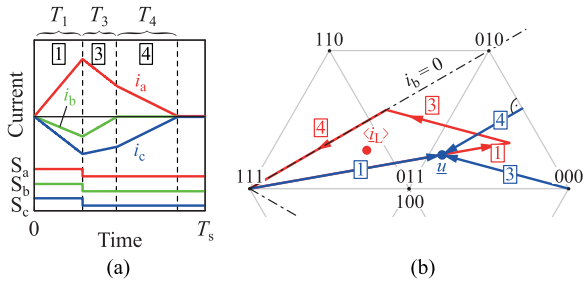


Fig. 3. Boost inductor currents during one switching period in DCM with synchronously operated switches while $u_a > 0 > u_b > u_c$ (a) and space vector representation of the same situation (b).

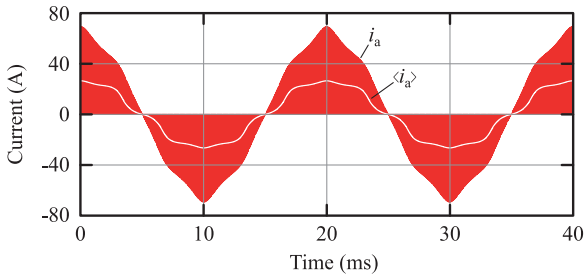


Fig. 4. Simulated boost inductor current of one phase and its local average value in DCM with synchronously operated switches. Operating condition and parameters used for the simulation: $\hat{u} = \sqrt{2} \cdot 230$ V, $U_{pn} = 800$ V, $P = 13$ kW, $f_s = 28$ kHz, $L = 50$ µH.

dc-link voltages and supplying asymmetric loads (unequal power drawn from the partial output voltages u_p and u_n) is investigated, the threshold to CCM is derived and the effect on the conducted electromagnetic interference (EMI) noise emission is studied. In Section III, experiments on a hardware prototype are presented that confirm the feasibility of the approach including control performance during load steps and efficiency, total harmonic distortion (THD) and EMI measurements.

II. Analysis

Aiming for a better understanding of the behavior of the VR in DCM space vector representations for voltages and currents can be used [12]. With $\underline{a} = \exp(j\frac{2\pi}{3})$ the mains voltages are transformed into the space vector

$$\underline{u} = u_\alpha + j u_\beta = \frac{2}{3}(u_a + \underline{a} u_b + \underline{a}^2 u_c) \tag{1}$$

the rectifier input voltages into the space vector

$$\underline{u}_r = u_{r\alpha} + j u_{r\beta} = \frac{2}{3}(u_{ram} + \underline{a} u_{rbm} + \underline{a}^2 u_{rcm}) \tag{2}$$

and the boost inductor currents into the space vector

$$\underline{i} = i_\alpha + j i_\beta = \frac{2}{3}(i_a + \underline{a} i_b + \underline{a}^2 i_c). \tag{3}$$

For the following considerations a switching period at a mains voltage angle of $\varphi = 10°$ of a symmetric three-phase system with $u_a = \hat{u}\cos(\varphi)$, $u_b = \hat{u}\cos(\varphi - \frac{2\pi}{3})$, $u_c = \hat{u}\cos(\varphi - \frac{4\pi}{3})$ is considered. The values of the mains voltages, which are assumed to be constant during the switching period, therefore, satisfy the condition $u_a > 0 > u_b > u_c$. It is also assumed that at the beginning of the switching period $T_s = \frac{1}{f_s}$, the boost inductor currents are zero.

A. Synchronous Switching DCM

One option, to control the VR in DCM, is to operate all switches synchronously, i.e., to turn them ON and OFF at the same time setting the duty cycle such that the required power is transferred into the dc-link. However, this operating principle results in nonsinusoidal input currents as can be easily shown by using space vector representation. After turning ON all switches at $t = 0$, each current is rising at a rate proportional to its according phase voltage as shown in interval 1 in Fig. 3(a). The space vector representation of this interval shown in Fig. 3(b) reveals that according to

$$\frac{d\underline{i}}{dt} = \frac{1}{L}(\underline{u} - \underline{u}_r) \tag{4}$$

the current space vector is moving along the indicated trajectory 1 in the direction of the mains voltage space vector, since the rectifier voltage space vector $\underline{u}_r(111)$ is zero. After turning OFF all switches at the same time, the phase currents commutate to the free-wheeling diodes and thus during this interval 3 all phase currents are decreasing. The voltage space vector applied to the boost inductors now is the difference between the rectifier voltage space vector $\underline{u}_r(000)$, which is applied during this switching state and the mains voltage space vector. The boost inductor current space vector, therefore, moves along the trajectory 3 during this state. As soon as the phase current with the smallest absolute value (i_b) reaches zero, state 4 is entered. Now, the difference between the rectifier voltage space vector 3 projected to the line $i_b = 0$ and the mains voltage space vector is applied to the boost inductors. The boost inductor current space vector moves along the line $i_b = 0$ until it reaches the origin where it remains until the end of the switching period. This investigation shows that the local average of the boost inductor current with synchronous switching is located somewhere within the triangle 1-3-4, which is aligned with the mains voltage space vector with one side. Therefore, the local average of the boost inductor current space vector is generally not in phase with the mains voltage space vector. Since the phase shift between the mains voltage space vector and the local average of the boost inductor current space vector varies throughout the mains period, taking positive and negative values, a nonsinusoidal shape of the input current is observed with synchronously controlled switches. This is confirmed by the simulated waveform shown in Fig. 4.

B. Proposed Sinusoidal Current DCM Pattern A

In order to achieve sinusoidal input currents, the phase shift between the local average of the boost inductor current space vector and the mains voltage has to be constant throughout the mains period. Achieving zero phase shift, i.e., resistive mains behavior, is intended in the following. For zero phase shift in the considered example an additional voltage space vector has to be

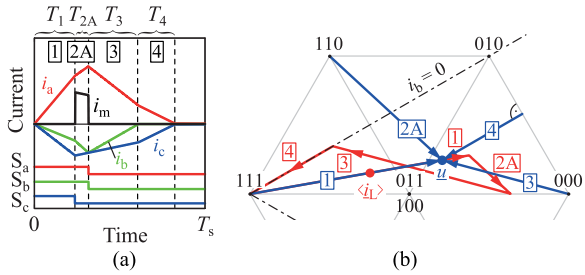


Fig. 5. Boost inductor currents during one switching period in DCM employing switching state 2A while $u_a > 0 > u_b > u_c$. (a) Space vector representation of the same situation. (b) The duration of the switching state 2A is chosen such that the phase shift between mains voltage space vector and boost inductor current space vector is zero.

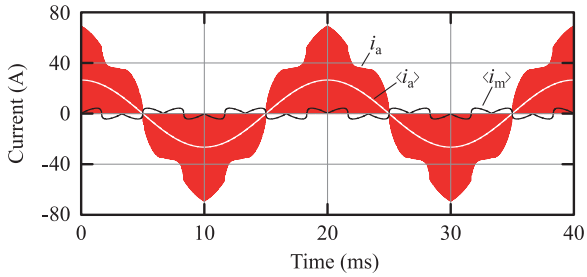


Fig. 6. Simulated boost inductor current of one phase, its local average value, and the local average value of the midpoint current in DCM employing switching state 2A to reach resistive mains behavior. Operating condition and parameters used for the simulation: $\hat{u} = \sqrt{2}\cdot$ 230 V, $U_{pn} = 800$ V, $P = 13$ kW, $f_s = 28$ kHz, $L = 50$ µH.

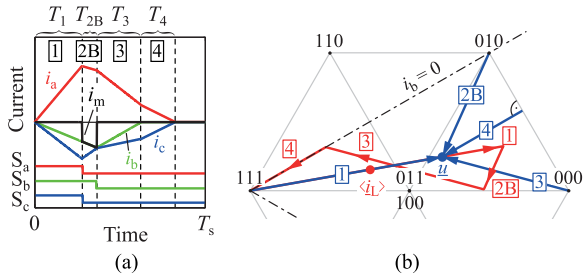


Fig. 7. Boost inductor currents during one switching period in DCM employing switching state 2B while $u_a > 0 > u_b > u_c$. (a) Space vector representation of the same situation. (b) Duration of the switching state 2B is chosen such that the phase shift between mains voltage space vector and boost inductor current space vector is zero.

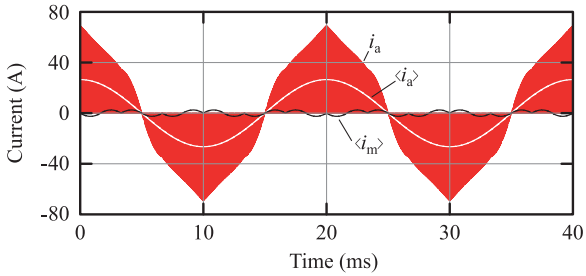


Fig. 8. Simulated boost inductor current of one phase, its local average value, and the local average value of the midpoint current in DCM employing switching state 2B to reach resistive mains behavior. Operating condition and parameters used for the simulation: $\hat{u} = \sqrt{2}\cdot$ 230 V, $U_{pn} = 800$ V, $P = 13$ kW, $f_s = 28$ kHz, $L = 50$ µH.

applied as shown in Fig. 5(b). Turning off the switch of phase c earlier than the others, inserts the state 2A with the according voltage space vector that shifts the boost inductor current space vector into the appropriate direction to eliminate the phase shift between mains voltage and boost inductor current. The phase current waveforms during one switching period applying to this situation are shown in Fig. 5(a) and it can be observed that during state 2A the absolute value of the current of the phase with the smallest absolute voltage increases. At the same time a current i_m is injected into the dc-link midpoint with opposite sign as the phase voltage with smallest absolute value. By adjusting the duration of state 2A such that zero phase shift is maintained throughout the mains period the simulated waveform of the boost inductor current of one phase shown in Fig. 6 is obtained. The local average of the boost inductor current is sinusoidal and it can be observed that the local average of the midpoint current varies with three times the mains frequency and contains no dc-component.

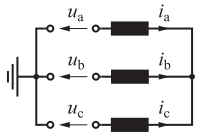
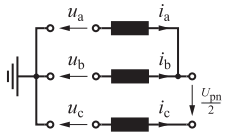
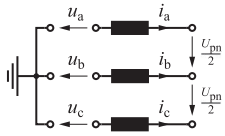
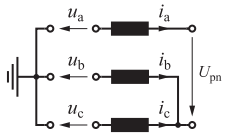
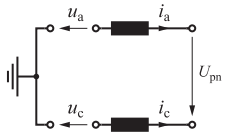
C. Proposed Sinusoidal Current DCM Pattern B

Although when using the switching pattern described in Section II-B, the generated midpoint current contains no dc-component, it is desired to be able to provide a small dc midpoint current to counteract asymmetric leakage currents or small asymmetric loads connected to the output that would otherwise cause unbalanced dc-link voltages. Using the switching state 010 in the aforementioned example as shown in Fig. 7 allows exactly that. By leaving the switch of the phase with the smallest absolute voltage turned ON longer than the two others, switching state 2B is inserted between states 1 and 3. The space vector diagram in Fig. 7(b) shows that this switching state also allows us to achieve zero phase shift between mains voltage and local average of the boost inductor current, if the duration of the state is chosen correctly. The current waveforms during one switching period [see Fig. 7(a)] reveal that the absolute value of the current of the phase with the smallest absolute voltage is also rising, as it is when state 2A is applied. However, since the midpoint current during state 2B equals the current of the phase with the smallest absolute value of the voltage the direction of the midpoint current during state 2B is opposite to its direction during state 2A. If the duration of state 2A is chosen correctly to eliminate the phase shift between mains voltage and boost inductor current throughout the mains period, the local average of the boost inductor current is also sinusoidal as shown in Fig. 8. By comparing Figs. 6 and 8, it is observed that the local average of the midpoint current has opposite sign in the two different switching patterns A and B.

D. Calculation of the Duty Cycles

In order to actually achieve sinusoidal currents by using the switching patterns, described in Sections II-B and II-C, the

TABLE I
SWITCHING STATES OF THE PROPOSED SINUSOIDAL CURRENT DCM CONTROL SCHEME, ASSUMING $u_a > 0 > u_b > u_c$

State	S_a,S_b,S_c	Equivalent Circuit	Changes of inductor currents	Duration of state
1	1 - 1 - 1		$\Delta i_{a1} = \frac{T_1}{L} \cdot u_a$ $\Delta i_{b1} = \frac{T_1}{L} \cdot u_b$ $\Delta i_{c1} = \frac{T_1}{L} \cdot u_c$	$T_1 = \frac{D_1}{f_s}$
2A	1 - 1 - 0		$\Delta i_{a2A} = \frac{T_{2A}}{L} \cdot (u_a - \frac{U_{pn}}{6})$ $\Delta i_{b2A} = \frac{T_{2A}}{L} \cdot (u_b - \frac{U_{pn}}{6})$ $\Delta i_{c2A} = \frac{T_{2A}}{L} \cdot (u_c + \frac{U_{pn}}{3})$	$T_{2A} = \frac{D_{2A}}{f_s}$
2B	0 - 1 - 0		$\Delta i_{a2B} = \frac{T_{2B}}{L} \cdot (u_a - \frac{U_{pn}}{2})$ $\Delta i_{b2B} = \frac{T_{2B}}{L} \cdot u_b$ $\Delta i_{c2B} = \frac{T_{2B}}{L} \cdot (u_c + \frac{U_{pn}}{2})$	$T_{2B} = \frac{D_{2B}}{f_s}$
3	0 - 0 - 0		$\Delta i_{a3} = \frac{T_3}{L} \cdot (u_a - \frac{2U_{pn}}{3})$ $\Delta i_{b3} = \frac{T_3}{L} \cdot (u_b + \frac{U_{pn}}{3})$ $\Delta i_{c3} = \frac{T_3}{L} \cdot (u_c + \frac{U_{pn}}{3})$	$T_3 = -\frac{L \cdot (\Delta i_{b1} + \Delta i_{b2x})}{u_b + \frac{U_{pn}}{3}}$
4	0 - 0 - 0		$\Delta i_{a4} = \frac{T_4}{2L} \cdot (u_a - u_c - U_{pn})$ $\Delta i_{b4} = 0$ $\Delta i_{c4} = \frac{T_4}{2L} \cdot (u_c - u_a + U_{pn})$	$T_4 = -\frac{2L \cdot (\Delta i_{a1} + \Delta i_{a2x} + \Delta i_{a3})}{u_a - u_c - U_{pn}}$

durations of switching states 1, 2A, and 2B have to be set correctly, depending on the amount of power to be transferred, the values of the phase voltages, and the dc-link voltage. As shown in the following the required expressions can be found analytically. For each of the described five switching states, n the equivalent circuit, the current change Δi_{kn} in each phase mains k and the duration T_n are given in Table I. Using these equations the local average values of the currents in the boost inductors are calculated as

$$\langle i_k \rangle = \frac{1}{2} \left(\Delta i_{k1} T_1 + (\Delta i_{k1} + \Delta i_{k2x}) T_{2x} + (\Delta i_{k1} + \Delta i_{k2x} + \Delta i_{k3}) T_3 + (\Delta i_{k1} + \Delta i_{k2x} + \Delta i_{k3} + \Delta i_{k4}) T_4 \right) f_s \tag{5}$$

with x being either A or B. In order to obtain sinusoidal input currents, the rectifier has to act like a symmetric three-phase resistive load concerning the local current average values $\langle i_k \rangle$. Therefore, it is required that for each phase k the resistance $r_k = \frac{u_k}{\langle i_k \rangle}$ is the same, i.e., $r_k = r$. Assuming $\sum_k u_k = 0$ and $\sum_k i_k = 0$, this condition is guaranteed if the resistances of two phases are the same. Therefore, solving the equation

$$\frac{u_a}{\langle i_a \rangle} = \frac{u_b}{\langle i_b \rangle} \tag{6}$$

with the local average values of the currents inserted from (5), yields the value of D_{2A} or D_{2B} (as defined in Table I) that is necessary for resistive behavior, i.e., sinusoidal input currents after filtering switching frequency components. The value of D_1 follows by inserting the values D_{2A} or D_{2B} obtained from (6) into any of the equations $r = \frac{u_k}{\langle i_k \rangle}$ for a required resistance r at the mains side. In order to normalize the resistance r emulated to the mains and the phase voltages, and in order to include the 30° symmetry of the three phase system

$$D_0 = \sqrt{\frac{f_s L}{r}} \tag{7}$$

$$m_{max} = \frac{2 \cdot \max(|u_a|, |u_b|, |u_c|)}{U_{pn}} \tag{8}$$

$$m_{min} = \frac{2 \cdot \min(|u_a|, |u_b|, |u_c|)}{U_{pn}} \tag{9}$$

are introduced. Using these expressions the duty cycles for switching pattern B are obtained as

$$D_{1B} = D_0 \sqrt{2 - 2m_{max} + m_{min}} \tag{10}$$

$$D_{2B} = D_0 \sqrt{2 - 3m_{min}} - D_{1B}. \tag{11}$$

The expressions for the duty cycles for pattern A are provided in Appendix due to the complexity of the terms. Because of that a realization of the control scheme in hardware is only possible by using look-up tables of the relative duty cycles $d_{1A} = \frac{D_{1A}}{D_0}$, $d_{2A} = \frac{D_{2A}}{D_0}$ and $d_{1B} = \frac{D_{1B}}{D_0}$, $d_{2B} = \frac{D_{2B}}{D_0}$. With the modulation index $M = \frac{2\hat{u}}{U_{pn}}$ the relative duty cycles are shown in Fig. 9. It is observed, that the functions are smooth and continuous, and therefore, well suited for implementation using look-up tables. It is observed that for high values of the modulation index, the duty cycle functions (18,19,10,11) result in negative values. Numerical investigations show that all duty cycle values are

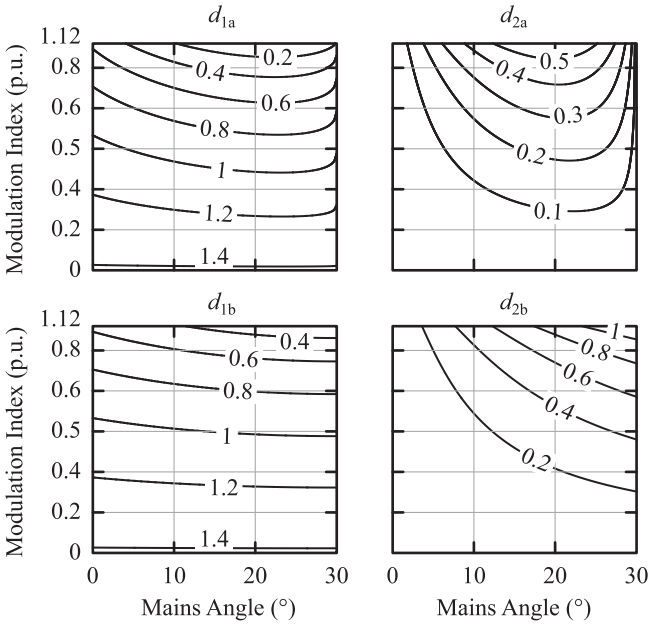


Fig. 9. Relative duty cycles $d_k = \frac{D_k}{D_0}$ for resistive behavior of the VR in DCM for switching patterns A and B as function of modulation index and mains angle.

valid for modulation indices up to $M \leq 1.12$, which is slightly less than the maximum modulation index of $M_{\max,\mathrm{ccm}} = \frac{2}{\sqrt{3}} \approx 1.15$ that the rectifier could theoretically be operated with in CCM [15]. However, also in CCM this modulation index can not be reached since a small voltage reserve is necessary to maintain current control.

E. DCM/CCM Threshold

Since the rectifier is operating at constant switching frequency, the total time T for all states is limited to

$$T = T_1 + T_{2x} + T_3 + T_4 < \frac{1}{f_\mathrm{s}}. \tag{12}$$

According to (7) the duration of each state is proportional to $\frac{1}{\sqrt{r}}$. Therefore, the resistance, which can be emulated for the mains in DCM is limited. This resistance value marks the threshold between CCM and DCM operation. By solving (12), the minimum resistance which can be emulated for the mains during a switching period with pattern B is obtained as

$$r_{\min,\mathrm{B}} = \frac{4 f_\mathrm{s} L}{2 + m_{\min} - 2 m_{\max}} \tag{13}$$

with the switching frequency f_s, the boost inductance L, and $m_{\max}$ and $m_{\min}$ as defined in (9) and (8). It is possible to find an analytic expression for $r_{\min,\mathrm{A}}$ for pattern A using symbolic math software, however, the result is too complicated to be shown here. Instead, it shall be mentioned that numerical investigations reveal that

$$r_{\min,\mathrm{A}} < 1.1 r_{\min,\mathrm{B}}. \tag{14}$$

However, one is usually only interested in the minimum resistance, which is achievable with both patterns A and B throughout

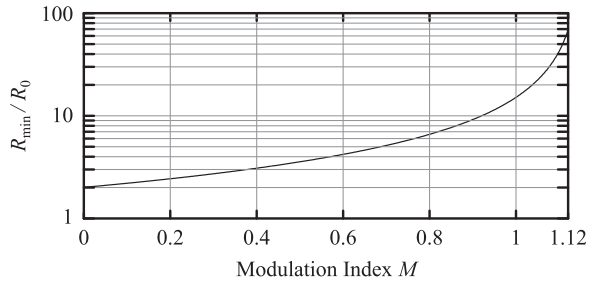


Fig. 10. Minimum resistance that can be emulated for the mains throughout the whole mains period using the DCM patterns A or B related to the base $R_0 = f_\mathrm{s} L$.

the whole mains period at a certain modulation index M. The exact value

$$R_{\min}(M) = \max_{\varphi \in [0°, 30°]} (r_{\min,\mathrm{A}}(M,\varphi), r_{\min,\mathrm{B}}(M,\varphi)) \tag{15}$$

is shown in Fig. 10. It can be approximated with less than 1% error as

$$R_{\min}(M) \approx \frac{4 f_\mathrm{s} L}{2 - \sqrt{3} M}. \tag{16}$$

Therefore, the maximum power that can be transferred by using both patterns A and B throughout the whole mains period, is estimated with less than 1% error as

$$P_{\max} \approx \frac{3 \hat{u}^2}{4 f_\mathrm{s} L} \left(1 - \frac{\sqrt{3}\hat{u}}{U_\mathrm{pn}}\right) \tag{17}$$

with the mains phase voltage amplitude $\hat{u}$, the switching frequency f_s, the boost inductance L, and the dc-link voltage U_pn. The minimum resistance, which is achievable in DCM marks the threshold for the phase current controllers to switch to DCM. To avoid that the controller constantly switches between CCM and DCM a hysteresis has to be implemented, so that DCM is only entered if the voltage controller requires a resistance of, e.g., $2R_{\min}$, and CCM is only re-entered if the required resistance drops below $R_{\min}$. Using such a hysteresis for the selection of the current control mode requires that the operating ranges for DCM and CCM are overlapping. That is, actually the case since at the value $R = R_{\min}$ the current ripple in DCM is approximately twice as high than it is in CCM. Therefore, operation in CCM with satisfactory input current quality is possible for emulated mains resistance values up to $2R_{\min}$.

F. DC-Link Balancing and Midpoint Current Limit

Since the direction of the current injected into the dc-link midpoint (midpoint current i_m) differs between switching patterns A and B, the ratio between the two dc-link voltages can be controlled by selecting the appropriate switching pattern. For equal voltage sharing between the two parts of the dc-link, bang–bang control can be used with the rule for selecting the switching pattern as specified in Table II. Applying this control in an idealized circuit simulation results in a boost inductor current waveform as shown in Fig. 11(a). By comparing the shape of the current ripple with Figs. 6 and 8, the continuous alternation of the switching pattern can be observed. Also, the

TABLE II
DC-LINK VOLTAGE BALANCING CONTROL RULE

	$u_\mathrm{p} > u_\mathrm{n}$	$u_\mathrm{p} < u_\mathrm{n}$
$\max(u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}) + \min(u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}) > 0$	Pattern A	Pattern B
$\max(u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}) + \min(u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}) < 0$	Pattern B	Pattern A

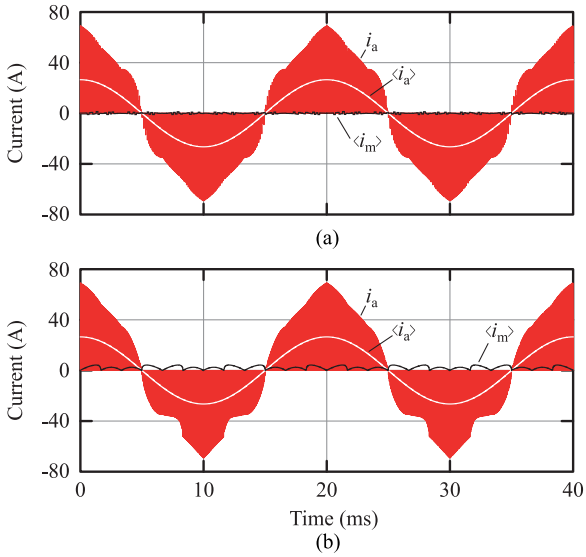


Fig. 11. Simulated boost inductor current, its local average value and the low-pass filtered midpoint current with output voltage balancing control and symmetric loading of the two dc-links. (a) With maximum permissible asymmetric loading (more load on negative dc-link). (b) Operating condition and parameters used for the simulation: $\hat{u} = \sqrt{2} \cdot 230$ V, $U_\mathrm{pn} = 800$ V, $f_\mathrm{s} = 28$ kHz, $L = 50$ µH, $P = P_\mathrm{p} + P_\mathrm{n}$ with $P_\mathrm{p} = P_\mathrm{n} = 6.5$ kW in (a) and $P_\mathrm{p} = 5.6$ kW and $P_\mathrm{n} = 7.4$ kW in (b).

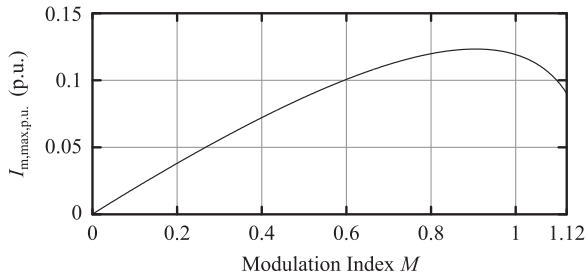


Fig. 12. Maximum average midpoint current that can be supplied into the midpoint of the dc-link relative to the phase current fundamental RMS value.

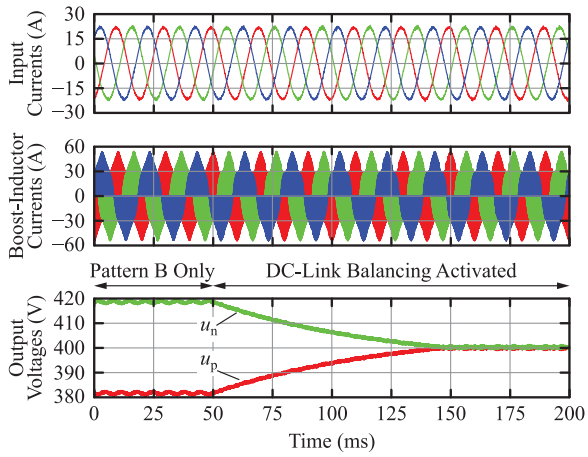


Fig. 13. Effect of proposed DCM dc-link balancing scheme, activated at $t = 50$ ms, with 30.4 Ω on the upper and 33.6 Ω on the lower dc-link after initial operation using pattern B only.

(low-pass filtered) midpoint current is virtually eliminated. If the two parts of the dc-link are loaded with slightly different loads or if there are different parasitic leakage currents present, the VR has to supply a steady-state average midpoint current throughout the mains period I_m. In CCM, the amount of midpoint current that can be supplied is proportional to the phase current amplitude and reduces with increasing modulation index [16]. At a modulation index $M = 1$, approximately 45% of the phase rms current amplitude can be supplied into the midpoint. In DCM, the current, which can be supplied to the midpoint by switching between patterns A and B is also limited. The maximum positive midpoint current is generated if state 2A is always used, while the phase voltage with the smallest absolute value is negative and state 2B is always used, while the phase voltage with the smallest absolute value is positive. The boost inductor current waveform for this situation is shown in Fig. 11(b). An asymmetry in the shape between positive and negative half-period of the boost inductor current can be observed but the local average value is sinusoidal. The average value related to the mains period of this maximum midpoint current can be found only numerically. Using the RMS value of the phase current fundamental I_p for normalization, the maximum relative midpoint current $I_\mathrm{m,max,p.u.} = \frac{I_\mathrm{m,max}}{I_\mathrm{p}}$ results, which is shown in Fig. 12 as a function of the modulation index M. It is observed that the maximum midpoint current for typically used modulation indices in the range of $M \in [0.6, 1.1]$ amounts to at least 10% of the phase current rms value. This is substantially less than the value, which is possible in CCM (cf. [16]), but sufficient to cover asymmetric leakage currents and to recover from a transient dc-link voltage unbalance. In the following either pattern A or B is selected according to Table II, which is the proposed control scheme of the VR in DCM with equal dc-link voltages. A circuit simulation of the prototype constructed within this work is used to demonstrate the functionality of the proposed balancing scheme to maintain symmetric output voltages with asymmetric load. The situation is shown in Fig. 13. At 400 V mains voltage and 800 V dc-link voltage, the rectifier is loaded with 30.4 Ω on the upper and 33.6 Ω on the lower dc-link (32 Ω ±5%). Initially, pattern B is applied constantly, i.e., the dc-link balancing scheme is turned off. At $t = 50$ ms the balancing scheme is activated, symmetrizing the output voltages within ≈ 100 ms with 2 × 2.3 mF dc-link capacitance. The shape of the main currents is not affected during the transition, however, the boost inductor current ripple shape changes slightly as soon as the dc-link balancing control is activated.

G. Noise Emission

If the proposed DCM control scheme is used all switches are turned ON at the same time, whereas in CCM operation the switches of positive and negative boost stages are operated with

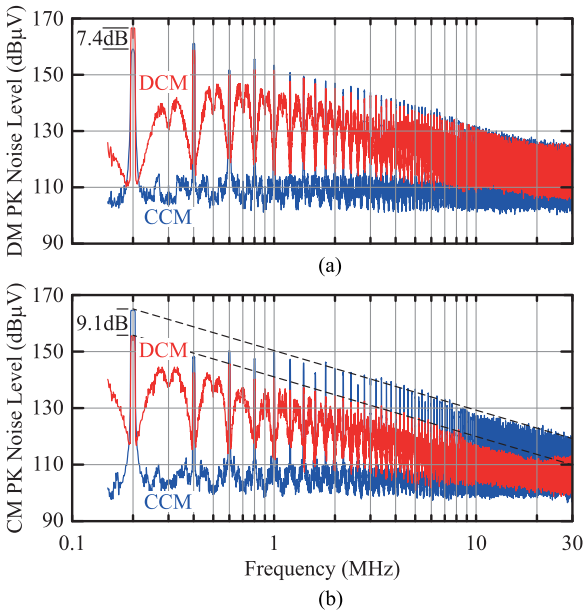


Fig. 14. Simulated noise emission detected with a CISPR11 peak receiver for the VR operating in CCM (blue) and in DCM (red) with 400V mains line-to-line RMS input voltage and 800 V output voltage. The DM noise with peak (PK) detection is shown in (a). It is observed that the DM noise in DCM at switching frequency is higher than in CCM. However, the noise levels at higher frequencies in DCM are the same or a little lower than in CCM. The CM noise with PK detection is shown in (b). It is shown that the CM noise level in DCM is lower than in CCM at all frequencies.

180° pulse width modulation (PWM) carrier phase shift. Therefore, higher differential mode (DM) and lower common mode (CM) conducted noise emission is expected. For the design of the input filter the noise spectrum as measured with an EMI test receiver is relevant. Therefore, for the comparison of the noise levels in CCM and DCM, the DM and CM noise parts of the simulated rectifier input voltages are separately fed into a simulated [17] peak detection test receiver according to CISPR11 [18]. The switching frequency of the simulated circuit is set to 200 kHz for this analysis such that the full PWM spectrum is evaluated by the CISPR detector. The resistance that the rectifier applies to the mains is set to the lowest value ($R_{\min}$), which represents the case of highest noise emission. Both switching patterns A and B are used to balance the output voltage using bang–bang control. The resulting noise spectra are shown in Fig. 14. It is confirmed that in DCM the DM noise at switching frequency is 7.4 dB higher than in CCM. At higher frequencies, however, the DM noise levels in DCM and CCM are comparable. On the other hand, the CM noise level in DCM is lower by 9.1 dB at all frequencies compared to CCM. Therefore, if the switching frequency is less than 150 kHz, which is the lowest frequency, for which CISPR defines noise emission limits, the rectifier can be operated in DCM using an EMI filter designed for CCM. If the switching frequency exceeds the 150 kHz threshold, the DM attenuation of the filter has to be increased by $\approx$ 7.4 dB.

III. Experiments

The prototype constructed for the experiments is optimized for the high peak, low average load scenario of an X-ray system as described in Section I. The specifications of the system are provided in Table III. The wide input voltage range is required since the system shall be used with weak grids even at 20% under voltage and with 10% over voltage with 400 or 480 V nominal voltage. Although the application only requires the full power for 10 s and only 1 kW continuously, for better comparability the system is designed for full power continuous operation. Thus, for the actual application the semiconductor cooling system could be much smaller. The inductor size, however, is determined by a TCO optimization, which considers the loss energy cost during the expected system life time of 20 years. In order to allow sufficient cooling, the semiconductors are directly soldered to aluminium core PCBs (insulated metal substrate), which are mounted to the heat sinks as shown in Fig. 15(b). Helically wound rectangular conductor profile windings are used for boost and filter inductors due to the excellent filling factor and HF performance of this type of winding and also since they allow efficient cooling. The inductors are connected by using busbars in order to avoid that the input currents, which can amount to up to 135 A RMS at the lowest input voltage, are conducted through the PCB, which only carries the dc output currents.

TABLE III
Prototype Specifications

Input voltage range	290–530 V
Output voltage	800 V
Output power	65 kW
Ambient temperature	45°C

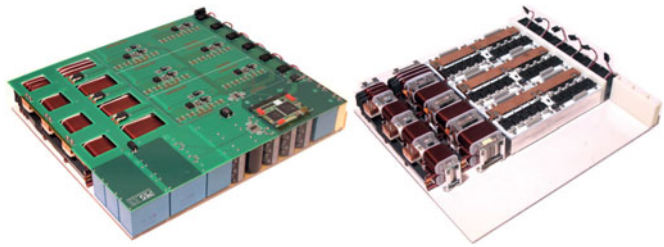


Fig. 15. 65 kW/28 kHz VR prototype used for the measurements to verify the proposed DCM control scheme. (a) Inside view showing CM and DM inductors of the two stage EMI filter (including the boost inductors) and semiconductors mounted to the heat sink using aluminium PCBs (b) Width × length × height = 33.6 cm × 37.4 cm × 5.4 cm (13.2 in × 14.7 in × 2.13 in), power density $\varrho = 9.56$ kW/dm^3 (157 W/in^3).

A. Switching Period Waveforms

The measured waveforms of boost inductor current and rectifier input voltage for a mains voltage angle of 10° (from the start of the 30° sector $u_a > 0 > u_b > u_c$) at 4.8 kW with 400 V line-to-line RMS input voltage and 800V dc output voltage are shown in Fig. 16. The measurement shows a switching period of pattern A followed by switching period with pattern B, the selection of the switching pattern is performed by the DSP in order to balance the output voltages according to Table II. In pattern A phase c, the one with middle absolute voltage, is turned OFF

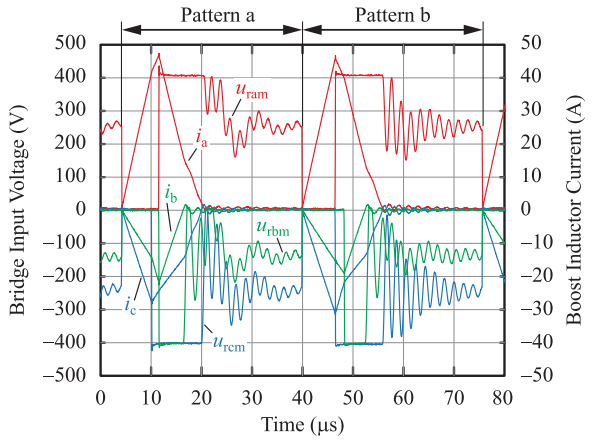


Fig. 16. Measured waveforms of the boost inductor currents and the rectifier input voltages with reference to the dc-link midpoint at the mains voltage sector $u_a > 0 > u_b > u_c$ with 4.8 kW output power, 400 V line-to-line RMS input voltage and 800 V dc output voltage.

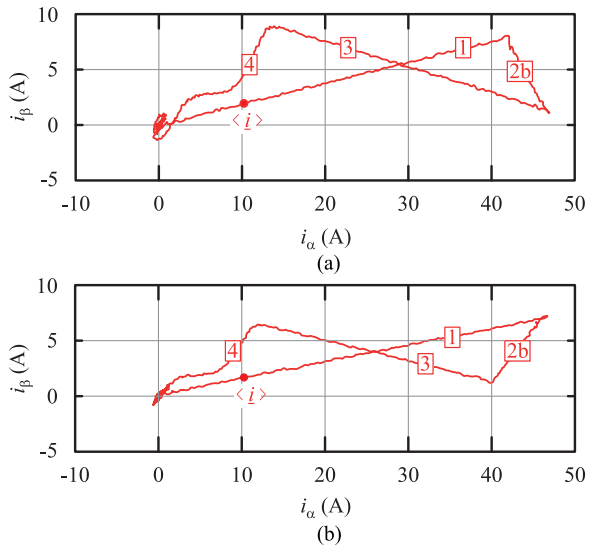


Fig. 17. Measured trajectories of the boost inductor currents with pattern A (a) and pattern B (b) displayed in α, β coordinates and the local average of each trajectory $\langle \underline{i} \rangle$ at the mains voltage sector $u_a > 0 > u_b > u_c$ with 4.8 kW output power, 400 V line-to-line RMS input voltage and 800 V dc output voltage.

first, in pattern B phases a and c are turned OFF before phase b, the one with minimum absolute value. During the current zero interval ringing of the IGBT output capacitance with the boost inductance is observed, which is initiated by the reverse recovery current of the free-wheeling diode.

Displaying the measured data of the boost inductor currents with switching pattern A in α, β coordinates results in the trajectory shown in Fig. 17(a) and for pattern B in the trajectory shown in Fig. 17(b). The switching state of each part of the trajectory is indicated. During state $\boxed{1}$ the boost inductor current space vector moves from the origin into the direction of the mains voltage space vector. As can be seen, the local average of the measured boost inductor current space vector $\langle \underline{i} \rangle$ is located on this part of the trajectory, and therefore, has the same angle as the mains voltage space vector indicating that the desired resistive behavior is achieved.

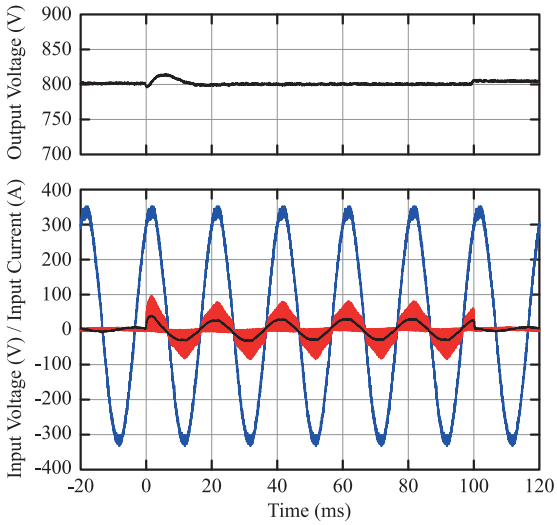


Fig. 18. Measured waveforms of input voltage, boost inductor current and mains current of one phase in DCM using both patterns A and B according to Table II during a 100 ms load pulse with 13 kW output power (no load otherwise) at 400 V mains voltage and 800 V output voltage.

The controller used is a TI TMS320f28335 DSP, which calculates the duty cycles in DCM by using four look-up tables created offline using the expressions (18), (19), (10), and (11) evaluated for 12 values of $m_{\max}$ and seven values of $m_{\min}$. Bilinear interpolation is carried out on the DSP to reduce the error when retrieving values from the look-up tables.

B. Load Step Response

Since the rectifier is intended to be used with a high voltage generator for an X-ray tube, it is typically subjected to a pulsed load with pulse durations ranging from 1 ms to 10 s at full power. The controller is implemented in a cascaded structure. The outer loop contains the dc-link voltage controller, which sets the resistance to be emulated to the mains by the current controller, using the output current measurement for feed-forward. In CCM, the boost inductor currents are closed loop controlled using the input voltage measurements for feed-forward, in DCM, however, they are open loop controlled as described in Section II. A measured load pulse with 13 kW output power and 100 ms duration at 400 V mains voltage with 800 V output voltage set value is shown in Fig. 18. As can be seen, the rectifier is still operating in DCM at this power level, although it is close to the threshold to CCM since the input current is almost half the peak value of the boost inductor current. At full power, the rectifier is operating in CCM, the load pulse measured for this situation is shown in Fig. 19. The output voltage shows under- and overshoot of $\approx 5\%$ at the beginning, respectively, the end of the load pulse. A negligible low-frequency output voltage ripple is observed during the pulse caused by the nonconstant power flow resulting by the resistive behavior of the rectifier with not perfectly sinusoidal mains voltages.

C. Input Current THD

With the applied control schemes, the input currents in DCM and in CCM are ideally proportional to the phase voltages.

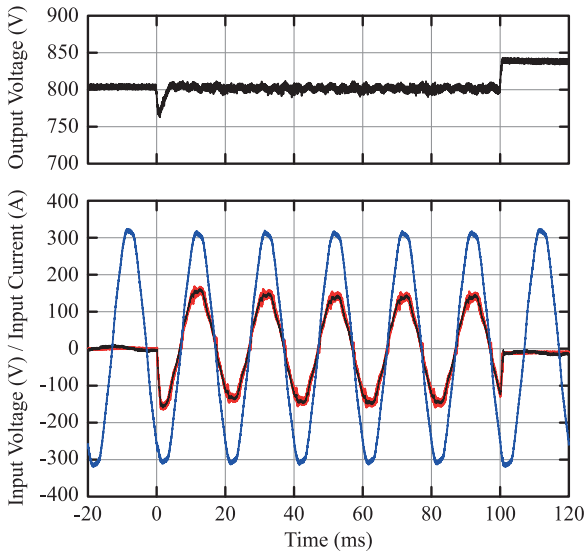


Fig. 19. Measured waveforms of input voltage, boost inductor current, and mains current of one phase in CCM during a 100 ms load pulse with 65 kW output power (no load otherwise) at 400 V mains voltage and 800 V output voltage.

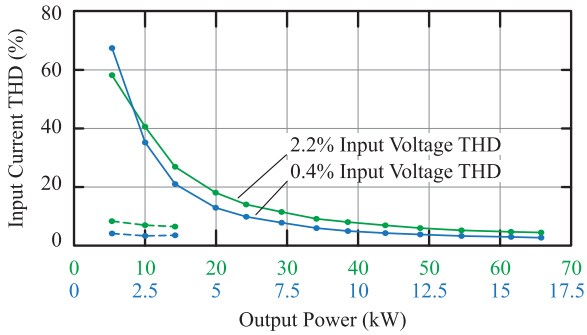


Fig. 20. Measured mains current THD at nominal voltage (green: 400 V line-to-line input voltage, 800 V output voltage) with 2.2 % voltage THD and at half nominal voltage (blue: 200 V line-to-line input voltage, 400 V output voltage) with 0.4 % voltage THD. Solid lines indicate measurements taken with closed loop CCM current control, dashed lines with the proposed open loop DCM current control.

Therefore, the input current THD is ideally the same as the voltage THD. However, in CCM the THD increases if the load is reduced due to two reasons. First, the DCM occurring at the current zero crossings causes disturbances in the current control loop due to inaccurate current measurements and the change in duty cycle voltage relationship. Second, the necessary low-pass filtering of the input voltage measurements leads to a difference between the actual and the feed-forwarded input voltage, in particular if the input voltage THD is high. This error in the feed-forwarded input voltage acts as disturbance in the current control loop. Both reasons combined lead to the increase in current THD in CCM at light load. With a mains voltage THD of 2.2 %, the measured input current THD is shown in Fig. 20. At 400 V line-to-line RMS voltage, 800 V output voltage, and 66 kW load the input current THD amounts to 4.5 %. In order to be able to use a linear three-phase ac power source that provides 0.4 % voltage THD but features only 20 kW output power, the

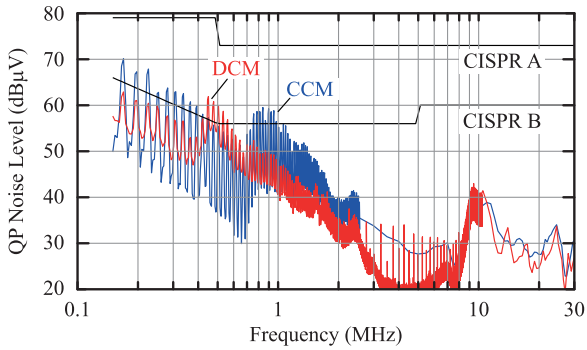


Fig. 21. Measured CISPR QP noise level at nominal voltages and a load of 20 kW in CCM and 5 kW in DCM. The measurements are conducted using an additional 390 µH CM inductor at the mains side of the filter to compensate for the loss of permeability of the nano-crystalline inductors at high frequencies not considered during the filter design.

power is reduced to $\frac{1}{4}$ of the rated value using 200 V line-to-line RMS voltage and 400 V output voltage. Since the load impedance remains unchanged, the relative current ripple is the same as with full power and nominal voltages. In this case, with 16.5 kW load, which represents the full load condition, the input current THD is reduced to 2.7 %.

At load levels of 15 kW or less, the rectifier can be operated using the closed loop CCM current control or the proposed open loop DCM control scheme (dashed line). The improvement of the input current THD with the proposed control scheme is significant, allowing to reduce the input current THD at nominal voltages and 15 kW from 26.9 % to 6.5 % with 2.2 % input voltage THD and with half the nominal voltages and 3.75 kW load at 0.4 % voltage THD from 21% to 3.5 %.

At medium power levels the input current THD, however, is still high owing to the synchronous sampling with twice the switching frequency. In order to reduce the THD further without increasing the value of the boost inductance or the switching frequency would require changes to the hardware such as using ADCs with higher sampling rates.

D. Conducted EMI Measurement

From the simulations discussed in Section II-G, it is expected that the noise emission in DCM is lower than in CCM due to the lower CM noise level. The measurements shown in Fig. 21 taken at 5 kW in DCM and at 20 kW in CCM with nominal voltages basically confirms this statement except for the frequency range from 400 to 600 kHz. This is explained by the oscillation of the output capacitance of the IGBTs with the boost inductance in DCM as it is observed in Fig. 16, which is taking place at a frequency of $\approx$ 500 kHz. The power level for CCM operation had to be selected higher than the one for DCM operation to make sure the converter actually operates fully in CCM and no unwanted DCM as in Fig. 2 occurs. Except for the switch $\frac{\mathrm{d}v}{\mathrm{d}t}$, the noise emission does not depend on the power level in CCM. Initially, a two stage DM and CM filter has been designed as shown in Fig. 22. However, because of the reduction in permeability of the nano-crystalline cores for frequencies higher than 100 kHz, which was not considered during the filter

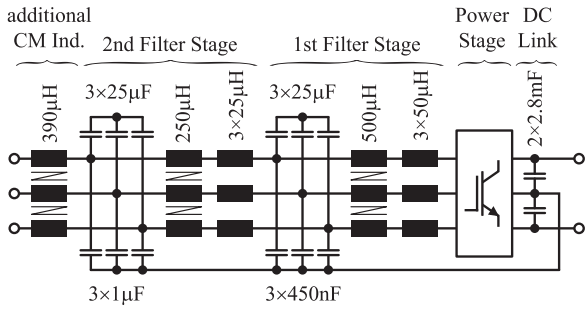


Fig. 22. Structure and component values of the two stage CM and DM EMI filter of the prototype using a capacitive CM return path to the dc-link midpoint, damping resistors not shown. The additional CM inductor at the mains side of the filter is necessary to comply with CISPR Class A.

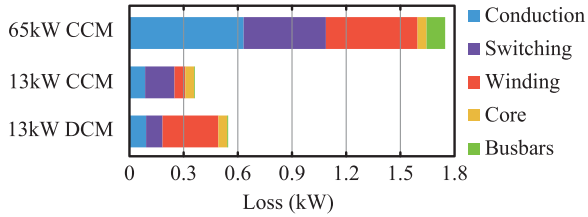


Fig. 23. Loss distribution at nominal voltages (400 V line-to-line RMS input voltage, 800 V output voltage) for selected operating points.

design process, an additional toroidal CM inductor of 390 µH had to be added at the mains side of the filter to comply with CISPR Class A.

E. Loss Distribution and Efficiency

Operation of the VR with the proposed DCM scheme has two major effects on the losses. First, turning on the switches at the same time leads to a higher DM voltage component at switching frequency and thus to a higher current ripple. The helical windings used for the boost inductors suffer from a high ac to dc resistance ratio at switching frequency, which amounts to $\frac{R_{\mathrm{ac}}(28\,\mathrm{kHz})}{R_{\mathrm{dc}}} \approx 38$ according to a FEM simulation. While, this is acceptable in CCM due to the low current ripple, the high current ripple in DCM leads to a significant increase in winding loss. This effect is observed in the calculated loss distribution shown in Fig. 23 for the operating point at 13 kW, which is shown for CCM and DCM operation. On the other hand in CCM, the CM voltage component is higher. Because of the high CM inductance virtually no CM current ripple is observed, but the higher CM voltage causes higher core losses in the CM inductor of the first filter stage than in DCM. The core losses in the DM inductors are, however, higher in DCM than in CCM due to the higher DM voltage component in DCM. Therefore, in DCM, the core losses are kind of shifted from the CM inductor of the first filter stage into the boost inductors and, according to the calculations presented in Fig. 23, remain approximately the same in total. The second effect on the losses in DCM concerns the switching losses. Since the transistors are turned on at zero current lower turn-on losses result compared to CCM. Since the turn-on losses are higher than the turn-off losses with the IGBTs [19] and the free-wheeling diodes [20] used, the total switching

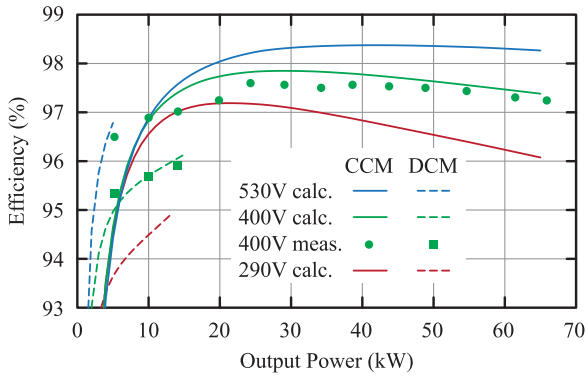


Fig. 24. Measured efficiency in DCM and CCM compared to the calculated values as function of the output power with nominal output voltage of 800 V.

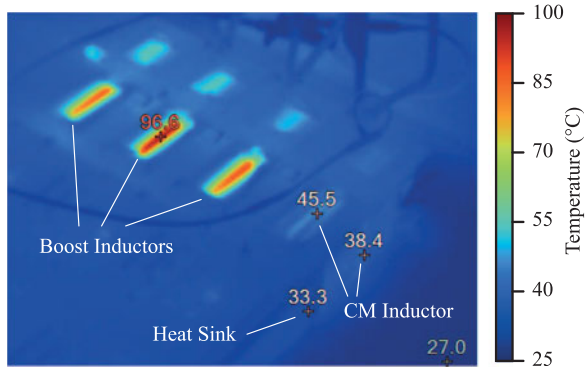


Fig. 25. Thermal image of the prototype running at 10 kW in DCM with nominal voltages. The hotspot is observed at the windings of the boost inductors near the airgap due to the high DM current ripple. The CM inductor and the heat sink temperatures are low.

losses in DCM are lower than in CCM as shown in Fig. 23. The measured efficiency at nominal voltages depending on the load is shown for CCM and DCM in Fig. 24 and compared to the calculated values. The calculations are based on data sheet values for forward voltage drop and switching losses of the semiconductors, core loss data provided by the manufacturers adapted for the actual flux density waveform using iGSE [21] and FEM simulations of the windings for the ac/dc resistance ratio. With CCM the measured efficiency fits the calculated value with less than 0.3 % deviation at medium to high load reaching 97.2 % at full load and a peak of 97.6 % at 24 kW. At low load the error with CCM control is growing, which can be explained by the partially occurring DCM in this region not covered by the loss model. With the proposed open loop DCM control scheme the measured efficiency is lower by up to 1.3 % due to the increased current ripple. Temperature measurements are carried out using a thermal camera. The first filter stage inductors temperatures demonstrate the effect of high DM voltage with DCM control and high CM voltage with CCM control. With 10 kW in DCM the thermal image is shown in Fig. 25. Due to the high current ripple the DM inductor windings heat up to 97°C in the vicinity of the airgap, which is relatively wide with 4.5 mm. The CM inductor in this situation only heats up to 46°C on the winding. In CCM with 32 kW output power the picture changes as shown

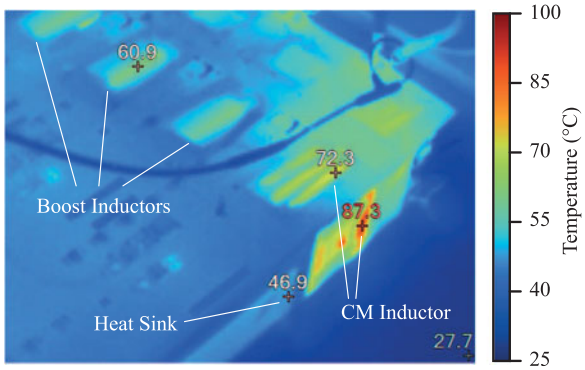


Fig. 26. Thermal image of the prototype running at 32 kW in CCM with nominal voltages. The hotspot is moved to the core of the CM inductance, due to the higher CM voltage amplitude in CCM.

in Fig. 26. As expected the higher CM voltage causes the CM inductor core to heat up to 87°C, due to the low current ripple the temperature of the DM inductor winding drops to 61°C even though the load is higher than in the situation of Fig. 25. The heatsink temperature at 32 kW is still low with 47°C. However, power levels higher than 40 kW could not be tested in continuous operation since the PCB close to the dc terminals heats up excessively.

IV. Conclusion

It has been shown that an open loop DCM current control scheme for the VR exists that allows resistive mains behavior. The expressions for the duty cycles can be derived analytically and are suitable for hardware implementation using look-up tables. Simulations and measurements show that a substantial reduction of input current THD is possible at light load, which for the prototype with $\approx 25\%$ inductor current ripple at nominal load can be considered as less than 20% of nominal load. Compared to conventional PI current control the proposed DCM control scheme achieves a THD reduction from 20% to less than 5%. The proposed control scheme does not rely on current measurements. Therefore, it is not necessary to resolve the actual local average of the inductor current in DCM. Other than common light load handling approaches, such as burst mode operation or increasing the switching frequency at light load, the proposed control scheme allows to operate continuously, therefore, with minimum output voltage ripple, and due to the constant switching frequency the requirements for the EMI filter are not affected if the switching frequency is less than the CISPR threshold of 150 kHz. If the switching frequency is higher, 7.4 dB more DM attenuation is required. Balancing of the output voltages is possible with the proposed control scheme by selecting the appropriate one of two redundant switching patterns and for typical modulation indices a dc current of 10% of the phase current RMS value can be delivered to the dc-link midpoint. The higher current ripple of the proposed control scheme leads to higher HF winding losses in the inductors of the first filter stage. However, zero current turn-on reduces the switching losses. The proposed control scheme is implemented and verified on a 65 kW prototype optimized for pulse load reaching 97.2 % efficiency at nominal load and 9.56 kW/dm^3 power density using only low cost Si components with 28 kHz switching frequency.

Acknowledgment

The concepts and information presented in this paper are based on research and are not commercially available.

Appendix

For switching pattern A, the relative duty cycles are

$$D_{1A} = \frac{D_0}{\sqrt{y}} \cdot \big((9m_{\min}^2 + 6m_{\min} + 2)m_{\max} - (6m_{\min} + 2)m_{\max}^2 - 3m_{\min}^3 - 4m_{\min}^2\big) \quad (18)$$

and

$$D_{2A} = D_{1A} \cdot (9m_{\min}^2 m_{\max} - 2m_{\min}^2 - \sqrt{x} - 6m_{\min}m_{\max}^2 + 4m_{\max}m_{\min} - 3m_{\min}^3) \div (3m_{\min}^3 - 9m_{\min}^2 m_{\max} + 4m_{\min}^2 - 2m_{\max} + 6m_{\min}m_{\max}^2 - 6m_{\max}m_{\min} + 2m_{\max}^2) \quad (19)$$

with

$$x = (2m_{\max} - 2 - m_{\min})m_{\min}(3m_{\min} - 2) \cdot (2m_{\max} - m_{\min})(m_{\max}^2 - m_{\min}^2) \quad (20)$$

and

$$y = 3m_{\min}^5 + m_{\min}^4(7 - 15m_{\max}) + m_{\min}^3(24m_{\max}^2 - 23m_{\max} + 2) + m_{\min}^2(20m_{\max}^2 - 8m_{\max} - 12m_{\max}^3) + m_{\min}(\sqrt{x} - 4m_{\max}^3 + 6m_{\max}^2) + m_{\max}(\sqrt{x} + 2m_{\max} - 2m_{\max}^2). \quad (21)$$

References

[1] F. H. Attix, *Introduction to Radiological Physics and Radiation Dosimetry*. Weinheim, Germany: Wiley, 2004.

[2] H. Krieger, *Strahlenphysik, Dosimetrie und Strahlenschutz - Band 2: Strahlungsquellen, Detektoren und klinische Dosimetrie*. Stuttgart, Germany: B. G. Teubner, 1997.

[3] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Proc. Int. Conf. Power Electron. Drive Syst.*, May 1997, vol. 1, pp. 425–430.

[4] R. Burkart and J. W. Kolar, "Overview and comparison of grid harmonics and conducted EMI standards for LV converters connected to the MV distribution system," in *Proc. 1st Int. Conf. Exhib. Power Electron. Intell. Motion Renew. Energy Energy Manage. Power Electron. South Amer.*, Sep. 2012.

[5] J. W. Kolar and T. Friedli, "The essence of three-phase PFC rectifier systems—Part I," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 176–198, Jan. 2013.

[6] J. W. Kolar and F. C. Zach, "A novel three-phase utility interface minimizing line current harmonics of high-power telecommunications rectifier modules," *IEEE Trans. Ind. Electron.*, vol. 44, no. 4, pp. 456–467, Aug. 1997.

[7] H. Uemura, F. Krismer, Y. Okuma, and J. W. Kolar, "$\eta - \rho$ pareto optimization of three-phase three-level T-type ac-dc-ac converter comprising Si and SiC hybrid power stage," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 2834–2841.

[8] J. W. Kolar and W. Korb, "Device and method for line-voltage dependent thyristor controlled pre-charging of output capacitors in a three-level pulse rectifier system," *U.S. Patent 6 377 482*, Apr. 23, 2002. [Online]. Available: https://worldwide.espacenet.com/publicationDetails/biblio?FT=D&date=20020423&DB=EPODOC&locale=en_EP&CC=US&NR=6377482B1&KC=B1&ND=5
[9] M. Leibl and J. W. Kolar, "Comparative analysis of inductor concepts for high peak load low duty cycle operation," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 899–906.
[10] S. F. Lim and A. M. Khambadkone, "A simple digital DCM control scheme for boost PFC operating in both CCM and DCM," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1802–1812, Jul. 2011.
[11] P. Ide, N. Froehleke, H. Grotstollen, W. Korb, and B. Margaritis, "Analysis of three-phase/three-level rectifiers at low load and discontinuous conduction mode," in *Proc. 15th IEEE Appl. Power Electron. Conf.*, 2000, pp. 197–204.
[12] J. W. Kolar, H. Ertl, and F. C. Zach, "Space vector-based analytical analysis of the input current distortion of a three-phase discontinuous-mode boost rectifier system," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 733–745, Nov. 1995.
[13] P. Ide, F. Schafmeister, N. Frohleke, and H. Grotstollen, "Enhanced control scheme for three-phase three-level rectifiers at partial load," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 719–726, Jun. 2005.
[14] M. Leibl, J. W. Kolar, and J. Deuringer, "New current control scheme for the vienna rectifier in discontinuous conduction mode," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2014, pp. 1240–1247.
[15] M. Hartmann, "Ultra-compact and ultra-efficient three-phase PWM rectifier systems for more electric aircraft," *Ph.D. dissertation, Power Electron. Syst. Lab., ETH Zurich, Zurich, Switzerland*, 2011.
[16] J. W. Kolar, U. Drofenik, and F. C. Zach, "Current handling capability of the neutral point of a three-phase/switch/level boost-type PWM (vienna) rectifier," in *Proc. 27th IEEE Power Electron. Spec. Conf.*, 1996, pp. 1329–1336.
[17] M. L. Heldwein, "EMC filtering of three-phase PWM converters," *Ph.D. dissertation, Power Electron. Syst. Lab., ETH Zurich, Zurich, Switzerland*, 2007.
[18] *International Special Committee on Radio Interference–C.I.S.P.R., Geneva, Switzerland*, "Specification for industrial, scientific and medical (ISM) radio-frequency equipment—electromagnetic disturbance characteristics—limits and methods of measurement—publication 11," 2004.
[19] *Infineon Technologies AG*, "IGW50N65F5—650V IGBT high speed switching series 5th generation," May 2015, rev. 2.1.
[20] *Infineon Technologies AG*, "IDW40E65D1—Emitter controlled diode rapid1 series," Dec. 2013, rev. 2.2.
[21] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *Proc. IEEE Workshop Comput. Power Electron.*, Jun. 2002, pp. 36–41.

Michael Leibl (M'12) received the B.Sc. degree in electrical engineering from the Vienna University of Technology, Vienna, Austria, in 2010 and the M.Sc. degree in electrical engineering from the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in 2012. He is currently working toward the Ph.D. degree in power electronics at the Power Electronic Systems Laboratory, ETH Zurich.

His research interests include optimized design of inductive components, in particular modeling high frequency winding loss, high power three-phase PFC rectifiers, and isolated dc–dc converters.

Johann W. Kolar (F'10) received the M.Sc. degree in industrial electronics and control engineering and the Ph.D. degree (*summa cum laude*) in electrical engineering both from the Vienna University of Technology, Vienna, Austria, in 1997 and 1999, respectively.

He is currently a Full Professor and the Head in the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland. He has proposed numerous novel PWM converter topologies and modulation and control methods (e.g., the vienna rectifier, the sparse matrix converter, and the SWISS rectifier). His research interest include ultracompact and ultraefficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, as well as ultrahigh speed and ultralight weight drives, bearingless motors, and energy harvesting.

Dr. Kolar has supervised more than 60 Ph.D. and has published more than 750 scientific papers in international journals and conference proceedings, three book chapters, and has filed more than 140 patents. He received 25 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Power Electronics Society R. David Middlebrook Achievement Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2016 IEEE PEMC Council Award, and the ETH Zurich Golden Owl Award for excellence in teaching.

Josef Deuringer received the Dipl.-Ing. (M.Sc.) degree in electrical engineering from the Technical University Munich, Munich, Germany, in 1993 and the Dr.-Ing (Ph.D.) degree in electrical engineering from Friedrich-Alexander University Erlangen-Nrnberg, Erlangen, Germany, in 1998.

During his research activities he worked on high power microwave sources for laser applications. After that, he worked for Siemens AG on numerous industrial research and development projects for X-Ray tube beam control electronics and high-voltage generators with high-frequency resonant inverters. He has filed 19 patents in these areas. He is currently the Head of the Department Innovation Electronics and Control, Siemens Healthcare GmbH, business area diagnostic imaging.