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Comparative Evaluation of a Full- and Partial-Power Processing Active Power Buffer for Ultra-Compact Single-Phase DC/AC Converter Systems

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***Abstract*—One of the key technical challenges of the Google & IEEE Little Box competition, an international contest to build the world's smallest $2\,\mathrm{kW}$ single-phase inverter in 2015, was to shrink the volume of the energy storage required to cope with the twice mains-frequency ($120\,\mathrm{Hz}$) pulsating power at the AC side and meet the stringent $2.5\,\%$ input voltage ripple at the DC side. In this paper, first, a full-power processing buck-type converter active buffer approach, selected by the 1st prize winner of the Little Box Challenge (LBC) is analyzed in detail. Being relieved from strict voltage ripple requirements, a larger voltage ripple is allowed across the buffer capacitor significantly reducing the capacitance requirement. Second, a partial-power active buffer approach, selected by the 2nd prize winner of the LBC, where conventional passive capacitive buffering of the DC-link is combined with a series-connected auxiliary converter, used to compensate the remaining $120\,\mathrm{Hz}$ voltage ripple across the DC-link capacitance, is studied in detail. In this paper, both selected concepts are comparatively evaluated in terms of achievable efficiency, power density and ripple compensation performance under both stationary and transient conditions. Novel control schemes and optimally designed hardware prototypes for both considered buffer concepts are presented and accompanied with experimental measurements to support the claimed efficiency and power density and assess the performance of the implemented control systems. Finally, by means of comparison with conventional passive DC-link buffering using only electrolytic capacitors, it is determined at what voltage ripple requirement it actually becomes beneficial in terms of volume to employ the considered active buffer concepts.**

***Index Terms*—Power Pulsation Buffer, Active Power Decoupling, Series Voltage Injector, Partial-Power Converter, Google Little Box Challenge**

I. Introduction

In order to achieve a cost reduction in solar power and promote wide bandgap (WBG) power semiconductors for the next generation of high efficiency and ultra-compact power electronics, Google and IEEE launched the Little Box Challenge (GLBC, [1]) in 2015 aiming for a massive power density enhancement of a $2\,\mathrm{kW}$ single-phase DC/AC converter system compared to state-of-the-art technology, advertising $1 million prize money.

One of the key technical challenges in the implementation of the Google Little Box was to shrink the volume of the energy storage required to cope with the twice mains-frequency ($120\,\mathrm{Hz}$) pulsating power at the AC side while meeting the stringent $2.5\,\%$ ($10\,\mathrm{V}$ pk-pk)[1] input voltage ripple. The additional challenging technical requirements as listed in Tab. I and the attractive prize money created a remarkable interest in the power electronics community, which led to the participation of 2000+ teams – companies, research institutes, consultants and universities – in the GLBC. Finally, 100+ teams submitted technical descriptions of realized systems. Out of these applications, 18 finalists [2] were selected to present their technical approaches and hand over their prototypes to the National Renewable Energy Laboratory (NREL), Golden (Co), USA, for final testing. The team from the Belgian company CE+T Power was finally awarded the grand prize of $1 million for the most compact inverter passing all tests, e.g. also the 100 hours testing, achieving a power density of $8.72\,\frac{\mathrm{kW}}{\mathrm{dm}^3}$ ($142.9\,\mathrm{W/in}^3$) and a CEC weighted efficiency of

[1]The specified $20\,\%$ input current ripple limit (cf. Tab. I) is more stringent and, for the stated $R_\mathrm{s} = 10\,\Omega$ input resistor, implies a $2.5\,\%$ ($10\,\mathrm{V}$ pk-pk) limit for the maximal permissible $120\,\mathrm{Hz}$ input voltage ripple.

TABLE I
KEY INVERTER SPECIFICATIONS OF THE GOOGLE LITTLE BOX CHALLENGE.

Parameter	Requirement
Input Voltage Source	$450\,\mathrm{V_{dc}}$ with $R_\mathrm{s} = 10\,\Omega$
Output Voltage & Frequency	$240\,\mathrm{V_{rms}}$/$60\,\mathrm{Hz}$
Maximum Apparent Output Power S	$2\,\mathrm{kVA}$
Power Factor	$0.7\,\ldots\,1$, lead & lag
Maximum Load Steps	$500\,\mathrm{W}$
Power Density	$> 3\,\frac{\mathrm{kW}}{\mathrm{dm}^3}$ ($> 50\,\mathrm{W/in}^3$)
CEC Efficiency	$\geq 95\,\%$
Lifetime (Test Duration)	$> 100\,\mathrm{h}$
Max. Outer Enclosure Temperature	$\leq 60\,^\circ\mathrm{C}$
DC Input Voltage Ripple ($120\,\mathrm{Hz}$)	$\leq 2.5\,\%$ (i.e. $\leq 10\,\mathrm{V}$ pk-pk)
DC Input Current Ripple ($120\,\mathrm{Hz}$)	$\leq 20\,\%$ (i.e. $\leq 1\,\mathrm{A}$ pk-pk)
Ground/Leakage Current	$\leq 50\,\mathrm{mA}$ (initially $\leq 5\,\mathrm{mA}$)
Electromagnetic Compliance	FCC Part 15B/CISPR11 Class B
AC Output Voltage/Current THD	$<5\,\%$

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95.4 %. The 2nd and 3rd place was awarded to the team from Schneider Electric for achieving a power density of 6.1 $\frac{\text{kW}}{\text{dm}^3}$ (100 W/in^3) and to the team from Virginia Tech for achieving a power density of 4.3 $\frac{\text{kW}}{\text{dm}^3}$ (70 W/in^3) with their converter prototypes, respectively.

One strategy followed by the majority of the GLBC finalists to reduce the size of the energy storage, conventionally realized with passive capacitive DC-link buffering using bulky electrolytic capacitors, is to employ an additional converter with dedicated buffer capacitor to enable a wide feasible capacitor voltage fluctuation Δv_b which, according to

$$\Delta E = C_\text{b} \cdot V_\text{b} \Delta v_\text{b} \tag{1}$$

wherein ΔE denominates the alternately stored and released energy of the buffer, results in a significantly reduced buffer capacitance size C_b and thus lower overall converter volume despite the additional power electronic components. The winning team from CE+T Power selected the Parallel Current Injector (PCI) approach as shown in Fig. 1 (a), where the buffer converter connected in parallel at the converter DC input injects current i_b to compensate the fluctuating portion of current $i_\text{inu} = p_\text{ac}/V_\text{dc}$ which results in a constant input current i_s and consequently in a constant voltage at the converter input. The depicted setup with $V_\text{s} = 450\,\text{V}$ DC source and $R_\text{s} = 10\,\Omega$ input resistor was specified in the testing requirements of the GLBC [1], [2]. The synchronous buck-type implementation of the PCI converter with totem-pole bridge-leg, HF filter inductor and buffer capacitor as shown in Fig. 1 (c) was chosen by the team of CE+T Power from several available options discussed in literature [3]–[9].

A different approach as depicted in Fig. 1 (b) was followed by the 2nd prize winner of the GLBC [10]–[12]. In this approach, conventional passive capacitive buffering of the DC-link is used, however, the total installed capacitance value is

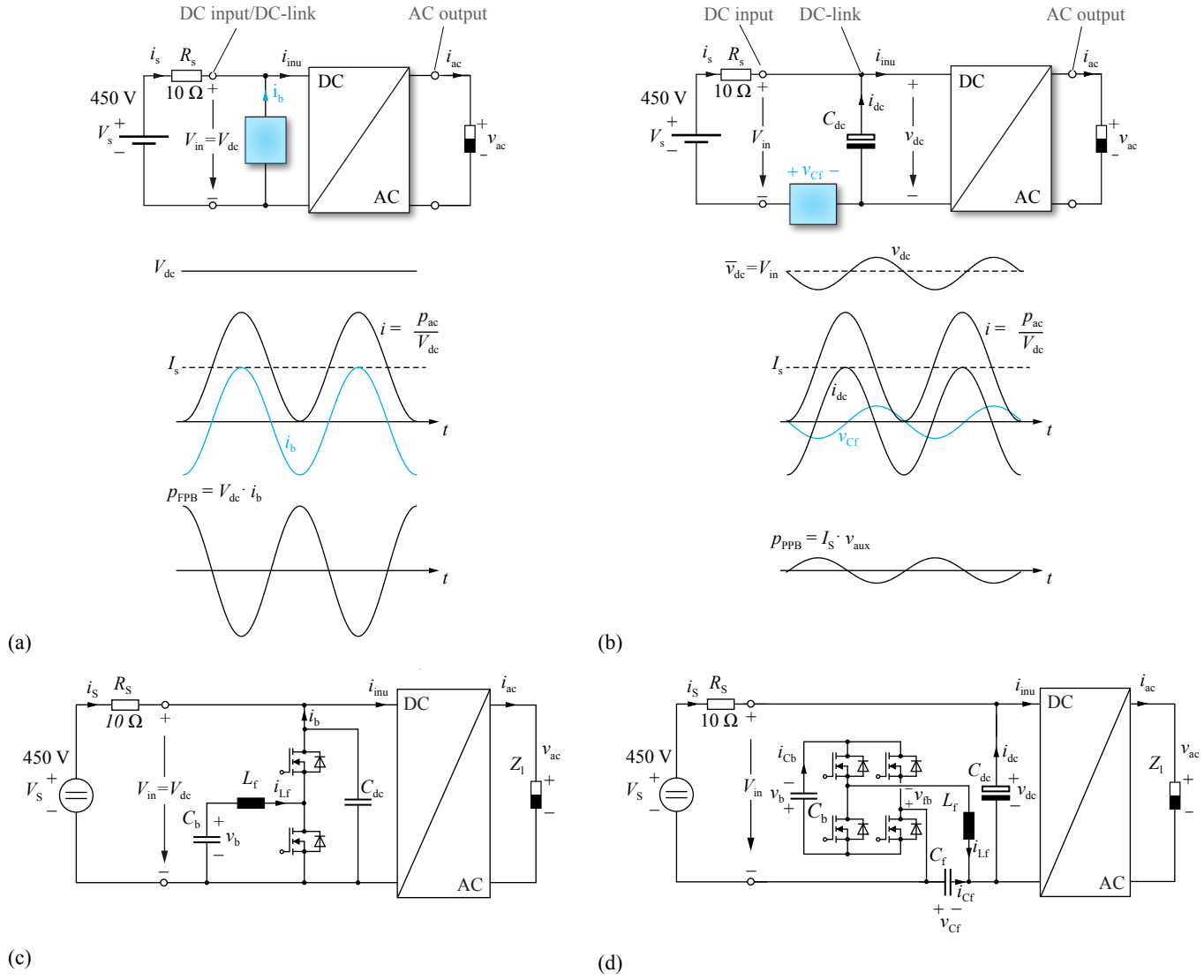

Fig. 1. (a) Full-power processing Parallel Current Injector (PCI) active power buffer concept with characteristic waveforms. (b) Partial-power processing Series Voltage Injector (SVI) buffer concept with characteristic waveforms. (c) Synchronous buck converter implementation of the PCI converter. (d) H-bridge based implementation of the SVI converter. The depicted setup with $V_\text{s} = 450\,\text{V}$ DC source and $R_\text{s} = 10\,\Omega$ input resistor is in accordance with the technical testing requirements of the Google Little Box Challenge (GLBC) [1], [2].

less then what would be actually needed to comply with the $2.5\,\%$ voltage ripple requirement. In order to meet the specified input voltage ripple, an additional Series Voltage Injector (SVI) converter impresses voltage v_{Cf} which compensates the $120\,\mathrm{Hz}$ voltage ripple still present in v_{dc} resulting in a constant input voltage V_{in}. Fig. 1 (d) shows the implementation of the SVI converter based on a H-bridge with LC output filter and flying buffer capacitor C_{b} selected by the team from Schneider Electric.

The key advantage of this concept is that the SVI converter can be implemented with low-voltage (LV) components and only processes a small share of the entire fluctuating power, $\hat{p}_{\mathrm{SVI}} = I_{\mathrm{s}} \cdot \hat{v}_{\mathrm{Cf}} \approx 100\,\mathrm{W}$, since, for a defined DC-link capacitance size of around $400\,\mu\mathrm{F}$ - $600\,\mu\mathrm{F}$, the amplitude of v_{Cf} required to compensate the remaining voltage ripple only amounts to approximately $20\,\mathrm{V}$ and $I_{\mathrm{s}} = 5\,\mathrm{A}$ in the nominal operating point (cf. Tab. I). For the remainder of this work, [SVI\C] denominates the combination of the partial-power SVI converter and the DC-link capacitor which jointly perform the buffering of the $120\,\mathrm{Hz}$ pulsating power.

On the contrary, the PCI buffer concept selected by the winning team processes the entire fluctuating portion of the AC power, $\hat{p}_{\mathrm{PCI}} = V_{\mathrm{dc}} \cdot \hat{i}_{\mathrm{b}} = V_{\mathrm{dc}} \cdot I_{\mathrm{s}} = 2\,\mathrm{kW}$, resulting in a lower overall conversion efficiency particularly at light load of the overall converter system. However, only a (non-electrolytic) single buffer capacitor is required which could result in a more compact design compared to the SVI approach where both a DC-link capacitor and an additional buffer capacitor C_{b} are needed. It should be noted that $C_{\mathrm{dc}} \approx 15\,\mu\mathrm{F}$ shown in Fig. 1 (b) is only intended to filter HF switching noise. Also note that, unlike in case of the [SVI\C] buffer, there is no distinction between the denomination "buffer" and "converter" in case of the full-power PCI approach, i.e. "PCI buffer" and "PCI converter" are synonyms for the remainder of this work.

Although the use of active power buffer concepts in various configurations to cope with the $120\,\mathrm{Hz}$ pulsating power in single-phase system has already been studied in literature in recent years [13]–[23], a direct multi-objective performance comparison of a full-power PCI buffer and a [SVI\C] buffer approach, particularly for the technical requirement of the GLBC (cf. Tab. I), has not been presented so far. For this reason, the main contribution of the work presented in this paper is the comparative evaluation of the PCI and [SVI\C] buffer concepts in terms of achievable efficiency, η, power density, ρ, and input voltage variation compensation performance under both stationary and transient conditions and consequently to assess whether the team from CE+T Power had a significant advantage by choosing the PCI concept for their Google Little Box inverter design.

Due to the numerous degrees of freedom in the design of the buffer converters, e.g. capacitance value and capacitor technology (aluminum electrolytic and ceramic capacitor technology), bridge-leg control (conventional PWM or zero voltage switching Triangular Current Mode [24]), switching frequency, etc., a design optimization is carried out and the $\eta\rho$-Pareto fronts are determined for both considered concepts in order to estimate the maximal achievable performance and allow a fair comparison. In previous work of the authors [6], the Pareto optimization and the hardware implementation of the PCI concept was described in detail. The main findings are summarized and complemented with latest experimental results in Section II-A - Section II-C of this paper. Likewise as presented in [6] for the PCI, a mathematical model of the capacitor voltages is derived in Section III-A for the [SVI\C] buffer and subsequently used in the design optimization outlined in Section III-B. A control system for the SVI converter is proposed in Section III-C and the implemented hardware demonstrator is described in detail in Section III-D including experimental measurements to assess the achieved performance under stationary and transient conditions. The obtained optimization results and the achieved $\eta\rho$-performance of the implemented prototypes of both considered concepts are then discussed and comparatively evaluated in Section IV. Moreover, a comparison between conventional passive buffering with solely electrolytic DC-link capacitors and the investigated optimally designed PCI and [SVI\C] buffer concepts is provided, indicating at which voltage ripple limit it actually becomes beneficial to implement an active power buffer. Furthermore, a short discussion on the implementation cost of the investigated active power buffer concepts will be provided. Section V concludes the paper and summarizes the most important findings.

II. Full-Power Parallel Current Injector (PCI) Power Buffer

A. PCI Converter Pareto Optimization

Despite the reduced capacitance requirement, the buffer capacitor still comprises a large portion of the active buffers' overall volume. Thus, the selected capacitor technology defines to a large extend the resulting power density and plays a critical role in the optimal design of the PCI converter. In principle, the design of the PCI converter is independent of the implemented inverter topology, however the reactive power consumption of the installed EMI filter on the AC-side also has to be considered. The PCI is controlled to fully compensate the fluctuating power resulting from the load and the EMI filter of the inverter stage. As a consequence, only a constant power P_s must be provided by the power supply V_s and v_{dc} is relieved from the twice mains-frequency voltage ripple. Accordingly, the PCI must be dimensioned to cope with the apparent power

$$S_{\mathrm{b}} = \sqrt{P_{\mathrm{ac}}^2 + (Q_{\mathrm{ac}} + Q_{\mathrm{filt}})^2}, \tag{2}$$

wherein Q_{filt} is the reactive power of the main DC/AC converter's EMI filter (not shown in Fig. 1 (c)). The instantaneous power provided by the PCI buffer can be calculated according to

$$p_b = v_b \cdot i_{\mathrm{Lf}} + v_{\mathrm{L,b}} \cdot i_{\mathrm{Lf}} = v_b \cdot i_{\mathrm{Lf}} + L_{\mathrm{f}} \cdot \frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{Lf}} \cdot i_{\mathrm{Lf}} \approx v_b \cdot i_{\mathrm{Lf}} \tag{3}$$

Neglecting the power contribution of the PCI inductor is reasonable, because when a mean buffer capacitor voltage of $V_b = 300\,\mathrm{V}$ and a reasonable inductor value of $20\,\mu\mathrm{H}$ is considered, then the peak power in the inductor only amounts to

$$\hat{p}_{\mathrm{L,f}} = \omega L_{\mathrm{f}} \hat{i}_{\mathrm{L,f}}^2 = \omega L_{\mathrm{f}} \left(\frac{2\,\mathrm{kW}}{300\,\mathrm{V}} \right)^2 = 335\,\mathrm{mW}.$$

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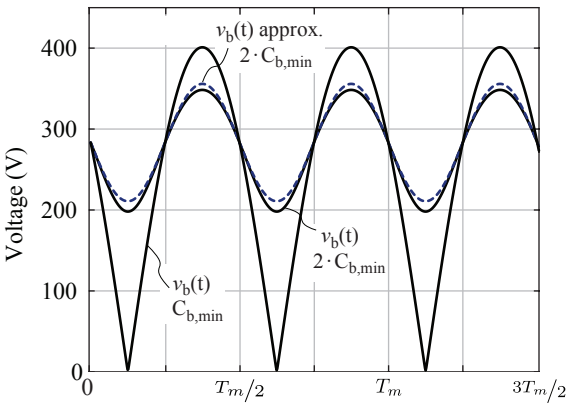

Fig. 2. Full-power Parallel Current Injector (PCI) converter buffer capacitor voltage for different capacitance values.

The fluctuating power is fully compensated if

$$v_b(t) \cdot i_{\mathrm{Lf}}(t) = p_{\mathrm{out,ac}}(t) = S_{\mathrm{b}} \cos(2\omega t - \tilde{\phi}), \tag{4}$$

where $\tilde{\phi} = \arctan\left({}^{(Q_{\mathrm{ac}}+Q_{\mathrm{filt}})}/_{P_{\mathrm{ac}}}\right)$. Inserting the voltage/current relationship of the buffer capacitor yields the differential equation

$$v_b \cdot C_b \frac{\mathrm{d}v_b}{\mathrm{d}t} = S_{\mathrm{b}} \cos(2\omega t - \tilde{\phi}), \tag{5}$$

with the analytical solution

$$v_b(t) = \sqrt{V_{\mathrm{b},0}^2 - \frac{S_{\mathrm{b}} \sin(2\omega t - \tilde{\phi})}{\omega C_b}}, \tag{6}$$

wherein $V_{\mathrm{b},0}$ is the RMS value of $v_{\mathrm{b}}(t)$ and also corresponds to the initial buffer capacitor voltage at $t = \frac{\tilde{\phi}}{2\omega}$ (cf. $t = 0$ in Fig. 2). Now, if the capacitance is chosen much larger than the minimum requirement,

$$C_b >> C_{\mathrm{b,min}} = \frac{2S_b}{\omega V_{\mathrm{dc}}^2} = 66.3\,\mu\mathrm{F}, \tag{7}$$

(6) can be approximated by means of

$$v_b(t) \approx V_{\mathrm{b},0} - \frac{1}{2} \frac{S_b \sin(2\omega t - \tilde{\phi})}{\omega C_b V_{\mathrm{b},0}}, \tag{8}$$

as shown in Fig. 2 for $C_b = 2 \cdot C_{\mathrm{b,min}} \approx 130\,\mu\mathrm{F}$ and $V_{\mathrm{b},0} \approx 280\,\mathrm{V}$.

On the one hand, the large feasible amplitude of the voltage ripple enables the use of thin-film and ceramic capacitors because of the much smaller needed capacitance values compared to conventional passive capacitive DC-link buffering. On the other hand, the large voltage ripple and the DC bias makes the design of the buffer capacitor more challenging especially in case of ceramic capacitor technology with non-linear capacitance-voltage relationship.

Identified as the two most promising ceramic capacitors for large voltage swing buffer applications, a comprehensive performance analysis of TDK's $2.2\,\mu\mathrm{F}/450\,\mathrm{V}$ class II/X6S capacitor [25], [26] and EPCOS/TDK's $2\,\mu\mathrm{F}/500\,\mathrm{V}$ 2nd generation CeraLink [27] was carried out. In particular, as depicted in Fig. 3, the capacitance ($\frac{\mu\mathrm{F}}{\mathrm{cm}^3}$) and loss density ($\frac{\mathrm{W}}{\mathrm{cm}^3}$) at 60 °C

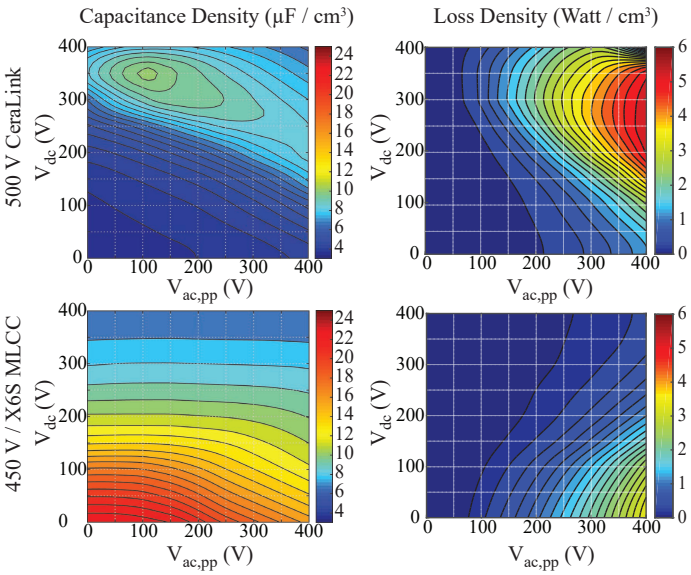

Fig. 3. Contour plot of capacitance density and loss density of a 500 V CeraLink and 450 V class II/X6S capacitor technology with respect to DC bias V_{dc} and 120 Hz AC excitation $V_{\mathrm{ac,pp}}$ at 60 °C operating temperature.

TABLE II
SYSTEM PARAMETERS & SEARCH LOCUS OF THE PCI CONVERTER PARETO OPTIMIZATION

Feature	**Range/Option**
Capacitor Technology	450 V class II/X6S 500 V 2nd generation CeraLink
C_b	[110 µF, 350 µF]
$V_{\mathrm{b},0}$	$^1/_2 C_b \cdot V_{\mathrm{b},0}^2 \in [E_{0,\mathrm{min}}, E_{0,\mathrm{max}}]$
E_{m}	5 % - 30 %
Inductor Technology	N87 MnZn ferrite, HF litz wire
L_f	[10 µH, 60 µH]
Modulation	TCM, f_s from 200 kHz to 1 MHz PWM, $f_s = 140$ kHz
Heat sink	CSPI $= 25.7\,\frac{\mathrm{W}}{\mathrm{K\,dm}^3}$

operating temperature as a function of applied DC bias and large-signal 120 Hz AC ripple was experimentally measured. In a characteristic PCI buffer operating point, i.e. a buffer capacitor voltage with 300 V DC bias and a $130\,\mathrm{V_{pp}}$ superimposed AC voltage, the X6S MLCC features a capacitance density of $8.4\,\frac{\mu\mathrm{F}}{\mathrm{cm}^3}$, as opposed to the slightly higher $9.5\,\frac{\mu\mathrm{F}}{\mathrm{cm}^3}$ of the CeraLink. However, the loss density of the X6S MLCC amounts to just $56\,\frac{\mathrm{mW}}{\mathrm{cm}^3}$. By contrast, the CeraLink dissipates roughly $1\,\frac{\mathrm{W}}{\mathrm{cm}^3}$ in the very same operating point.

According to (8) and a particular value of C_b and $V_{b,0}$ from the considered design space listed in Tab. II, the operating point of the buffer capacitor can be calculated. Given this operating point and a ceramic material from the design space, the prevailing large-signal capacitance density is extracted from the empirical dataset (cf. Fig. 3). This allows to accurately calculate the number of single capacitor chips mounted in parallel to meet the requested large-signal capacitance value C_b, despite the non-linear behavior of the considered ceramic materials. Likewise, the power losses occurring in

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the capacitor assembly caused by continuously storing and releasing

$$\Delta E = \frac{S_b}{\omega} = 5.31\,\mathrm{J} \tag{9}$$

is extracted from the experimental measurements (cf. Fig. 3). Additional losses due to the high frequency current ripple in i_{Lf} is negligible, since the ESR of the buffer capacitor assembly is vanishingly low at the considered switching frequencies. Moreover, $V_{b,0}$, the RMS value of the buffer capacitor voltage or the mean buffer voltage according to (8), can be adjusted by the employed control system as proposed in Section II-B and is considered a further degree of freedom in the design. Depending on the large-signal ripple and bias properties of the respective capacitor technology, different bias voltages might lead to the optimal design. However, in order to have enough energy margin to cope with load transients, the bias voltage must be kept within certain bounds. Specifically, given C_b then $V_{\mathrm{b},0}$ must be chosen such that

$$1/2 C_b \cdot V_{\mathrm{b},0}^2 \in [E_{0,\min}, E_{0,\max}]\,, \tag{10}$$

where the interval boundaries of the mean energy E_0 are given by

$$E_{0,\min} = E_m + \frac{\Delta E}{2}, \quad E_{0,\max} = E_{\max} - E_m - \frac{\Delta E}{2},$$

with the maximal energy

$$E_{\max} = 1/2 C_b V_{\mathrm{dc}}^2$$

and an empirically chosen energy margin in the range of

$$E_m = (5\,\% - 30\,\%\text{ of }\Delta E).$$

Besides the buffer capacitor, a compact implementation of the PCI half-bridge and the HF filter inductor is also vital. In [28], [29] GaN was identified as the key power semiconductor technology for the implementation of ultra-compact converter designs for the Google Little Box Challenge. For the implementation of the half-bridge, $600\,\mathrm{V}$ / $70\,\mathrm{m\Omega}$ CoolGaN devices form Infineon in combination with a novel high-performance gate drive circuit [28] are considered. The bridge-leg is operated with a Triangular Current Mode (TCM) modulation scheme [24], where the on/off intervals of the power transistors are adjusted such that a triangular current is impressed in the bridge-leg filter inductor and Zero Voltage Switching (ZVS) is achieved in all operating points. Due to reduced switching losses and accordingly reduced heat sink volume, a higher efficiency and higher power density is expected when TCM is applied. Moreover, a rather high switching frequency in the range of 200kHz-1MHz results in a significantly reduced volume of the inductor. However, as outlined in [28], the required large HF current ripple leads to increased conduction losses which reduces the gain of soft-switching resulting from TCM. Therefore also conventional PWM is considered for the bridge-leg, since the large turn-on switching losses associated with PWM can be reduced when a relatively high current ripple is allowed (ZVS around the current zero crossings). In [30], advanced models for winding and core loss calculation and thermal models for HF inductor design are presented. Adopting these models to a large variety of available core geometries, N87 MnZn ferrite material and available HF-litz wires, an optimal inductor in terms of volume can be identified for a given inductance value and current waveform. The generated power losses are extracted by means of an optimized forced-air cooled heat sink with a experimentally verified Cooling System Performance Index (CSPI) of $25.7\,\frac{\mathrm{W\,dm^3}}{\mathrm{K}}$ as described in more detail in [29].

Given the design space as summarized in Tab. II and elaborate loss and volume models of the utilized components, the performance of several PCI converter configurations was calculated. Fig. II-A (a) displays the performance of the calculated designs in the $\eta\rho$-performance space. In particular, PCI converter designs with class II and CeraLink capacitors, both either with TCM or conventional PWM operation, are distinguished by color. As reference, the $\eta\rho$-performance of a conventional DC-link assembly, which will be introduced later in Section IV, is also shown. Clearly noticeable, designs with class II/X6S ceramic outperform those with CeraLink capacitors. The highest power density of $41.3\,\frac{\mathrm{kW}}{\mathrm{dm^3}}$ ($677.1\,\mathrm{W/in^3}$) and an efficiency of $99.4\,\%$ (P2) is achieved with TCM modulation, $C_b = 110\,\mu\mathrm{F}$ with class II/X6S capacitors, and $L_{\mathrm{f}} = 30\,\mu\mathrm{H}$. As discussed previously, the CeraLink capacitors exhibits much higher $120\,\mathrm{Hz}$ losses compared to the class II/X6S capacitors which explains the drop in efficiency of the PCI converter designs with CeraLink capacitors as shown in Fig. II-A (a), and the reduction in power density due to the higher cooling effort. As a consequence, power density optimal designs with class II/X6S (P2), (P3) feature a low total buffer capacitance around $110\,\mu\mathrm{F}$, accordingly a large $120\,\mathrm{Hz}$ voltage ripple with $\approx 180\,\mathrm{V_{pp}}$ amplitude, and a mean voltage $V_{\mathrm{b},0}$ of $300\,\mathrm{V}$. On the other hand, optimal designs employing the CeraLink capacitor, feature comparably high total capacitance values of $\approx 200\,\mu\mathrm{F}$ and a consequently low voltage ripple with $\approx 80\,\mathrm{V_{pp}}$ amplitude in order to to keep the losses small. Moreover, since the capacitance density of the CeraLink capacitors increases with applied bias, optimal results (P4), (P5) exhibit increased bias voltages $V_{\mathrm{b},0} \approx 330\,\mathrm{V} - 340\,\mathrm{V}$. In order to show the impact of the bias voltage on the overall performance of the CeraLink PCI buffer and better reflect the performance of the actually realized prototype (cf. Section II-C1), the optimization results for a fixed bias voltage of $V_{\mathrm{b},0} = 300\,\mathrm{V}$, which corresponds to a more conservative energy margin of $E_{\mathrm{m}} = 30\,\%$, are also included in Fig. II-A.

Also noticeable in the $\eta\rho$-space, designs using TCM modulation feature higher efficiency compared to PWM operation with $f_s = 140\,\mathrm{kHz}$. Naturally, designs (P2)-(P5) with maximum power density tend towards the lowest energy margins as specified in the design space (cf. Tab. II).

The volume of the PCI converter is clearly dominated by the buffer capacitor as shown in Fig. II-A (b). Also the volume required for cooling is significant, especially in the case of design (P6). As stated earlier, optimal designs using CeraLink feature a higher total buffer capacitance, consequently occupying more volume. The loss distribution of the optimal designs is given in Fig. II-A (c), revealing the almost negligible losses occurring in the class II/X6S designs (P2), (P3), and the almost 7 times higher losses in the CeraLink

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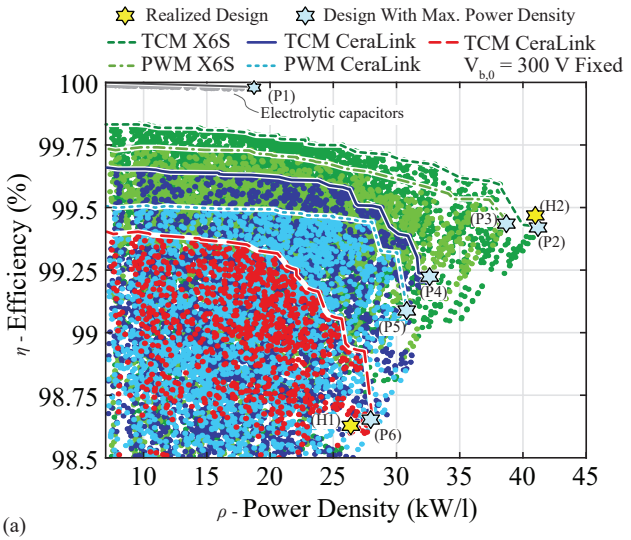
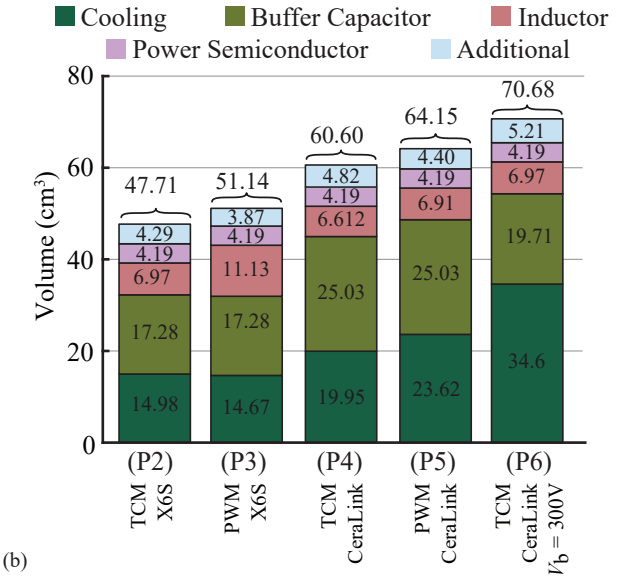


(a)



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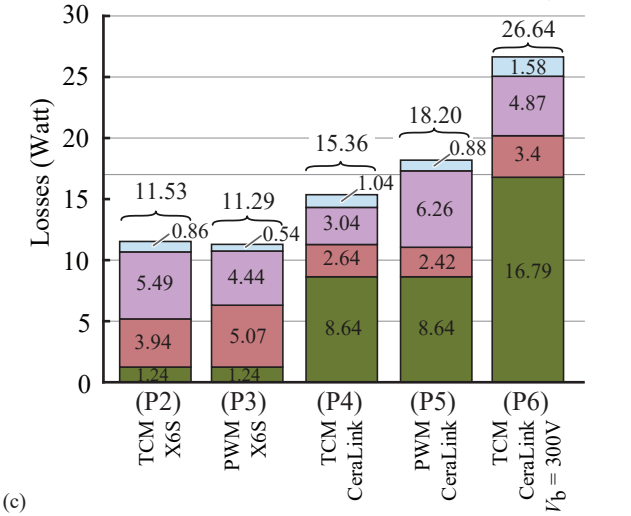

(c)

Results of the PCI converter design optimization. (a) $\eta\rho$-plot of the calculated designs with indicated Pareto fronts. (b) Volume distribution of the optimal designs (P2)-(P6) (c) Loss distribution of the optimal designs (P2)-(P6).

designs (P4), (P5). Surprising are the dominating losses in the CeraLink capacitor of the pragmatic design (P6), which drastically reduces efficiency and substantially increases the heat sink volume. Clearly, the buffer capacitor operating point occurring at steady-state in design (P6) is not optimal given the characteristics of the CeraLink. The category *Additional* shown in Fig. II-A (b) & (c) includes the volume and loss data of the current zero-crossing detector (required for TCM operation), analog measurement circuits, metal enclosure of the PCI converter, and the power consumption of the heat sink fans, respectively. Given the gained insights from the $\eta\rho$-space of the calculated designs, it is clearly advisable to realize a PCI converter using class II/X6S capacitors. However, practical manufacturing considerations have to be included in the decision making. In order to realize $110\,\mu\text{F}$ roughly 150 single class II/X6S chips must be mounted in parallel. With the known issue of ceramic cracking due to mechanical and thermal stress, this certainly requires advanced packaging techniques in order to achieve a reliable assembly. On the other hand, the CeraLink capacitor is available in a package with 20 chips mounted in parallel by means of a silver sintered connection onto a common lead-frame which is able to absorb mechanical stress. Two different PCI converter designs were selected from the presented Pareto optimization results for hardware implementation: (i) Due to the easier and more reliable assembly of the buffer capacitor, it was decided to realize the $28\,\frac{\text{kW}}{\text{dm}^3}$ ($458.8\,\text{W/in}^3$) design (P6) in hardware, with $C_b = 150\,\mu\text{F}$ comprised of individual $2\,\mu\text{F}$ CeraLink capacitors despite the higher losses, the conservative energy margin of $E_\text{m} = 30\,\%$ ($V_{\text{b},0} = 300\,\text{V}$) and TCM modulation of the bridge-leg. (ii) Aiming at maximum power density, the $38.4\,\frac{\text{kW}}{\text{dm}^3}$ ($629.3\,\text{W/in}^3$) design (P3) with $C_b = 110\,\mu\text{F}$ comprised of individual $2.2\,\mu\text{F}/450\,\text{V}$ class II/X6S, a bias voltage $V_{\text{b},0} = 280\,\text{V}$ and $140\,\text{kHz}$ PWM operation of the bridge-leg, was also selected for hardware implementation despite the more challenging buffer capacitor assembly. The actually achieved $26.12\,\frac{\text{kW}}{\text{dm}^3}$ ($428\,\text{W/in}^3$) power density and $98.65\,\%$ efficiency of the implemented CeraLink-TCM prototype, is indicated with label (H1) in Fig. II-A (a). Likewise, the implemented class II/X6S-PWM prototype with an achieved $\eta\rho$-performance of $99.4\,\%$ and $41.3\,\frac{\text{kW}}{\text{dm}^3}$ ($676.8\,\text{W/in}^3$) as indicated with label (H2). Both implemented PCI converter prototypes will be described in detail in Section II-C.

B. Control System of the PCI converter

One of the downsides of using an active approach to cope with the $120\,\text{Hz}$ power pulsation, is the required control system which increases the overall complexity of the DC/AC converter. The cascaded control system for the PCI converter proposed in [6] is depicted in Fig. 4 and contains dedicated subsystems with the objective to (a) control the mean/bias voltage of the buffer capacitor, (b) achieve a tight control of the DC-link voltage during load transients, (c) compensate the fluctuating AC power by proper current injection, and (d) combine all control objectives into a single reference value for the underlying inductor current control. In order to completely eliminate the DC-link voltage ripple, feed-forward control of

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the fluctuating portion of the AC power and an additional resonant controller [31] tuned at even multiples of the AC frequency are employed as shown in Fig. 4 (c). If only control aspects are considered, then the reference of the mean PCI converter capacitor voltage V_b^* is set to a voltage level

$$V_{b,\mathrm{mid}} = {}^{V_{dc}}/_{\sqrt{2}} = 282.8\,\mathrm{V} \tag{11}$$

corresponding to half of the maximal stored energy. Maintaining the bias of the buffer capacitor at $V_{b,\mathrm{mid}}$ results in symmetrical energy margins, and load step-up and step-down can be handled equally well. However, as outlined in Section II-A, the DC bias of the buffer capacitor strongly affects the $\eta\rho$-performance results since (i) the prevailing capacitance density of the considered ceramic capacitors is strongly dependent on the DC bias and (ii) the amplitude of current i_{Lf} is inversely proportional to v_b. Therefore, a compromise between transient handling capability and $\eta\rho$-performance must be made. In case of the realized Ceralink-TCM and class II/X6S-PWM PCI converter prototypes presented in Section II-C of this paper, the reference voltage V_b^* is set to 300 V and 280 V, respectively. The inner loop of the cascaded control structure (cf. Fig. 4 (b)) is required to tightly regulate the average DC-link voltage under all load conditions. Due to the cascaded structure, controlling the DC-link voltage has always priority over the mean buffer capacitor voltage. This has significant advantages in case of abrupt load changes, since the average buffer capacitor voltage V_{b} can be temporarily deflected from the reference V_b^*, keeping v_{dc} tightly controlled. As can be seen, the individual current reference values computed by the control subsystems (a)-(c) are then combined in a single current reference i_{Lf}^* and forwarded to the inner PWM current control loop (cf. control subsystem (d)). If TCM modulation is employed (not shown in Fig. 4), the turn-on and turn-off times of the power transistors are computed such that, on average over one switching cycle, the current in the inductor meets i_{Lf}^* and ZVS of the bridge-leg applies. The interested reader is referred to [6] for more details.

C. Hardware Implementation and Experimental Verification

1) Version 1 - CeraLink and TCM Modulation: The first implemented prototype (Version 1) of the PCI converter concept is shown in Fig. 5 (a). As mentioned before, the half-bridge is implemented with 600 V/70 mΩ CoolGaN devices. In order to reduce reverse conduction losses of the GaN transistors during the dead-times, 600 V SiC Schottky diodes from Wolfspeed are mounted in parallel to the power transistors. The bridge-leg is operated with a TCM modulation scheme with variable switching frequency in the range of 200 kHz - 1000 kHz that enables ZVS transitions in all operating points. The inductor $L_{\mathrm{f}} \approx 21\,\mu\mathrm{H}$ of the power buffer was realized by a series connection of two 10.5 µH inductors implemented based on a novel multiple-gap multiple parallel foil winding design using the DMR51 low-loss HF MnZn Ferrite core material from DMEGC. The buffer capacitor, C_{b}, with a large-signal equivalent capacitance of 150 µF, is implemented by means of 108 individual 2 µF/500 V CeraLink capacitors. By the courtesy of EPCOS/TDK, a custom package with 18 capacitor chips mounted together on silver coated copper lead frames was available. The design parameters and selected features of the realized system are summarized in Tab. III.

Combined with a 2 kW high power density inverter stage designed for the Google Little Box Challenge (cf. Fig. 5 (a)), the constructed PCI converter was experimentally tested. As can be seen from the picture, the power buffer was designed as a stand-alone module which allowed to directly substitute the electrolytic capacitor bank of a preliminary version of

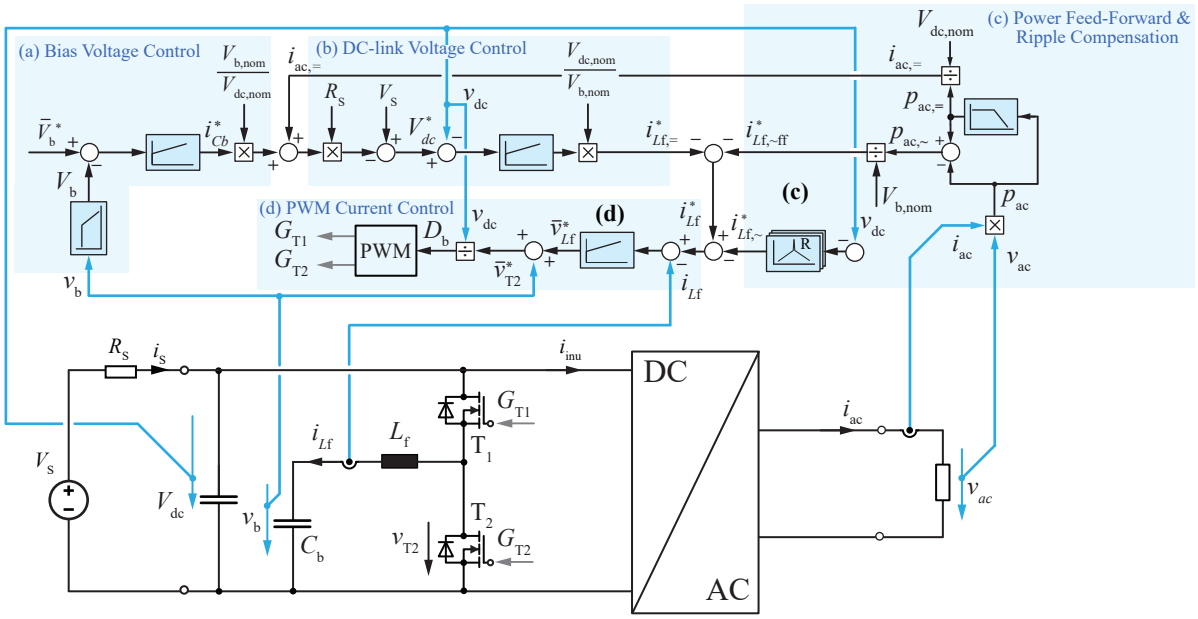

Fig. 4. Proposed cascaded control structure of the PCI converter. (a) Control of the average buffer capacitor voltage. (b) Control of the DC-link voltage. (c) Compensation of the pulsating power by means of feed-forward control and resonant compensators. (d) Inner loop PWM current control of the inductor current.

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TABLE III
TECHNICAL DETAILS OF THE CERALINK-TCM PCI CONVERTER.

Feature	Value	Description
Volume (no cooling)	$47.3\,\mathrm{cm}^3$ $(2.9\,\mathrm{in}^3)$	Boxed volume of the constructed PCI converter without cooler
Volume (with cooling)	$76.6\,\mathrm{cm}^3$ $(4.7\,\mathrm{in}^3)$	Total boxed volume of the PCI converter with a CSPI $= 25.7\,\frac{\mathrm{W}}{\mathrm{K\,dm}^3}$ heat sink
Capacitor volume	$24.6\,\mathrm{cm}^3$ $(1.5\,\mathrm{in}^3)$	Total volume of the installed buffer capacitor
η	$98.65\,\%$	Efficiency at $2\,\mathrm{kW}$
L_f	$21\,\mu\mathrm{H}$	Foil winding and custom shape, multi-gap MnZn ferrite core with 2 times $10.5\,\mu\mathrm{H}$ in series
C_b	$150\,\mu\mathrm{F}$	Equivalent large signal capacitance of the installed CeraLink capacitors

TABLE IV
TECHNICAL DETAILS OF THE CLASS II/X6S-PWM PCI CONVERTER.

Feature	Value	Description
Volume (no cooling)	$34.0\,\mathrm{cm}^3$ $(2.1\,\mathrm{in}^3)$	Boxed volume of the constructed PCI converter without cooler
Volume (with cooling)	$48.4\,\mathrm{cm}^3$ $(3.0\,\mathrm{in}^3)$	Total boxed volume of the PCI converter with a CSPI $= 37.5\,\frac{\mathrm{W}}{\mathrm{K\,dm}^3}$ heat sink
Capacitor volume	$19.9\,\mathrm{cm}^3$ $(1.5\,\mathrm{in}^3)$	Total volume of installed buffer capacitor
η	$99.4\,\%$	Efficiency at $2\,\mathrm{kW}$
L_f	$40\,\mu\mathrm{H}$	HF litz wire and RM 10 MnZn ferrite core (N87)
C_b	$120\,\mu\mathrm{F}$	Equivalent large signal capacitance of the installed $200 \times 2.2\,\mu\mathrm{F}/450\,\mathrm{V}$ MLCC

the initial Google Little Box converter developed at ETH Zurich. In order to extract the power losses, an optimized forced-air cooled dual-sided heat sink with an effective CSPI of $25.7\,\frac{\mathrm{W}}{\mathrm{dm}^3\,\mathrm{K}}$ is utilized. The heat sink has a height of only $4.5\,\mathrm{mm}$ and employs 6 Sunon $5\,\mathrm{V}$ DC micro blowers $(30 \times 30 \times 3\,\mathrm{mm})$ per element (UB5U3-700). It should be noted that in Fig. 5 (a) the top-side heat sink is removed. The novel control system presented in Section II-B is implemented on a *TMS320F28335* from Texas Instrument's C2000 32-bit family of microcontrollers. As mentioned previously in Section II-B, the PWM current control highlighted in Fig. 4 is substituted with a cycle-by-cycle TCM control, whereby the turn-on and turn-off intervals of the power transistors are computed on the microcontroller and then forwarded to a modulator implemented on a Lattice XP2 FPGA.

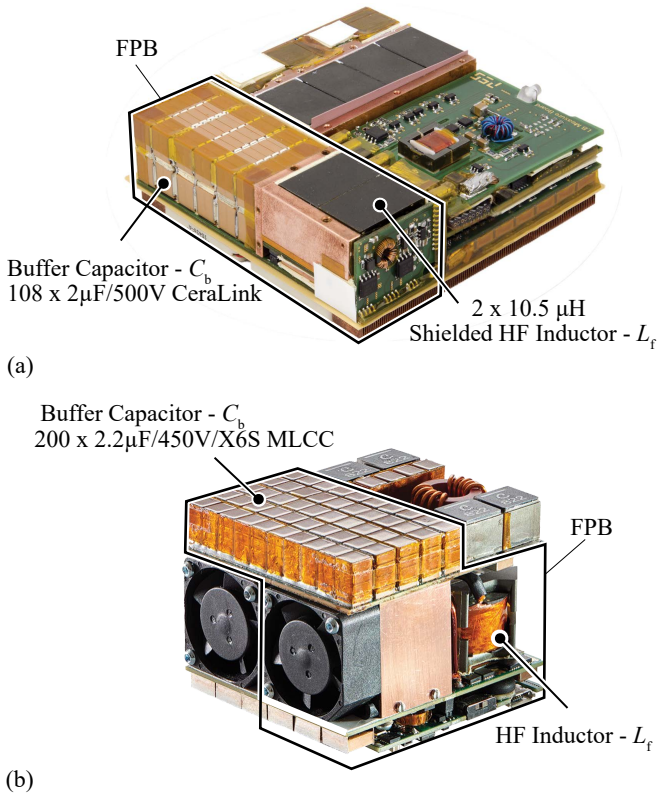

Fig. 5. (a) Picture of the Google Little Box 1.0 (1st version of the Little Box inverter developed at ETH Zurich) with PCI converter using CeraLink capacitors and TCM control of the bridge-leg. (b) Picture of the Google Little Box 2.0 (2nd further optimized version of the Little Box inverter) with PCI converter using class II/X6S MLCC and constant $140\,\mathrm{kHz}$ PWM.

2) Version 2 - Class II/X6S and PWM: Benefiting from the gained insights of the design optimization in Section II-A carried out in the aftermath of the GLBC, a second prototype of the PCI converter (Version 2) was implemented and the design parameters and selected features of the realized system are summarized in Tab. IV. For the sake of maximum power density, the implemented power pulsation buffer is, unlike before, not designed as stand-alone module but instead incorporated in the inverter stage as can be seen from the picture in Fig. 5 (b) of the 2nd version of the Google Little Box inverter developed at ETH Zurich. The bridge-leg of the PCI converter Version 2 prototype is implemented with the same $600\,\mathrm{V}/70\,\mathrm{m\Omega}$ CoolGaN technology, but uses two parallel connected transistors per switch and is operated with an EMI friendly constant $140\,\mathrm{kHz}$ PWM instead of TCM modulation. The inductor of the active power buffer, $L_\mathrm{f} = 40\,\mu\mathrm{H}$, is implemented on a RM 10 core using the MnZn ferrite material N87 from TDK. The winding is realized with 20 turns of a $225 \times 71\,\mu\mathrm{m}$ HF litz wire without additional silk insulation.

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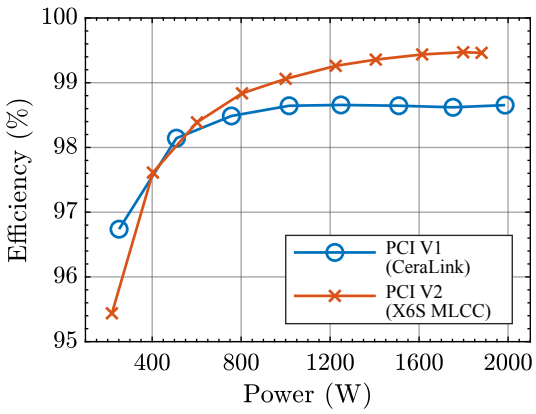

Fig. 6. Measured efficiency of the constructed PCI converter prototypes as a function of the peak value of the processed apparent power S_b.

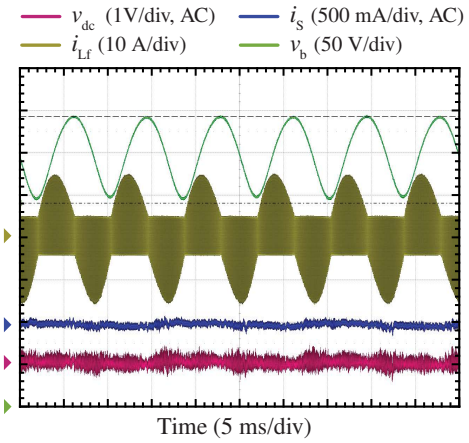

Fig. 7. Steady-state performance of the realized PCI converter at 2 kW rated power. The timebase of the measurement is 5 ms/div. Probes for measuring the converter input current and the DC-link voltage are AC coupled in order to highlight the excellent ripple cancellation.

The limbs of the RM 10 core were shortened with a diamond wheel precision saw to achieve a total air gap length of 2 mm (1 mm per limb) while keeping the total height of the core unchanged. The buffer capacitor, C_b, features an effective large-signal equivalent capacitance of $\approx$ 120 µF, and was realized by means of 200 individual 2.2 µF/450 V class II/X6S MLCC. As can be seen from Fig. 5 (c), 200 of these chip capacitors were soldered together on a PCB which is on the one hand a very challenging assembly task and on the other hand bears the risk of electrical failures due to micro-cracks in the ceramic material caused by mechanical stress during assembly and/or operation.

The novel control system presented in Section II-B is entirely implemented on the *TMS320F28335* microcontroller. Because conventional PWM current control is employed (cf. Fig. 4), no additional FPGA is needed which simplifies soft- and hardware development of the digital control system.

3) PCI converter $\eta\rho$-performance: The conversion efficiency of the active power buffer is defined according to

$$\eta = 1 - \frac{P_v}{S_b} \tag{12}$$

where P_v denominates the losses of the PCI buffer when processing the apparent power S_b of the main inverter with ohmic load (cf. (2)). The efficiency measured with a Yokogawa WT3000 precision power analyzer of the CeraLink-TCM prototype at 2 kW rated power is 98.65 % as depicted in Fig. 6 which corresponds to 27 W of losses. The total volume of the realized PCI converter including cooling volume amounts to 76.6 cm^3 which corresponds to a power density of 26.1 $\frac{kW}{dm^3}$ (428 W/in^3).

The measured efficiency of the class II/X6S-PWM prototype, as also depicted in Fig. 6, is around 99.4 % at close to 2 kW which corresponds to only about 12 W of losses at rated power. The total volume of the realized PCI converter Version 2 including cooling volume amounts to 48.4 cm^3 which corresponds to a power density of 41.3 $\frac{kW}{dm^3}$ (677 W/in^3).

As described in Section II-A, the main reason for the significantly higher efficiency of the second implemented version of the PCI converter, is that compared to the CeraLink capacitor technology, the class II/X6S MLCC exhibit a much lower power loss ($\approx$ 1.5 W instead of $\approx$ 17.3 W at 2 kW) when cycled at low frequency (120 Hz) with a large amplitude voltage swing.

4) Experimental Waveforms: Since both versions of the PCI converter are using the same control systems and exhibit very similar stationary and transient behavior, for the sake of brevity, only the experimental waveforms of the CeraLink-TCM prototype are presented in the following.

The steady-state performance at 2 kW rated power of the implemented PCI converter controller is illustrated in Fig. 7. It can be seen from the recorded DC-link voltage and the converter input current (cf. i_s in Fig. 1 (c)), that the power pulsation was successfully shifted from the DC-link to the buffer capacitor which features a distinctive 100 V_{pp}, 120 Hz voltage ripple. The inductor current waveform is a result of the employed TCM modulation, clearly showing the envelope of the double-line frequency charging currents. In order to verify the dynamic performance of the implemented control system, the inverter was subject to load variations. The transient performance of the PCI converter subject to a load step from 0 W to 700 W is depicted in Fig. 8 (a). Triggered by the load step, the average buffer capacitor voltage drops 50 V below the 300 V at steady-state. Simultaneously, the control system of the PCI converter starts to compensate the power pulsation by means of injecting an appropriate current i_b in the DC-link. As a consequence, a distinct 120 Hz voltage ripple develops at the buffer capacitor immediately after the load step. After a transient time of 60 ms, the average buffer capacitor voltage has recovered and the intrinsic single-phase power pulsation is completely compensated by the PCI converter. During the transient, a small ripple is visible in the DC-link voltage. Take note that because of the $R_s = 10\,\Omega$ input resistor (cf. Fig. 1 (c)), the average DC-link voltage decreases with increasing power and therefore settles at a lower value after the transient. The reactive power drawn by the EMI filter of the inverter stage is also compensated by the PCI converter, thus a small ripple is present in the buffer capacitor voltage

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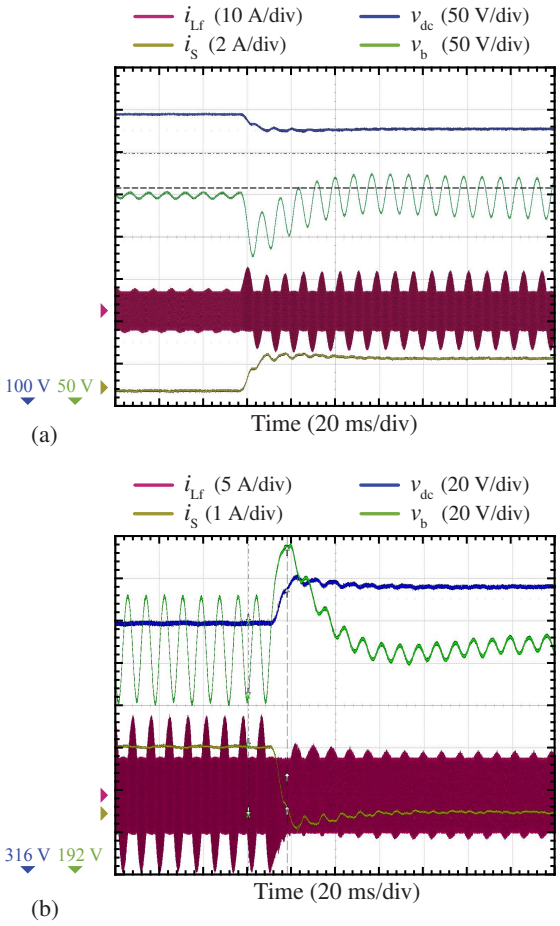

Fig. 8. PCI converter transient response to (a) an abrupt load step from 0 W to 700 W and (b) an abrupt load drop from 700 W to 0 W. The timebase of the measurement is 20 ms/div.

prior to the load step although no load is connected to the inverter. Analogously, a step down from 700 W to 0 W is depicted in Fig. 8 (b). Prior to the load step, the converter system was operating in steady-state exhibiting a 50 V peak-to-peak voltage ripple in the buffer capacitor. Triggered by the load drop, the average buffer capacitor voltage temporarily increases up to 350 V and settles after approximately 60 ms to the reference value. The DC-link voltage remains tightly controlled during the entire transient, showing virtually no overshoot but a small voltage ripple of $\approx$ 5 V during the transient.

This surpasses the required performance specified in the GLBC technical requirements [1], where load steps of maximal 500 W had to be handled within 1 s. Due to the 10 Ω resistor of the application, the DC-link voltage settles at a higher value after the transient.

III. [SVI\C] Power Buffer

A. Mathematical Model of the [SVI\C] Buffer

For the setup of the [SVI\C] buffer as depicted in Fig. 1 (d), the DC-link capacitor voltage is, likewise to (6), given by

$$v_{\mathrm{dc}}(t) = \sqrt{V_{\mathrm{dc},0}^2 - \frac{S_{\mathrm{b}} \sin(2\omega t - \tilde{\phi})}{\omega C_{\mathrm{dc}}}}, \tag{13}$$

wherein $V_{\mathrm{dc},0}$ is the RMS value of $v_{\mathrm{dc}}(t)$ and also corresponds to the initial voltage at $t = \frac{\tilde{\phi}}{2\omega}$. Moreover, referring to Fig. 1 (b), it must hold that

$$\overline{v}_{\mathrm{dc}} = \frac{1}{T}\int_0^T v_{\mathrm{dc}}(t)\mathrm{d}t \stackrel{!}{=} V_{\mathrm{S}} - I_{\mathrm{S}} \cdot R_{\mathrm{S}}. \tag{14}$$

Because the voltage ripple of the DC-link capacitor is compensated by means of the SVI converter, a much wider voltage swing across the DC-link is feasible. The actual size of the DC-link capacitor is limited by the voltage requirement of the inverter to generate v_{ac} at the output. For this reason, $v_{\mathrm{dc}}(t) > v_{\mathrm{ac}}(t)$ has to be ensured at all times which requires a minimum capacitance of

$$C_{\mathrm{dc,min}} \geq \max_t \frac{S_b \sin(2\omega t - \tilde{\phi})}{\omega\left(V_{\mathrm{dc},0}^2 - (\hat{V}_{\mathrm{ac}}\cos(\omega t))^2\right)}. \tag{15}$$

For $\tilde{\phi} = 0$, (15) can be expressed analytically in a compact form,

$$C_{\mathrm{dc,min}} \geq \frac{S_b}{\omega V_{\mathrm{dc},0}\sqrt{V_{\mathrm{dc},0}^2 - \hat{V}_{\mathrm{ac}}^2}}. \tag{16}$$

The operation of the system with minimal DC-link capacitance, which amounts to $C_{\mathrm{dc,min}} \approx 62.66\,\mu\mathrm{F}$ for the given system parameters, is shown in Fig. 9 (a). From a practical point of view it is not reasonable to design the power buffer with $C_{\mathrm{dc,min}}$ since there is no voltage margin and the large resulting voltage ripple of ± 100 V requires the SVI converter to generate high voltages and process power levels of up to 500 W at rated output power. Following a more conservative approach,

$$\min_t v_{\mathrm{dc}}(t) \geq \frac{\hat{V}_{\mathrm{ac}}}{m_{\mathrm{inu,max}}}, \tag{17}$$

the minimum DC-link capacitance is given by

$$\begin{aligned}\widetilde{C}_{\mathrm{dc,min}} &= \frac{S_{\mathrm{b}}}{\omega(V_{\mathrm{dc},0}^2 - (\hat{V}_{\mathrm{ac}}/m_{\mathrm{inu,max}})^2)} \\ &= 298.4\,\mu\mathrm{F}\ (\approx 5 \cdot C_{\mathrm{dc,min}}),\end{aligned} \tag{18}$$

whereby $|m_{\mathrm{inu}}| \leq m_{\mathrm{inu,max}} = 0.9$ is the maximum allowed modulation index of the inverter. Note, that (17) is more demanding compared to the condition

$$\min_t v_{\mathrm{dc}}(t) \geq \frac{v_{\mathrm{ac}}(t)}{m_{\mathrm{inu,max}}}. \tag{19}$$

As can be seen from Fig. 9 (a), the peak value of the varying voltage only amounts to $\approx \pm 20$ V and consequently the SVI converter only processes up to 100 W at rated output power of the inverter and thus can be implemented with low voltage (100 V) components. Likewise to (8), selecting a more conservative DC-link capacitor size ($C_{\mathrm{dc}} > 5 \cdot C_{\mathrm{dc,min}}$) allows to approximate the square root function in the analytical expression of the DC-link voltage,

$$v_{\mathrm{dc}}(t) \approx V_{\mathrm{dc},0} - \frac{1}{2}\frac{S_b \sin(2\omega t - \tilde{\phi})}{\omega C_{\mathrm{dc}} V_{\mathrm{dc},0}}. \tag{20}$$

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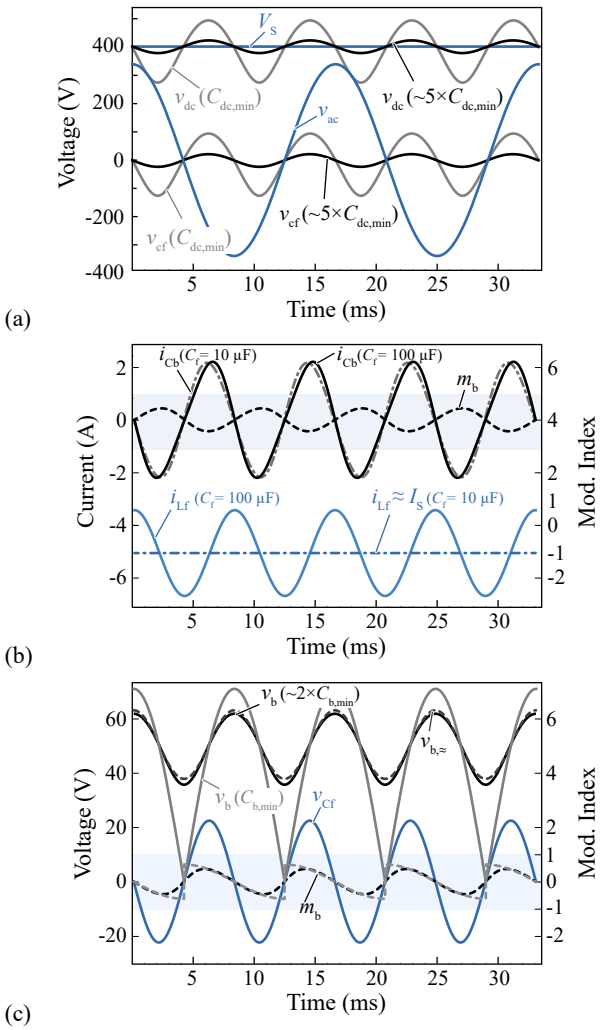

Fig. 9. Simulated waveforms of the derived mathematical model of the [SVI\C] buffer for different component values. (a) Operation with theoretical minimal installed DC-link capacitance $C_{\mathrm{dc,min}}$ and more practical relevant dimensioning with $\tilde{C}_{\mathrm{dc,min}} = 5C_{\mathrm{dc,min}}$. (b) Impact of the size of the switching ripple filter capacitor C_{f} on average buffer capacitor current i_{Cb}. The averaging introduced by the duty cycle variation of the SVI results in a similar average buffer capacitor current i_{Cb}, regardless of whether the filter inductor current i_{Lf} is approximately constant or features are pronounced superimposed twice mains-frequency harmonic component. (c) Operation with theoretical minimal installed buffer capacitance $C_{\mathrm{b,min}}$ and more practical relevant dimensioning with $\tilde{C}_{\mathrm{b,min}} \approx 1.4C_{\mathrm{b,min}}$.

In order to compensate the remaining DC-link voltage ripple and meet the technical specifications, the required voltage across the filter capacitor C_{f} is given by

$$v_{\mathrm{Cf}}(t) = -\frac{1}{2}\frac{S_b \sin(2\omega t - \tilde{\phi})}{\omega C_{\mathrm{dc}} V_{\mathrm{dc},0}}. \tag{21}$$

The current in the filter inductor L_{f} averaged over the switching cycle can then be expressed by

$$i_{\mathrm{Lf}}(t) = C_{\mathrm{f}} \cdot \frac{\mathrm{d}v_{\mathrm{Cf}}}{\mathrm{d}t} - I_{\mathrm{S}} \approx -I_{\mathrm{S}}. \tag{22}$$

Typically for a small filter capacitance, $C_f \approx 10\,\mu\mathrm{F}$, the amplitude of the capacitive charging currents to meet the low-frequency (LF) sinusoidal compensation voltage is negligible compared to the ideally constant DC source current I_{S}. Interestingly, for the sizing of the buffer capacitor this approximation also holds for much larger filter capacitor values. Fig. 9 (b) depicts the switching cycle averaged buffer capacitor current, $i_{\mathrm{Cb}} = m_{\mathrm{b}} i_{\mathrm{Lf}}$, with constant filter inductor current ($i_{\mathrm{Lf}} \approx -I_{\mathrm{S}}$) and with pronounced ripple at twice the AC frequency considering a large filter capacitor, $C_{\mathrm{f}} = 100\,\mu\mathrm{F}$. Because of the averaging introduced by the duty cycle variation to generate the sinusoidal voltage at the SVI converter output, the resulting buffer capacitor charging currents are nearly identical. This also explains why the buffer capacitor does not exhibit a voltage ripple at a quadruple of the AC frequency while generating a sinusoidal voltage with twice the fundamental AC frequency at the SVI converter output. In order to ensure v_{Cf} according to (21), the H-bridge circuit must generate

$$v_{\mathrm{fb}} = v_{\mathrm{Cf}} - v_{\mathrm{Lf}} = v_{\mathrm{Cf}} - L_f \frac{\mathrm{d}i_{\mathrm{Lf}}}{\mathrm{d}t} \approx v_{\mathrm{Cf}}, \tag{23}$$

at its output terminals on average with respect to the switching cycle. Even for a large filter inductance, $L_{\mathrm{f}} = 100\,\mu\mathrm{H}$, and a large peak value of the 120 Hz superimposed charging current of $\approx 1.5\,\mathrm{A}$ (cf. Fig. 9 (b)), the amplitude of the voltage drop across the inductance only amounts to around $100\,\mathrm{mV}$ and is therefore negligible compared to v_{Cf}. Based on these approximations, the differential equation governing the buffer capacitor voltage can be expressed as

$$C_{\mathrm{b}} \frac{\mathrm{d}v_{\mathrm{b}}}{\mathrm{d}t} = m_{\mathrm{b}} \cdot i_{\mathrm{Lf}} = -\frac{v_{\mathrm{cf}}}{v_{\mathrm{b}}} I_{\mathrm{S}}, \tag{24}$$

with the analytical solution

$$v_{\mathrm{b}}(t) = \sqrt{V_{\mathrm{b},0}^2 + \frac{I_{\mathrm{S}} S_{\mathrm{b}} \cos(2\omega t - \tilde{\phi})}{2\omega^2 C_{\mathrm{b}} C_{\mathrm{dc}} V_{\mathrm{dc},0}}}, \tag{25}$$

whereby $V_{\mathrm{b},0}$ is the RMS value of the buffer capacitor voltage and represents the initial voltage at $t = \frac{\tilde{\phi} - \pi/2}{2\omega}$. Similar to the derivation of the minimum DC-link capacitance, it must hold that $v_{\mathrm{b}}(t) \geq v_{\mathrm{Cf}}(t)$ at all times which allows to calculate the theoretical minimum value of the installed buffer capacitance,

$$C_{\mathrm{b,min}} = \frac{I_{\mathrm{S}} S_{\mathrm{b}}}{2\omega^2 C_{\mathrm{dc}} V_{\mathrm{b},0}^2 V_{\mathrm{dc},0}}, \tag{26}$$

resulting in $C_{\mathrm{b,min}} = 117.9\,\mu\mathrm{F}$ for a given bias voltage of $V_{\mathrm{b},0} = 50\,\mathrm{V}$. Similar to the PCI power buffer concept, the offset or average voltage of the buffer capacitor is a degree of freedom which will be exploited in the design optimization described in the next section. The simulated waveforms for operation with minimal buffer capacitance are depicted in Fig. 9 (c). The buffer capacitor is fully utilized since its voltage drops to zero after every buffer cycle. As pointed out previously, for a practical implementation it is by far more reasonable to dimension the buffer capacitor to meet

$$\min_t v_{\mathrm{b}}(t) \geq \frac{\hat{V}_{\mathrm{cf}}}{m_{\mathrm{b,max}}}, \tag{27}$$

whereby $|m_{\mathrm{b}}| \leq m_{\mathrm{b,max}} = 0.9$ is the maximal allowed modulation index of the H-bridge (cf. Fig. 1 (d)) and $\hat{V}_{\mathrm{cf}}$ is

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the crest value of the filter capacitor voltage v_{cf}. With this condition, the minimum buffer capacitor size is given by

$$C_{\mathrm{b},\approx} = \frac{2m_{\mathrm{b,max}}^2 C_{\mathrm{dc}} V_{\mathrm{dc},0} I_{\mathrm{S}} S_{\mathrm{b}}}{4m_{\mathrm{b,max}}^2 \omega^2 C_{\mathrm{dc}}^2 V_{\mathrm{dc},0}^2 V_{\mathrm{b},0}^2 - S_{\mathrm{b}}^2} = 155.9\,\mu\mathrm{F}. \quad (28)$$

As can be seen from the waveforms in Fig. 9, installing at least $2 \cdot C_{\mathrm{b,min}} \approx 240\,\mu\mathrm{F}$ of buffer capacitance allows to approximate the exact buffer capacitor voltage (25) with

$$v_{\mathrm{b},\approx}(t) \approx V_{\mathrm{b},0} - \frac{1}{4}\frac{I_{\mathrm{S}} S_{\mathrm{b}} \cos(2\omega t - \tilde{\phi})}{\omega^2 C_{\mathrm{b}} C_{\mathrm{dc}} V_{\mathrm{dc},0} V_{\mathrm{b},0}}. \quad (29)$$

Likewise to the PCI converter, the dimensioning and loss calculation of the DC-link and buffer capacitor of the [SVI\C] buffer relies on the approximated waveforms given by (20) and (29).

B. [SVI\C] Pareto Optimization

As described in the previous section, the minimum DC-link voltage requirement of the inverter stage defines the minimum feasible capacitor size. Moreover, depending on the selected capacitor technology, also the maximum allowed ripple current imposes a restriction on the minimum feasible capacitance size. With decreasing size of the installed DC-link capacitance, the amplitude of the 120 Hz voltage ripple and thus the power and voltage rating of the SVI converter increases. In this work, the DC-link capacitance is chosen large enough such that the SVI converter only processes up to maximal 150 W and can be implemented with LV technology. In order to accomplish a cost-effective and reliable implementation of the [SVI\C] buffer, 450 V ultra-compact aluminum electrolytic capacitors from TDK (B43630 series) in the range of 390 µF - 680 µF are considered in the design optimization for the implementation of the DC-link capacitance. It would be in principle possible to implement the DC-link capacitance with ceramic capacitor technology, however, the prohibitively high cost and the large number of over 400 MLCC chips renders this design approach impractical an unreliable. Also, the minimum available electrolytic capacitor 390 µF is reasonably close to the theoretical minimum given by (18) for a maximum modulation index of 0.9 of the inverter.

For the implementation of the H-bridge, 100 V/7 mΩ E-Mode GaN transistors from EPC (EPC2001C) with unipolar PWM and a switching frequency in the range of 50 kHz - 300 kHz are considered in the design optimization. Similar to the design space of the PCI converter, for the design of the HF filter inductor L_{f} various E-type core geometries with N87 MnZn ferrite material and available HF-litz wires are considered in the optimization. For the implementation of the buffer capacitor C_{b} both 100 V/15 µF class II/X7S MLCC and 200 V ultra-compact aluminum electrolytic capacitors (also from TDK's B43630 series) are considered. For cost and assembly related restrictions as mentioned previously, a buffer capacitance range of 200 µF - 1000 µF is considered in case of the buffer capacitance implementation with MLCC. The effective capacitance for the class II/X7S buffer capacitor subject to a DC bias was obtained from the datasheet provided by the manufacturer [32]. Furthermore, the power loss due to the LF voltage ripple was calculated based on the extrapolated Equivalent Series Resistance (ESR) value of the class II/X7S MLCC specified at 1 kHz in the datasheet (minimum frequency with specified ESR value). In accordance with the available capacitance values of the 200 V B43630 series, a capacitance in the range of 390 µF - 3300 µF is considered

TABLE V
SYSTEM PARAMETERS & SEARCH LOCUS OF THE [SVI\C] CONVERTER PARETO OPTIMIZATION

Feature	Range/Option
DC-link Cap. Technology	450 V ultra-compact aluminum electrolytic (TDK B43630-Series)
C_{dc}	[390 µF, 680 µF]
Buffer Cap. Technology	100 V X7S/class II (TDK C5750X7S2A156M250KB) 200 V ultra-compact aluminum electrolytic (TDK B43630-Series)
C_b	[200 µF, 1 mF] (MLCC) [390 µF, 3.3 mF] (electrolytic cap.)
$V_{\mathrm{b},0}$	$m_{\mathrm{b},0} = [0.35, 0.65]$, $V_{\mathrm{b},0} = \hat{V}_{\mathrm{Cf}}/m_{\mathrm{b},0}$
Inductor Technology	N87 ferrite, E-core, round and HF litz wire
L_f	[1 µH, 100 µH]
Semiconductor	100 V/7 mΩ GaN e-HEMT (EPC 2001C)
f_{s}	[50 kHz, 300 kHz] (PWM w/ const. f_{s})
Heat sink	CSPI = 25.7 $\frac{\mathrm{W}}{\mathrm{K\,dm^3}}$

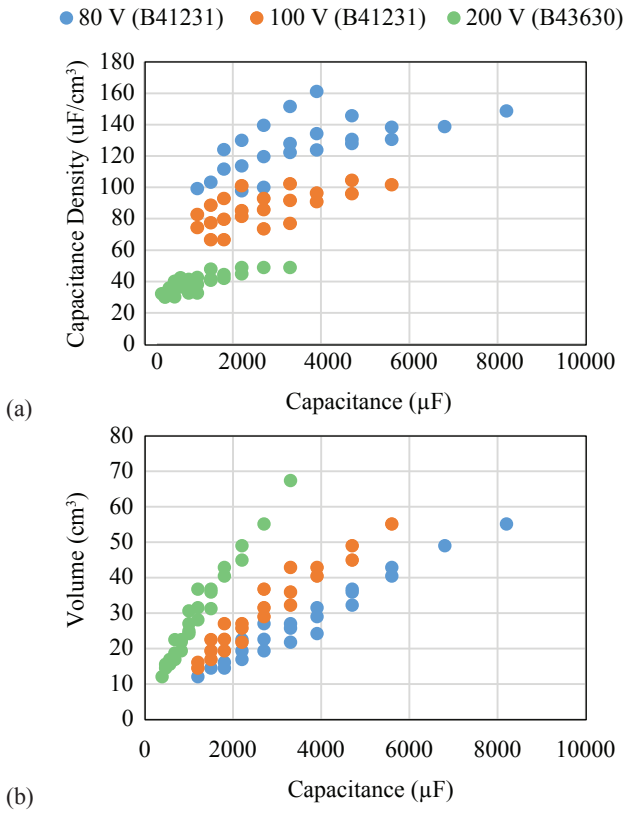

Fig. 10. (a) Capacitance density and (b) boxed volume as a function of available capacitance of TDK's B43630 and B41231 electrolytic capacitor series.

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in the design space. As shown in Fig. 10 (a), capacitors with lower voltage rating typically feature higher capacitance per volume. However, as can be seen from Fig. 10 (b), for very low capacitance values in the range of 390 µF - 1000 µF, the effective boxed volume of 80 V, 100 V and 200 V electrolytic capacitors are very similar. Thus, in order to limit the modeling effort, the same electrolytic capacitor technology (B43630 ultra-compact series) is considered for the implementation of the DC-link (450 V model) and the buffer capacitor (200 V model). As described in the previous section, the bias voltage of the buffer capacitor is a further degree of freedom in the optimization and is adjusted by means of varying the average modulation index of the SVI converter,

$$m_{\mathrm{b},0} = \frac{\hat{V}_{\mathrm{Cf}}}{V_{\mathrm{b},0}}, \tag{30}$$

in the range of 0.35 - 0.65 for a given size of the DC-link capacitor and resulting output voltage amplitude $\hat{V}_{\mathrm{Cf}}$. The design space variables are summarized in Tab. V. Given the described design space and elaborate loss and volume models of the utilized components, a large number of possible [SVI\C] designs was calculated. Fig. 11 (a) and (b) display the $\eta\rho$-performance of the designs with aluminum electrolytic and ceramic buffer capacitor, respectively. Designs with different DC-link capacitor size are distinguished by color.

As can be seen in Fig. 11 (a), using electrolytic capacitors to implement the buffer capacitance, a maximal power density of about 35 $\frac{\mathrm{kW}}{\mathrm{dm}^3}$ (574 $\mathrm{W/in}^3$) at an efficiency of 99.77 % is achieved for design (S5) with the smallest considered DC-link capacitance of 390 µF. As can be seen from Fig. 11 (b), the power density can be further increased if the buffer capacitor is implemented with 100 V/X7S ceramic capacitors. For the smallest available DC-link capacitance, a maximal power density of almost 45 $\frac{\mathrm{kW}}{\mathrm{dm}^3}$ (737 $\mathrm{W/in}^3$) at a nominal efficiency of 99.83 % of design (S1) is possible according to the optimization results.

The volume and loss distribution of several selected Pareto optimal designs is shown in Fig. 12 (a) and (b), respectively. From the volume balance it can be clearly seen that the size of the DC-link capacitor is dominating the overall volume. Comparing the two designs with maximal power density (S1) and (S5) using ceramic and electrolytic capacitor, it can be seen that the higher power density of design (S1) is mainly ascribed to the more compact implementation of the buffer with X7S MLCC. As can be seen from Fig. 12 (b), the electrolytic buffer capacitor also exhibits higher power loss.

The realized design indicated with label (H3) in Fig. 11 (b) and described in detail in Section III-D achieves a power density of 34.5 $\frac{\mathrm{kW}}{\mathrm{dm}^3}$ (565 $\mathrm{W/in}^3$) at an efficiency of 99.5 %.

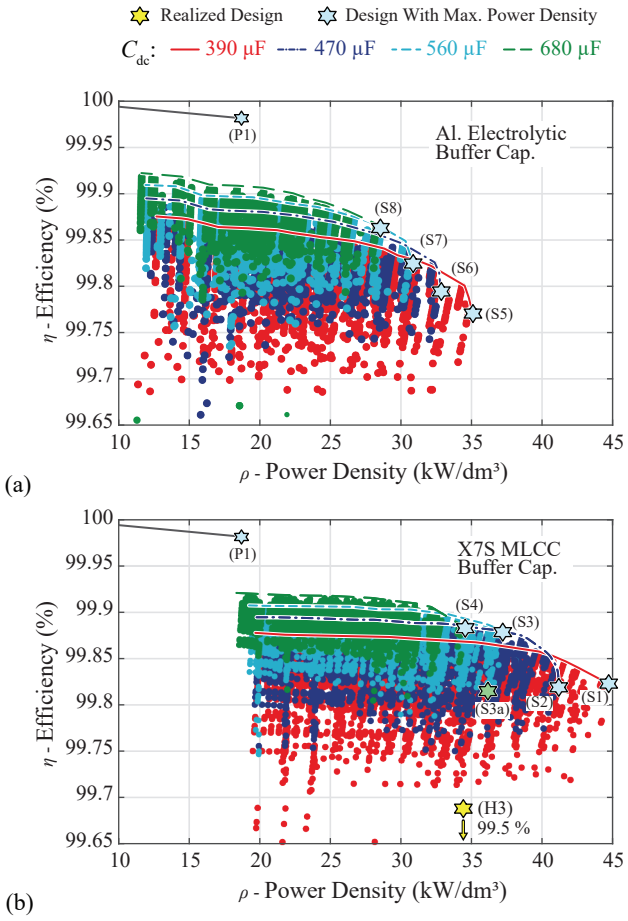

Fig. 11. $\eta\rho$-plot of the calculated [SVI\C] designs with indicated Pareto fronts. (a) Both DC-link and buffer capacitor are implemented with 450 V and 200 V electrolytic capacitor technology, respectively. (b) The DC-link is implemented with 450 V electrolytic capacitor technology and the buffer capacitor is implemented with 100 V class II/X7S MLCC technology.

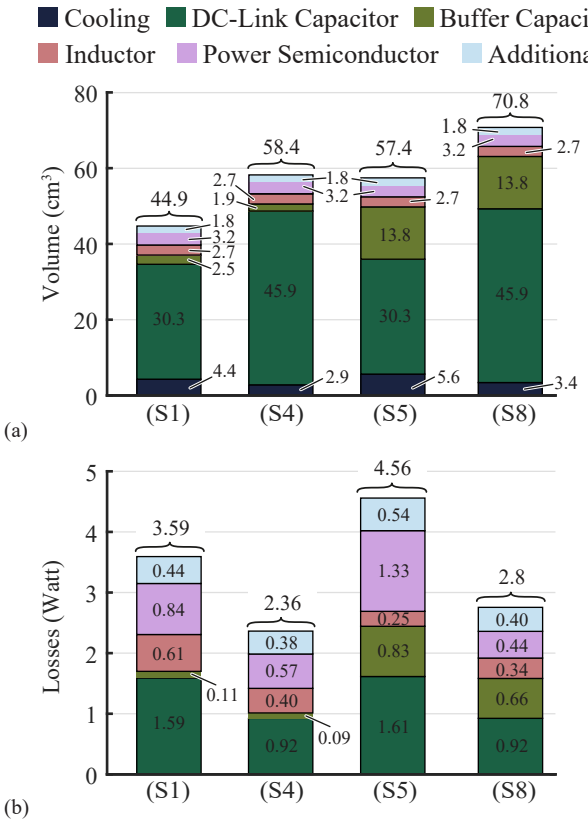

Fig. 12. (a) Volume and (b) loss distribution of selected Pareto optimal [SVI\C] designs.

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C. Control System of the SVI converter

The control system proposed to regulate the SVI converter is depicted in Fig. 13. The installed DC-link capacitor is large enough to prevent severe overshoots and sags in the DC-link voltage during load transients. For this reason, there is less demand on the dynamic performance of the control system which allows to omit the feed-forward control of the fluctuating AC power and the cascaded DC-link voltage control. Referring to Fig. 13, control subsystem (c) cancels the 120 Hz voltage ripple present in v_{dc}. The reference $v^*_{\mathrm{dc},\sim}$ of the auxiliary converter output voltage control is obtained by means of subtracting the average DC-link voltage, $v_{\mathrm{dc},=}$, from the measured value v_{dc}. In order to extract the average DC-link voltage $v_{\mathrm{dc},=}$ a moving-average low-pass filter with window size of one 120 Hz period is employed. A purely resonant compensator (proportional gain set to zero) tuned at 120 Hz is employed to regulate the output voltage v_{cf} to precisely track the reference $v^*_{\mathrm{dc},\sim}$ and thus completely cancel the 120 Hz voltage ripple present in v_{dc}. Likewise to the PCI converter controls presented in the Section II-B, control subsystem (a) is employed to keep the mean value of the buffer capacitor voltage $\bar{v}_b = V_b$ at a chosen reference. The output of the PI controller, current reference i^*_{Cb}, is multiplied with the constant scaling factor $-V_{\mathrm{b,nom}}/I_{\mathrm{S,nom}}$ to obtain voltage reference $\overline{v}^*_{\mathrm{cf}}$. This scaling factor relates the charging/discharging power of the buffer capacitor, $v_{\mathrm{b}} \cdot i_{\mathrm{b}}$, to the power which must be provided/absorbed at the output of the SVI converter $\approx v_{\mathrm{cf}} I_{\mathrm{s}}$. According to the voltage/current directions as shown in Fig. 13 and the condition $I_{\mathrm{S}} \geq 0$, a positive/negative bias in v_{Cf} discharges/charges the buffer capacitor over time, respectively. During idle mode of the converter, when no real power is transferred to the AC side and I_{S} is essentially zero, the buffer capacitor voltage cannot be kept at its desired bias voltage level. For this reason it is crucial to include an anti-windup logic in the series compensating voltage PI controller. The average filter capacitor bias voltage $\overline{v}_{\mathrm{Cf}}$ is then regulated to meet the reference $\overline{v}^*_{\mathrm{Cf}}$ by means of an inner-loop PI controller which outputs current reference $i^*_{\mathrm{Cf},=}$ (cf. Fig. 13 (a)). Similar to the PCI converter controls described previously, the control objectives are combined in a single reference for the filter inductor current, i^*_{Lf}. Note that the source current I_{S} must flow entirely through L_{f} since it holds that $\bar{i}_{\mathrm{Cf}} = 0$ in steady-state. For this reason, $i^*_{\mathrm{Lf},=}$ is calculated based on the real power of the AC load and added to the filter current reference (cf. Fig. 13 (b)). A satisfying initial set of control parameters for the PI and Resonant compensators was empirically determined with the aid of extensive circuit simulations and then fine tuned during testing of the converter prototype (cf. Section III-D).

D. Hardware Implementation and Experimental Verification

Benefiting from the gained insights of the design optimization in Section III-B, a prototype of the [SVI\C] buffer as shown in Fig. 14 was implemented in hardware. The design parameters and selected features of the realized system are summarized in Tab. VI. By the courtesy of TDK, a custom 560 µF/450 V aluminum electrolytic capacitor with $\approx$ 40 % higher capacitance density but reduced lifetime compared to B43630 series (cf. Section III-B) was available. The buffer capacitor C_{b} was implemented with a total of 45 single 15 µF/100 V, class II/X7S MLCC chips. With a bias voltage of the buffer capacitor set to 55 V in the control system (cf. Section III-C), the effective large-signal capacitance amounts to 260 µF.

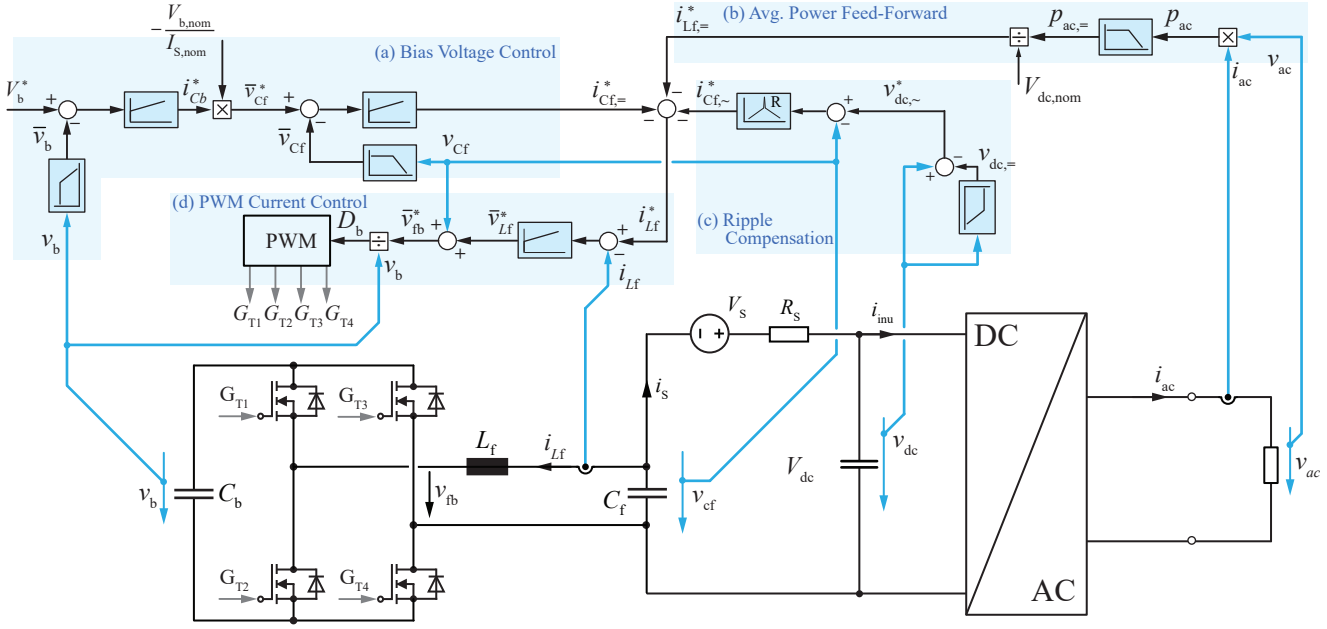

Fig. 13. Proposed cascaded control structure of the SVI converter of the [SVI\C] power buffer. (a) Control of the average buffer capacitor voltage $\overline{v}_{\mathrm{b}}$. (b) Feed-forward control of the average AC power (real power). (c) Compensation of the DC-link voltage ripple. (d) Inner loop control of filter inductor current i_{Lf} with PWM.

TABLE VI
TECHNICAL DETAILS OF THE REALIZED [SVI\C] BUFFER.

Feature	Value	Description
Volume (no cooling)	$54.0\,\mathrm{cm}^3$ $(2.1\,\mathrm{in}^3)$	Boxed component volume of the [SVI\C] buffer without heat sink
Volume (with cooling)	$58\,\mathrm{cm}^3$ $(3.5\,\mathrm{in}^3)$	Total volume of the constructed [SVI\C] buffer with a CSPI $= 27.5\,\frac{\mathrm{W}}{\mathrm{K\,dm}^3}$ heat sink
Capacitor volume	$42.9\,\mathrm{cm}^3$ $(2.6\,\mathrm{in}^3)$	Total volume of installed buffer capacitor and DC-link capacitor volume (boxed)
η	$99.52\,\%$	Efficiency at $2\,\mathrm{kW}$
L_f	$33\,\mu\mathrm{H}$	Coilcraft XAL1510-333MED
C_f	$60\,\mu\mathrm{F}$	$4 \times 15\,\mu\mathrm{F}$ 100 V/X7S MLCC
C_b	$260\,\mu\mathrm{F}$	Equivalent large signal capacitance of the installed $45\times$ $15\,\mu\mathrm{F}/100\,\mathrm{V}$/X7S MLCC
C_dc	$560\,\mu\mathrm{F}$	Ultra-compact aluminum electrolytic capacitor technology (EPCOS B43991-X0009-A224)

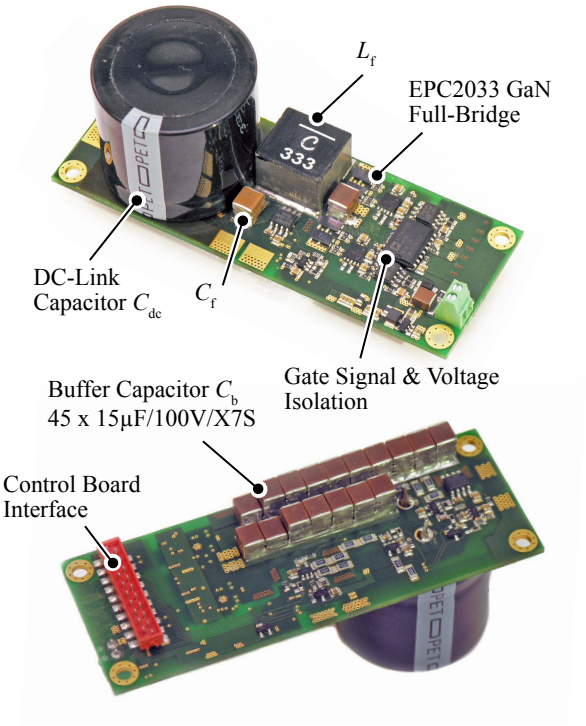

Fig. 14. Picture of the implemented [SVI\C] buffer. The shown aluminum electrolytic capacitor is buffering the DC-link and the buffer capacitor of the SVI converter is implemented with ceramic capacitors.

Since the EPC2001C $7\,\mathrm{m\Omega}/100\,\mathrm{V}$ GaN transistors were unavailable at the time of the prototype design, the H-bridge was implemented with EPC2033 $7\,\mathrm{m\Omega}/150\,\mathrm{V}$ e-mode GaN transistors from EPC which feature similar $R_\mathrm{ds,on}$ values but higher output capacitance C_oss. The switching frequency per bridge-leg is set to $70\,\mathrm{kHz}$ which, in case of the employed unipolar PWM, corresponds to an effective switching frequency of $140\,\mathrm{kHz}$ and matches the switching frequency of the 2nd version of the Little Box inverter operated with PWM (cf. Fig. 5 (b)). The gate-drive is implemented based on the LM5113 half-bridge driver IC with bootstrap supply of the high-side transistors. In addition, power and gate-signal isolation is implemented with the ADuM500 and SI8620 ICs, respectively. The filter inductor, $L_\mathrm{f} = 33\,\mu\mathrm{H}$, was implemented by means of an off-the-shelf available inductor from Coilcraft's XAL1510 series (XAL1510-333MED, $12\,\mathrm{A}$, $R_\mathrm{dc} = 20\,\mathrm{m\Omega}$). The maximum current ripple amounts to approximately $2.5\,\mathrm{A}$ peak-to-peak and occurs at the maximum of the output voltage v_Cf. The control system proposed in the previous section was also implemented on the *TMS320F28335* microcontroller from Texas Instruments which was located on an external control PCB (cf. Fig. 14, control board interface). All necessary analog measurement circuits to sense v_dc, v_cf, i_Lf, and the buffer voltage v_b are placed on the prototype PCB. The inner current feedback loop is executed with a frequency of $140\,\mathrm{kHz}$ and the voltage feedback loops and feed-forward control are executed at $28\,\mathrm{kHz}$.

The efficiency according to (12) of the [SVI\C] buffer measured with a Yokogawa WT3000 precision power analyzer is depicted in blue in Fig. 15. For comparison, the efficiency curves of the two variants of PCI converter presented in Section II-C are shown in grey. At rated output power of $2\,\mathrm{kW}$, the [SVI\C] buffer exhibits an efficiency of $99.52\,\%$. As can be seen, at high output power $> 1.7\,\mathrm{kW}$, the efficiency of the PCI converter with class II/X6S capacitors is just slightly lower. However as mentioned before, one of the major

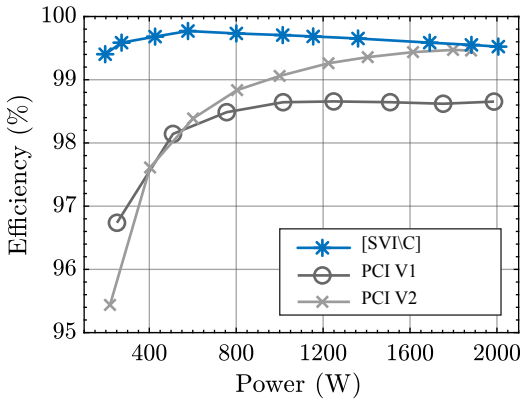

Fig. 15. Measured efficiency of the constructed [SVI\C] buffer prototype as a function of apparent power S_b. For reference, the efficiency of the PCI converter prototypes is shown in grey.

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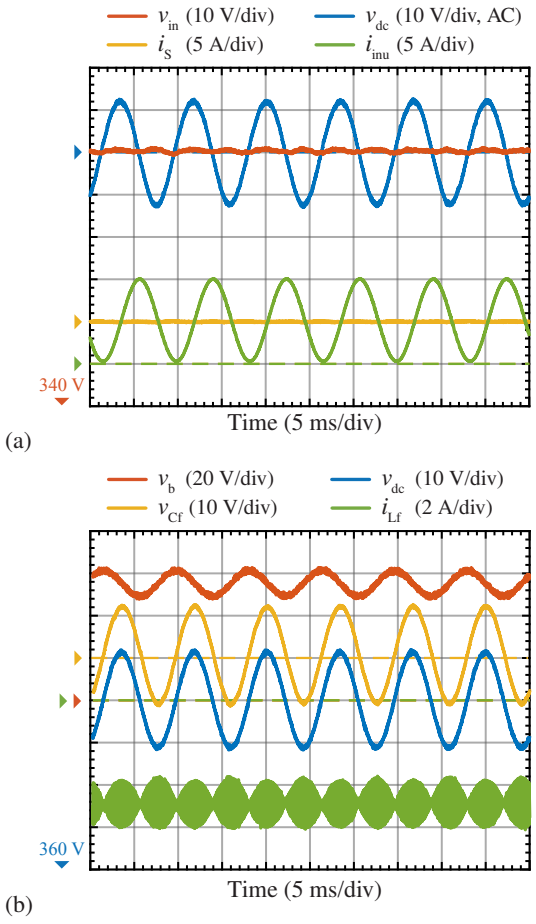

Fig. 16. Steady-state performance of the realized [SVI\C] buffer at 2 kW rated power. (a) Characteristic waveforms of the SVI converter. (b) Elimination of DC-link voltage ripple and resulting constant input voltage, v_{in}, and source current i_{s}.

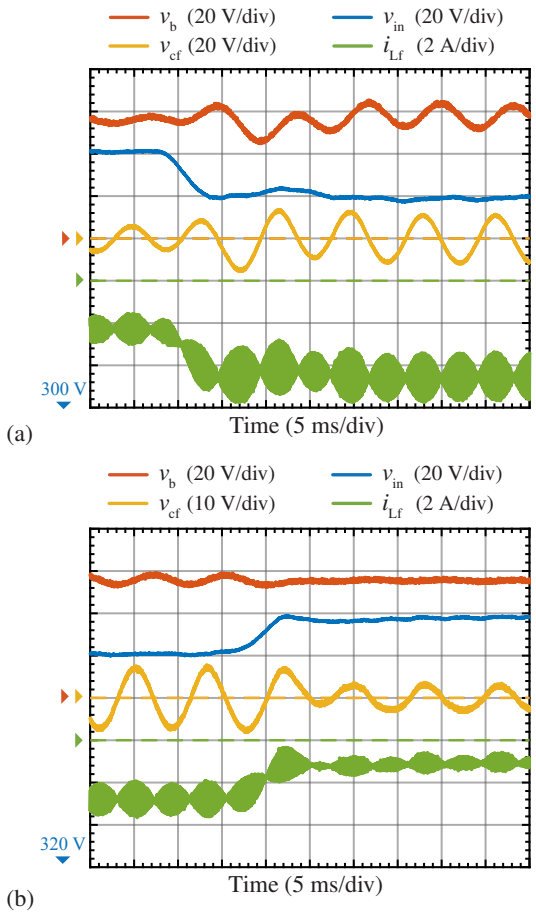

Fig. 17. [SVI\C] buffer transient response to (a) an abrupt load step from 1000 W to 2000 W and (b) an abrupt load drop from 1250 W to 500 W.

advantages of the [SVI\C] approach is the excellent partial-load efficiency. The measured peak efficiency amounts to 99.8 % at about 578 W output power. Even at a very low output power of around 200 W, the efficiency of the buffer remains above 99.2 %. The achieved power density based on aggregated boxed component volume amounts to 34.5 $\frac{\mathrm{kW}}{\mathrm{dm}^3}$ (565 $\mathrm{W/in}^3$). Since the [SVI\C] buffer prototype was designed to facilitate testing in the laboratory, the components were not arranged to fit tightly in a rectangular enclosure and using the boxed volume of the entire prototype would lead to wrong conclusions regarding the achieved power density of the implemented [SVI\C] buffer.

The steady-state performance at 2 kW rated power of the proposed control system is illustrated by the experimental measurements shown in Fig. 16. It can be seen from the recorded converter input voltage (cf. v_{in} in Fig. 16 (a)) that the 120 Hz voltage ripple in the DC-link voltage v_{dc} is almost entirely compensated. Note, that the ripple of v_{dc} with an amplitude of around 22 $\mathrm{V_{pp}}$ would violate the GLBC technical specification of 12 $\mathrm{V_{pp}}$ (3 % of 400 V). Although the current provided to the inverter, i_{inu}, exhibits the characteristic squared sinusoidal shape with a peak current of 10 A for delivering 2 kW of real power to the inverter, the current coming from the source i_{S} is perfectly constant due to the operation of the SVI converter. The characteristic waveforms of the auxiliary converter during stationary operation at rated power are shown in Fig. 16 (b). As discussed in Section III-A, because of the source current bias of i_{Lf} and the small amplitude of the required 120 Hz charging current such that v_{Cf} compensates the voltage ripple present in v_{dc}, the buffer capacitor voltage v_{b} exhibits only a distinct 120 Hz voltage ripple and no 240 Hz component. In order to verify the dynamic performance of the implemented control system, the main DC/AC converter was subject to load variations. The corresponding transient performance of the [SVI\C] buffer for a load step from 1 kW to 2 kW is depicted in Fig. 17 (a). Triggered by the load step, the average SVI buffer capacitor voltage drops only roughly $R_{\mathrm{s}} = 10$ V below the 55 V at steady-state and recovers within 20 ms. The voltage controller immediately adapts v_{Cf} to the increased amplitude of the DC-link voltage ripple which facilitates a very smooth transition of both the input voltage v_{in} and input current i_{S}. As already pointed out before, because of the 10 Ω input resistor (cf. Fig. 1), the input voltage v_{in} decreases with increasing power and therefore settles at a lower value after the transient. As a consequence of the increase in power being processed by the SVI converter, the

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amplitude of the characteristic 120 Hz voltage ripple across the buffer capacitor becomes more pronounced immediately after the load step. Analogously, a step down from 1250 W to 500 W is depicted in Fig. 17 (b). Triggered by the load drop, the input voltage and current attains the new steady-state value smoothly without any overshoot. The output voltage v_{Cf} is immediately adjusted by the control system and therefore no considerable voltage fluctuation is present in v_{in} even during the transient which is approximately settled within 15 ms - 20 ms. This also clearly surpasses the required performance of the GLBC technical specifications.

IV. Discussion

Fig. 18 summarizes and compares the Pareto optimization results of the PCI buffer presented in Section II-A and the [SVI\C] buffer presented in Section III-B. In general, both the PCI converter equipped with 450 V class II/X6S MLCC and the [SVI\C] buffer equipped with 100 V class II/X7S MLCC and a 390 µF electrolytic DC-link capacitor can reach power densities above 40 $\frac{\mathrm{kW}}{\mathrm{dm}^3}$ (656 $\mathrm{W/in}^3$) and high efficiencies above 99.4 % at rated power. Based on the Pareto optimization results, it seems that the [SVI\C] buffer approach can potentially outperform the PCI converter both in terms of power density and conversion efficiency. However, in accordance with the experimental results presented in the previous chapter, this has not been demonstrated in hardware so far. The maximum power density of 41.3 $\frac{\mathrm{kW}}{\mathrm{dm}^3}$ (677 $\mathrm{W/in}^3$) was achieved with the PCI converter prototype equipped with 450 V class II/X6S MLCC and operated with 140 kHz PWM. Moreover, the implemented [SVI\C] buffer prototype (cf. Fig. 14) is a first, proof-of-concept implementation primarily designed to facilitate experimental testing and verify the proposed control system described in Section III-C. For this reason, the components have not been arranged to fit tightly into a cuboidal shape with minimum volume as it is the case for the PCI converter prototypes (cf. Fig. 5), which are already in a later, refined stage of development. As mentioned before, for a fair comparison, the sum of all boxed component volumes was used to calculate the power density of the [SVI\C] buffer prototype rather than the boxed rectangular volume of the entire system shown in Fig. 14.

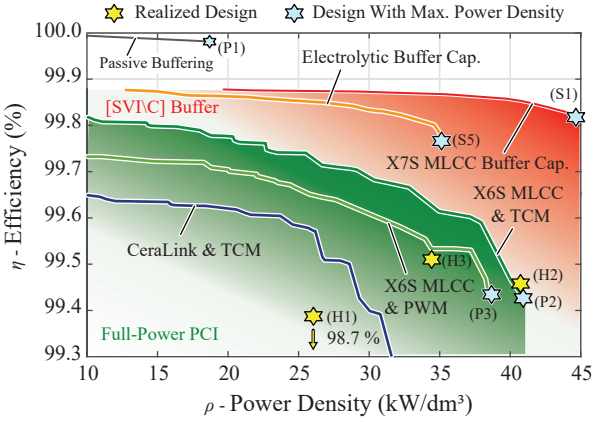

Fig. 18. Comparison of calculated $\eta\rho$-Pareto fronts of the PCI buffer and the [SVI\C] buffer.

It is worth noting that, by employing aluminum electrolytic capacitors to implement both the DC-link and the buffer capacitance, the [SVI\C] buffer can still potentially reach high power densities up to 35 $\frac{\mathrm{kW}}{\mathrm{dm}^3}$ which outperforms the PCI converter with TCM modulation and CeraLink capacitors. This is particularly of interest regarding a cost-effective realization of the active power buffer. To exemplify, the 2nd version of the presented PCI converter uses 200 pieces of the 2.2 µF/450 V class II/X6S MLCCs which amounts to $290 of component cost for the buffer capacitor (order quantities above 1000 pieces considered). In contrast, a 390 µF/450 V electrolytic capacitor costs $4 and a 390 µF/200 V electrolytic capacitor costs just $2. Hence, the capacitor component cost of the all-electrolytic [SVI\C] buffer design (S5) amounts to only about $6. Striving for maximum power density, the buffer capacitor can be implemented with 35× 15 µF/100 V X7S MLCC (S1) which amounts to $62.3 and therefore results in a total capacitor component cost of about $66.3 for the [SVI\C] system. From this point of view, the [SVI\C] buffer and in particular the all-electrolytic [SVI\C] buffer is a very cost competitive approach and clearly outperforms the PCI converter in this regard. Although it was not considered in the optimization of the PCI converter, it is in principle also possible to use aluminum electrolytic capacitors to implement C_{b} and thus achieve a significantly lower cost. However, because of the imposed lifetime related ripple current limitations, the minimum feasible buffer capacitor size results in a comparably low capacitor utilization (small amplitude of the buffer voltage swing) and it is therefore unlikely that this approach would actually yield a $\eta\rho$-competitive design.

As can be seen from the measured efficiencies of the implemented buffer prototypes (cf. Fig. 15), the [SVI\C] approach features the highest efficiency of 99.5 % at rated output power as opposed to the efficiency of 99.4 % of the PCI converter with class II/X6S MLCCs. It is important to mention that the worst case power measurement accuracy of the employed Yokogawa WT3000 power analyzer [33] amounts to ±8 W which corresponds to an uncertainty of the measured efficiency of up to ±0.4 %. This also suggests that the discrepancy between the efficiency of the Pareto optimal design S1 and the realized hardware H3 (cf. Fig. 18) is, besides a suboptimal implementation of the SVI converter and imperfections in the underlying component models of the optimization, attributed to uncertainty in the power measurements.

Due to the nature of the partial-power approach, the auxiliary converter only processes a small share of the entire fluctuating power and thus exhibits a very low power loss which explains the high efficiency. In this regard, one of the clear advantages of the [SVI\C] buffer is its excellent partial-load efficiency. At 500 W output power, the efficiency of the implemented [SVI\C] system amounts to around 99.7 % in contrast to the substantially lower efficiency of 98 % of the implemented PCI converter. The high partial-load efficiency is in particular beneficial to achieve a high CEC or European weighted efficiency of the inverter equipped with active buffer.

The presented experimental waveforms of the implemented

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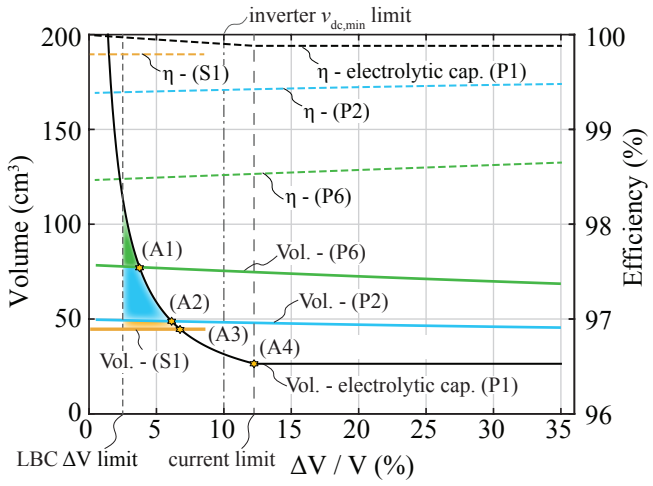

Fig. 19. Volume and efficiency comparison between conventional DC-link with electrolytic capacitors and optimally designed current or voltage injection power buffers with respect to the 2.5 % ΔV limit specified in [1].

prototypes are clearly demonstrating that the proposed control systems in Section II-B and Section III-C, both achieve excellent mitigation of the 120 Hz DC-link voltage ripple and also clearly meet the transient response requirements specified in [1]. Because of the still comparably large size of the installed aluminum electrolytic capacitor in case of the [SVI\C] buffer, abrupt load changes are handled with much less demand on the dynamic performance of the control system because the DC-link capacitance provides enough passive buffering to temporarily accommodate the power mismatch between DC and AC side without pronounced sags or overshoots in the DC-link voltage. On the contrary, the small remaining DC-link capacitor of around 15 µF in case of the PCI converter concept, intended as commutation capacitor to reduce the parasitic inductance of the power loop, requires active stabilization of the DC-link voltage which leads to a somewhat more complicated control system. From this perspective, it can be argued that the [SVI\C] buffer in combination with the proposed control system for the SVI is more robust and exhibits better transient performance.

It is also interesting to compare the performance of the power buffers based on parallel current or series voltage injection with a conventional passive DC-link comprised of electrolytic capacitors and to determine the voltage ripple $\frac{\Delta V}{V}$ limit when it actually becomes beneficial in terms of volume to employ a converter based buffer concept and accept the increased hardware effort. A volume model was extracted by means of a least-square fit to the calculated boxed volumes of all possible DC-link assemblies generated with the ultra-compact 450 V electrolytic capacitors from TDK considered in this work [34], allowing at maximum five capacitors to be connected in parallel. The resulting volume of the DC-link with respect to the voltage ripple limit is depicted in Fig. 19. Decreasing ΔV results in a larger volume since more electrolytic capacitors have to be installed to meet the more stringent requirement. Likewise, relaxing the voltage ripple limit results in a volume reduction until the specified ripple current limitation of the electrolytic capacitor prevents a further reduction in volume (A4). Given the calculated ESR for each capacitor assembly obtained from the data provided in [34], [35], the power losses caused by the 120 Hz charging current is calculated and the resulting efficiency is depicted in Fig. 19. The Pareto optimal design (P2) with TCM and class II/X6S capacitors, and the optimal design (P6) with TCM and CeraLink capacitors were chosen from the PCI converter designs for the volume benchmarks. Typically, the proposed control system as proposed in Section II-B achieves complete ripple cancellation, but can be modified to tolerate a certain ΔV across C_{dc}, which slightly changes the rated power of the PCI converter design according to $\tilde{S}_b = S_b - \Delta E_{\mathrm{dc}}\omega$. The performance of the designs (P2) and (P6) were recalculated for several voltage ripple limits. Likewise, the Pareto optimal [SVI\C] buffer design (S1) is also included in the benchmark. For the 390 µF DC-link capacitor employed in (S1), the voltage ripple at the input, if the SVI converter compensation reference is set to zero, amounts to $\Delta V = 34$ V and explains why the trace stops at $\frac{\Delta V}{V} \approx 8.5\,\%$. As indicated by intersection (A2) between the total volume of design (P2) and the electrolytic capacitor, it becomes beneficial (only considering volume) to employ a PCI converter if a $^{\Delta V}/_{V} = 6\,\%$ or less is demanded. For the design (P6) with CeraLink the intersection (A1) occurs at $^{\Delta V}/_{V} = 3.7\,\%$. Considering the intersection (A3) between the total volume of the optimal [SVI\C] buffer design (S1) and the electrolytic capacitor, it becomes beneficial to employ an [SVI\C] buffer (with ceramic buffer capacitor) if a $^{\Delta V}/_{V} = 6.8\,\%$ or less is demanded. Also indicated in the plot is the admissible 2.5 % voltage ripple limit specified in [1] (cf. Section I), which reveals that roughly 35 cm^3 of volume were saved with the PCI converter (CeraLink/TCM) in the 1st version of the Google Little Box and about 65 cm^3 of volume were saved with the PCI buffer (class II/X6S-PWM) in case of the 2nd implementation of the Little Box. Concerning efficiency, Fig. 19 shows that passive capacitive DC-link buffering with electrolytic capacitors always achieves a higher efficiency compared to an optimal designed buffer employing current or voltage injection stages regardless of the specified voltage ripple limit.

V. Conclusion

In order to shrink the volume of the energy storage required in single-phase inverter systems to cope with the 120 Hz fluctuating AC power, the power pulsation buffer concepts selected by the 1st and 2nd prize winner of the Google Little Box Challenge (GLBC) were analyzed in detail and comparatively evaluated in this paper. Based on Pareto optimization results, the full-power processing Parallel Current Injector (PCI, approach of the 1st prize winner) can reach power densities as high as 41.3 $\frac{\mathrm{kW}}{\mathrm{dm}^3}$ (677.1 $\mathrm{W/in}^3$) mainly because of the small feasible buffer capacitance values. The [SVI\C] buffer (approach of the 2nd prize winner) employing a partial-power Series Voltage Injector (SVI) converter equipped with 100 V class II/X7S ceramic capacitors can reach power densities as high as 45 $\frac{\mathrm{kW}}{\mathrm{dm}^3}$ (737 $\mathrm{W/in}^3$) and mainly benefits from the low heat sink volume due to its very high

efficiency. Experimental results obtained from three prototype implementations of the considered concepts were presented. The first version of the PCI converter employing CeraLink capacitors features an efficiency of $98.7\,\%$ at rated power and an overall volume of $76.6\,\mathrm{cm}^3$ ($4.7\,\mathrm{in}^3$) which corresponds to a power density of $26.1\,\frac{\mathrm{kW}}{\mathrm{dm}^3}$ ($428\,\mathrm{W/in}^3$). The second version of the PCI converter employing $450\,\mathrm{V}$ class II/X6S capacitors features an efficiency of $99.4\,\%$ at rated power and an overall volume of $48.4\,\mathrm{cm}^3$ ($3.0\,\mathrm{in}^3$) which corresponds to a power density of $41.3\,\frac{\mathrm{kW}}{\mathrm{dm}^3}$ ($676.8\,\mathrm{W/in}^3$). The implemented [SVI\C] buffer prototype achieved an efficiency of $99.5\,\%$ at rated power and an overall volume of $58\,\mathrm{cm}^3$ ($3.5\,\mathrm{in}^3$) which corresponds to a power density of $34.5\,\frac{\mathrm{kW}}{\mathrm{dm}^3}$ ($565\,\mathrm{W/in}^3$). Clearly, one major advantage of the presented [SVI\C] buffer is the remarkable partial-load efficiency with a measured peak value of $99.8\,\%$ at $\approx 580\,\mathrm{W}$ output power. According to the comparison with a conventional capacitive buffered DC-link using only electrolytic capacitors, it becomes beneficial in term of volume to employ an optimized active power buffer if a ripple requirement of $^{\Delta V}/_{V} = 6 - 7\,\%$ or less is demanded by the application. The outstanding performance of the presented cascaded control structures for the PCI and [SVI\C] buffer under stationary conditions ($120\,\mathrm{Hz}$ voltage ripple compensation) and subject to stepwise load changes was demonstrated by means of experimental waveforms which showed that the technical requirements of the Google Little Box Challenge (GLBC) were clearly met. Because of the still comparably large capacitance provided by the installed electrolytic capacitor in case of the [SVI\C] buffer approach, abrupt load changes are handled with much less demand on the dynamic performance of the digital control system. With respect to cost, it is possible to implement an all-electrolytic [SVI\C] buffer design with, according to the conducted Pareto optimization, still high power density of $\approx 35\,\frac{\mathrm{kW}}{\mathrm{dm}^3}$ ($574\,\mathrm{W/in}^3$) but at a very low expense of only \$ 6 of total capacitor cost as opposed to the \$ 290 needed to implement the class II/X6S buffer capacitor of the presented PCI buffer approach.

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