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99% Efficient Isolated Three-Phase Matrix-Type DAB Buck-Boost PFC Rectifier

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***Abstract*—Three-phase power factor correction rectifiers are an essential area of power electronics, supplying a direct current load with tens of kW, or more, from the public three-phase mains and achieving sinusoidal input currents. In many applications isolation is required between the mains and the load, for example due to safety reasons or different grounding schemes. This paper describes the modulation, design and realization of a buck-boost-type, unity power factor, isolated matrix-type, dual active bridge, three-phase rectifier (IMDAB3R). It uses a circuit similar to a conventional dual active bridge converter, but employs a direct matrix converter to connect the high frequency transformer's primary winding to the mains. A soft switching modulation scheme is proposed and comprehensively analyzed, deriving closed form solutions and numerical optimization problems to calculate switching times that achieve minimal conduction losses. Based on this analysis, the design of an 8 kW, 400 V rms three-phase ac to 400 V dc prototype is discussed, striving for the highest possible efficiency. Using 900 V SiC MOSFETs and a transformer with integrated inductor, a power density of 4 kW dm^{-3} (66 W in^{-3}) is achieved. Measurement results confirm an ultra-high full-power efficiency of 99.0 % at nominal operating conditions and 98.7 % at 10 % lower input voltage.**

***Index Terms*—Isolated Rectifier, Three-Phase PFC Converter, Direct Matrix-Type, Dual Active Bridge**

I. Introduction

In recent years the number and power demand of intrinsic dc loads has increased significantly in residential areas and commercial or office buildings. These loads include electric vehicles, LED lighting, variable speed drives for energy efficient air conditioning and ventilation systems and information and communication technology equipment, such as desktop computers, servers and data centers. At the same time the amount of generated dc power increases as well, as renewable energy sources, such as photovoltaic panels and small-scale wind turbines, produce a direct current. Hence, dc distribution systems that span either only a single commercial building, industrial plant or a full residential area are expected to reduce conversion losses, improve reliability and/or lower cost. These so-called dc microgrids have received significant attention in scientific literature, research and industry [1–4].

The same benefits are also expected for dc distribution systems in data centers as the number of conversion stages can be reduced [5–8]. As data centers and telecommunication equipment consume significant amounts of power and are typically operated 24/7, the conversion losses of rectifiers and dc-dc converters constitute a significant share of a site's operational expenses, and circuit efforts resulting in efficiencies as high as 99 % are economically feasible in this case [9–11].

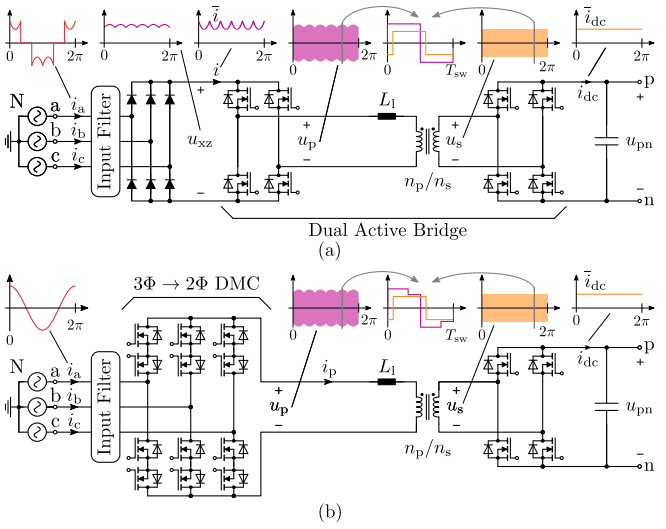

Fig. 1. Isolated single-stage three-phase rectifier circuits: In (a) a diode bridge is used to create a six-pulse voltage u_{xz} which supplies a Dual Active Bridge (DAB) dc-dc converter that provides galvanic isolation and creates an output voltage u_{pn} that can be higher or lower than u_{xz}. As only two front-end rectifier diodes conduct at any time, the resulting mains currents $i_{\mathrm{a,b,c}}$ are nonsinusoidal. (b) By using a 3-to-2 Direct Matrix Converter (DMC), any line-to-line mains voltage can be selected as primary side winding voltage u_{p}, which enables operation with sinusoidal mains currents [12–14]. This circuit is analyzed and denominated Isolated Matrix-Type DAB Three-Phase Rectifier (IMDAB3R) in this paper.

Typically, loads of tens to hundreds of kilowatts are supplied, which implies that three-phase power factor correction (PFC) rectifiers are required to supply the dc bus from the conventional ac mains. In many applications two conversion stages are used, where a three-phase boost-type PFC front end provides an $\approx$ 800 V dc voltage which is stepped down by a dc-dc converter to the dc bus voltage of $\approx$ 400 V, yielding a two-stage system. Galvanic isolation can be included in the dc/dc converter if this is required by the application, for example due to safety reasons or grounding schemes. Alternatively, this conversion process between the mains and a dc output voltage can also be performed by different isolated matrix-type three-phase PFC rectifiers in a single stage without an intermediate dc voltage and/or energy storage [15–23].

One of the simplest isolated single-stage three-phase rectifier circuits is shown in Fig. 1(a). It consists of an input filter, a diode rectifier bridge providing the six-pulse voltage u_{xz} and a dual active bridge (DAB) arrangement used as isolated dc/dc converter. Using a DAB converter has the advantage that

TABLE I
NOMINAL OPERATING CONDITIONS & CONVERTER SPECIFICATIONS

Input Voltage (Line-to-Neutral)	$U_1 = 230\,\mathrm{V}$ rms
Input Frequency	$\omega = 2\pi\,50\,\mathrm{Hz}$
Nominal DC Output Voltage	$U_{\mathrm{pn}} = 400\,\mathrm{V}$
Nominal Output Power	$P = 8\,\mathrm{kW}$
Nominal Switching Frequency	$f_{\mathrm{sw}} = 31\,\mathrm{kHz}$
Leakage Inductance	$L_{\mathrm{l}} = 36\,\mu\mathrm{H}$
Turns Ratio	$n_{\mathrm{p}}/n_{\mathrm{s}} = 22/17 \approx 1.29$

only a single magnetic component, the isolation transformer, is required, provided that it is designed with a sufficiently large leakage inductance L_{l} and it enables both buck- and boost-operation. This means that the output voltage u_{pn} can be higher or lower than the six-pulse voltage u_{xz}. However, only two diodes of the input rectifier conduct at any time and therefore the resulting mains input currents $i_{\mathrm{a,b,c}}$ are not sinusoidal. To overcome this, the diode rectifier and the DAB converter's primary side full bridge can be replaced with a direct matrix converter (DMC) as shown in Fig. 1(b). This circuit was proposed in [12] as vehicle-to-grid interface with bidirectional power flow and in [13] and [14] as inverter. The resulting circuit is called Isolated Matrix-Type DAB Three-Phase Rectifier (IMDAB3R) in this paper. The modulation schemes described in the above mentioned publications both lead to low-order harmonics in the input currents. In [14] an ac current total harmonic distortion (THD) of 12 % is reported, which is typically not acceptable for a PFC rectifier.

Several switching patterns for a similar buck-type rectifier that uses a diode rectifier and an additional output inductor on the secondary side are analyzed in [23]. The proposed ideal switching pattern is also selected for the IMDAB3R's primary side, but different duty cycle values are required, due to the additional degrees of freedom introduced by the secondary-side switches.

In this paper, a zero voltage / zero current switching modulation scheme achieving purely sinusoidal mains currents is analyzed in Section II, and conduction loss optimal switching times are derived. Based on this, the design procedure of an ultra-efficient 8 kW prototype rectifier and the DMC's commutation patterns are described in Section III. Measurement results are presented in Section IV, and finally a summary of the main findings and conclusions is given in Section V.

II. MODULATION

In order to derive a modulation scheme for the IMDAB3R, its basic circuit topology [cf. Fig. 1(b)] is simplified by replacing the DMC MOSFETs with two one-of-three selector switches $\mathrm{S_g}$ and $\mathrm{S_h}$ that connect nodes g and h to one of the three input terminals a, b, and c. The input filter is omitted, resulting in the circuit shown in Fig. 2(a). For the calculation of the resulting primary-side transformer current i_{p}, the circuit is simplified further by replacing the mains voltages, $\mathrm{S_g}$ and $\mathrm{S_h}$, with an equivalent voltage source u_{p}, and the output voltage u_{pn}, the secondary-side full-bridge and the turns ratio are replaced with the voltage source $u'_{\mathrm{s}} = u_{\mathrm{s}} n_{\mathrm{p}}/n_{\mathrm{s}}$ as shown in Fig. 2(b). Without loss of generality, only the first mains voltage sector with $0° \leq \omega t < 30°$ [$u_{\mathrm{a}} > 0 > u_{\mathrm{b}} \geq u_{\mathrm{c}}$, cf. Fig. 2(c)] is analyzed. The obtained results can be generalized to the remaining 11 sectors using common symmetry considerations.

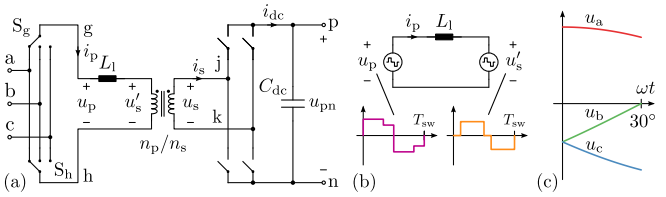

Fig. 2. (a) Simplified schematic of the IMDAB3R where the DMC MOSFETs are replaced by two one-of-three selector switches, $\mathrm{S_g}$ and $\mathrm{S_h}$, and the input filter is omitted. In (b) the DAB-like converter model, used for the derivation of a modulation scheme achieving PFC, is shown. The input and output switches are replaced by equivalent voltage sources u_{p} and u'_{s}, referred to the transformer's primary-side. Only mains voltages in sector 1, as shown in (c), are considered in the derivation.

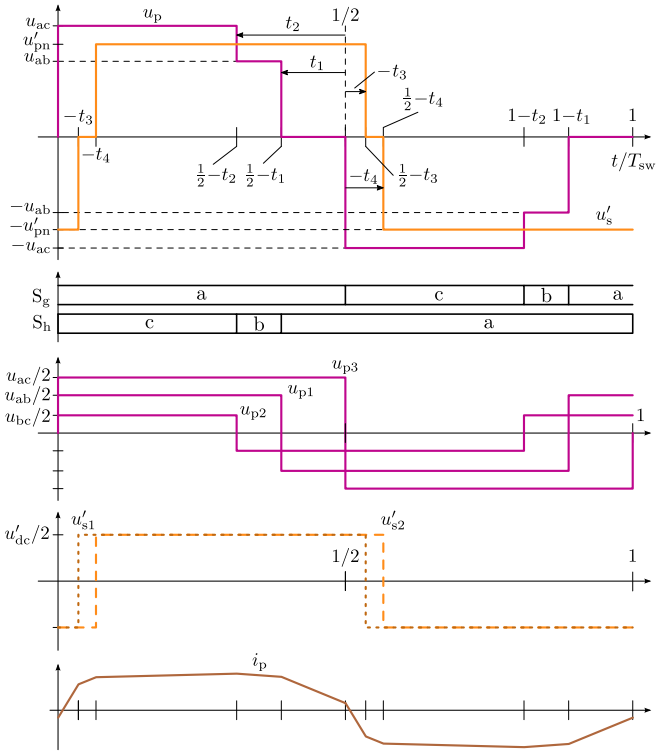

Fig. 3. Drawing (not to scale) of the primary (u_{p}) and secondary-side (u'_{s}) transformer voltages and the resulting primary-side current i_{p} for a mains voltage in sector one, i.e. $u_{\mathrm{a}} > 0 \geq u_{\mathrm{b}} \geq u_{\mathrm{c}}$. To achieve ZVS a staircase shaped voltage u_{p} is created by first selecting the mains line-to-line voltage with largest absolute value (u_{ac}) until $t = 0.5 - t_2$, followed by the line-to-line voltage with the second largest absolute value (u_{ab}) until $t = 0.5 - t_1$ and finally 0 V until $t = 0.5$ [23]. The same shape, but with inverted polarity, is used for the negative half wave $0.5 < t \leq 1$. This voltage u_{p} can be modeled as sum of three, 50 % duty cycle square-waves u_{p1}, u_{p2} and u_{p3}, with amplitudes of half the ac line-to-line voltages. The secondary-side voltage u_{s} is split into two 50 % duty cycle signals u'_{s1} and u'_{s2}. All times are normalized to the switching period T_{sw} and all secondary-side voltages are shown with respect to the primary-side, i.e. multiplied by the turns ratio $n_{\mathrm{p}}/n_{\mathrm{s}}$.

A. ZVS/ZCS Switching Pattern

A comprehensive analysis and comparison of different switching patterns for the primary-side voltage u_{p} can be found in [23]. The authors conclude that the pattern shown in Fig. 3 (called *Type-A* in [23]) is ideal, as it allows to achieve zero voltage switching (ZVS) for a sufficiently high output power.

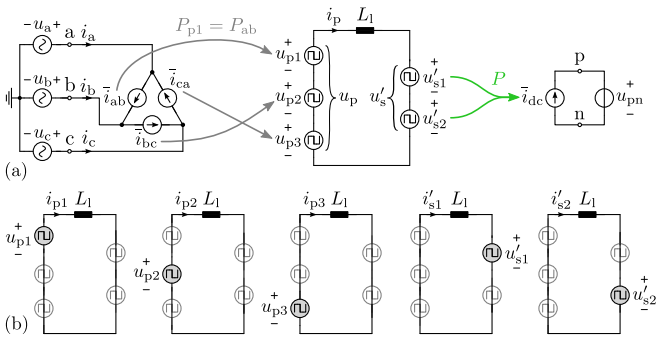

Fig. 4. (a) Equivalent circuit model where losses, voltage ripples and the magnetizing inductance are neglected, and all quantities are referred to the primary-side. The winding voltage u_p is split into a sum of three voltages $u_{\mathrm{p}1}$, $u_{\mathrm{p}2}$ and $u_{\mathrm{p}3}$ (cf. Fig. 3), which correspond to the instantaneous powers drawn from the three mains line-to-line voltages. This allows to calculate the local average values of the equivalent Δ-connection mains input currents, i.e. $\bar{i}_{\mathrm{ab}}$, $\bar{i}_{\mathrm{bc}}$ and $\bar{i}_{\mathrm{ca}}$. Likewise u'_s is split into $u'_{\mathrm{s}1}$ and $u'_{\mathrm{s}2}$, and the power received by these sources equals the power delivered to the output by the equivalent current source i_{dc} within a switching cycle. (b) The superposition principle is used to calculate i_p as sum of five components driven by the primary and secondary-side voltage sources.

For ZVS to occur, all rising edges of u_p must occur when i_p is negative an vice versa and all rising edges of u_s must occur while i_p is positive. As a positive u_p generally results in an increasing current i_p, a staircase type pattern is used for u_p, where the mains line-to-line voltage with the highest absolute value (u_{ac} in sector 1) is selected for u_p at the beginning of the switching frequency period, when i_p is still $< 0\,\mathrm{A}$ due to the last period. Next, the line-to-line voltage with the second largest absolute value (u_{ab}) is selected and finally zero volts are applied to the primary-side winding. Both transitions cause falling edges of u_p at positive i_p, which enables ZVS. At the beginning of the second half of every switching frequency cycle, u_p is switched to $-u_{\mathrm{ac}}$ and the same waveform as before, but with inverted polarity of u_p, u_s and i_p, is created. This ensures that no dc voltage is applied to the transformer's primary-side winding. With the time t normalized to the period $T_{\mathrm{sw}} = 1/f_{\mathrm{sw}}$ of one switching cycle, u_p is defined as:

$$u_\mathrm{p}(t) = \begin{cases} u_{\mathrm{ac}} & \text{if } 0 \le t < \frac{1}{2} - t_2 \\ u_{\mathrm{ab}} & \text{if } \frac{1}{2} - t_2 \le t < \frac{1}{2} - t_1 \\ 0 & \text{if } \frac{1}{2} - t_1 \le t < \frac{1}{2} \\ -u_\mathrm{p}\left(t - \frac{1}{2}\right) & \text{if } \frac{1}{2} \le t < 1 \end{cases} , \tag{1}$$

where t_1 and t_2 must fulfill:

$$0 \le t_1 \le t_2 \le \frac{1}{2} \quad . \tag{2}$$

A pulse width modulated square-wave ac voltage with variable duty cycle and phase shift is used for the secondary-side voltage u'_s, where the switching times of the leading edges are determined by t_3 and the lagging ones by t_4 as shown in Fig. 3. Like in a conventional DAB converter, u_p leads u'_s for a power transfer from the ac mains to the dc side.

B. Calculation of Input and Output Currents

In the following derivation switching frequency voltage ripples, conduction losses and the transformer's magnetizing inductance are neglected. To calculate the transformer current

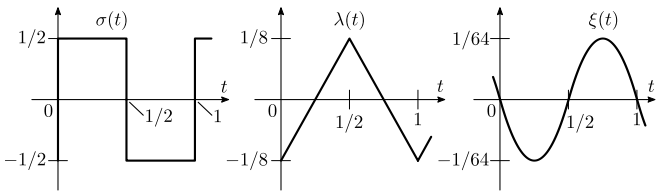

Fig. 5. Drawing of the auxiliary functions $\sigma(t)$, $\lambda(t)$ and $\xi(t)$ used in the derivation of mains and output current equations. Note that $\xi(t)$ is not sinusoidal, but consists of two quadratic functions.

i_p and the resulting mains currents $i_{\mathrm{a,b,c}}$, the primary-side voltage u_p is split into a sum of three $50\,\%$ duty cycle square-wave voltages $u_{\mathrm{p}1}$, $u_{\mathrm{p}2}$ and $u_{\mathrm{p}3}$ as shown in Fig. 4(a). The amplitude of $u_{\mathrm{p}3}$ equals half of the mains line-to-line voltage with the highest absolute value (u_{ac}), the one of $u_{\mathrm{p}2}$ is defined by the line-to-line voltage with lowest absolute value (u_{bc}) and the remaining line-to-line voltage (u_{ab}) determines the amplitude of $u_{\mathrm{p}1}$. This can be written as

$$u_{\mathrm{p}1}(t) = u_{\mathrm{ab}}\,\sigma(t + t_1) \quad , \tag{3}$$
$$u_{\mathrm{p}2}(t) = u_{\mathrm{bc}}\,\sigma(t + t_2) \quad \text{and} \tag{4}$$
$$u_{\mathrm{p}3}(t) = u_{\mathrm{ac}}\,\sigma(t) \quad \text{with} \tag{5}$$
$$\sigma(t) = \begin{cases} \frac{1}{2} & \text{if } 0 < (t \bmod 1) \le \frac{1}{2} \\ -\frac{1}{2} & \text{if } \frac{1}{2} < (t \bmod 1) \le 1 \end{cases} . \tag{6}$$

Considering, for example, the interval $0 < t < 1/2 - t_2$ the three voltages $u_{\mathrm{p}1}$, $u_{\mathrm{p}2}$ and $u_{\mathrm{p}3}$ are all positive, resulting in:

$$u_\mathrm{p} = \underbrace{\frac{u_{\mathrm{ac}}}{2}}_{u_{\mathrm{p}3}} + \underbrace{\frac{u_{\mathrm{ab}}}{2}}_{u_{\mathrm{p}1}} + \underbrace{\frac{u_{\mathrm{bc}}}{2}}_{u_{\mathrm{p}2}} = \frac{u_{\mathrm{ac}}}{2} + \frac{u_{\mathrm{ac}}}{2} = u_{\mathrm{ac}} \quad , \tag{7}$$

which matches (1). In the same way u'_s is split into two square-waves given by

$$u'_{\mathrm{s}1}(t) = u_{\mathrm{pn}}\,(n_\mathrm{p}/n_\mathrm{s})\,\sigma(t + t_3) \quad \text{and} \tag{8}$$
$$u'_{\mathrm{s}2}(t) = \underbrace{u_{\mathrm{pn}}\,(n_\mathrm{p}/n_\mathrm{s})}_{u'_{\mathrm{pn}}}\,\sigma(t + t_4) \quad . \tag{9}$$

As $u_{\mathrm{p}1}$ is the only voltage which depends on the mains voltage u_{ab}, the power $P_{\mathrm{p}1}$ delivered by $u_{\mathrm{p}1}$ can be used to calculate the average of the Δ-connected mains input current i_{ab} over one switching frequency period T_{sw} [cf. Fig. 4(a)]:

$$\bar{i}_{\mathrm{ab}} = \frac{P_{\mathrm{ab}}}{u_{\mathrm{ab}}} = \frac{P_{\mathrm{p}1}}{u_{\mathrm{ab}}} = \frac{1}{u_{\mathrm{ab}}} \int_0^1 u_{\mathrm{p}1}(t) i_\mathrm{p}(t)\,dt \quad . \tag{10}$$

In this paper a bar above a symbol, as in $\bar{i}_{\mathrm{ab}}$, is used to indicate the local average over one switching frequency period. Note that an alternative, more detailed, derivation of $\bar{i}_{\mathrm{ab}}$ is described in Appendix A.

The required transformer current $i_\mathrm{p}(t)$ can be found using superposition (cf. Fig. 4(b)):

$$i_\mathrm{p}(t) = \underbrace{\frac{u_{\mathrm{ab}}}{f_{\mathrm{sw}} L_\mathrm{l}} \lambda(t + t_1)}_{i_{\mathrm{p}1}(t)} + \underbrace{\frac{u_{\mathrm{bc}}}{f_{\mathrm{sw}} L_\mathrm{l}} \lambda(t + t_2)}_{i_{\mathrm{p}2}(t)} + \underbrace{\frac{u_{\mathrm{ac}}}{f_{\mathrm{sw}} L_\mathrm{l}} \lambda(t)}_{i_{\mathrm{p}3}(t)} + \underbrace{\frac{-u'_{\mathrm{pn}}}{f_{\mathrm{sw}} L_\mathrm{l}} \lambda(t + t_3)}_{i'_{\mathrm{s}1}(t)} + \underbrace{\frac{-u'_{\mathrm{pn}}}{f_{\mathrm{sw}} L_\mathrm{l}} \lambda(t + t_4)}_{i'_{\mathrm{s}2}(t)} \quad , \tag{11}$$

where each of the five individual current components has a triangular shape with 50 % duty cycle, as shown in Fig. 5 and given by:

$$\lambda(t) = \int_0^t \sigma(\tau)\, d\tau - \frac{1}{8} = \frac{1}{8}\begin{cases} -1+4t & \text{if } 0 < t \le 1/2 \\ 3-4t & \text{if } 1/2 < t \le 1 \end{cases} . \quad (12)$$

To solve the integral in (10), (12) can be integrated, resulting in the periodic function $\xi(t)$ shown in Fig. 5:

$$\xi(t) = \int_0^t \lambda(\tau)\, d\tau = \frac{1}{8}\begin{cases} -t+2t^2 & \text{if } 0 < t \le 1/2 \\ -1+3t-2t^2 & \text{if } 1/2 < t \le 1 \end{cases} = \frac{1}{8}\left[(t \bmod 1) - \frac{1}{2}\right]\left[1 - 2|(t \bmod 1) - \frac{1}{2}|\right] , \quad (13)$$

This allows to calculate the average of i_{ab} over one switching frequency period as:

$$\bar{i}_{\mathrm{ab}} = \frac{-2}{f_{\mathrm{sw}} L_{\mathrm{l}}} [u_{\mathrm{bc}}\, \xi(t_2 - t_1) + u_{\mathrm{ac}}\, \xi(0 - t_1) - u'_{\mathrm{pn}}\, \xi(t_3 - t_1) - u'_{\mathrm{pn}}\, \xi(t_4 - t_1)\ ] . \quad (14)$$

In almost the same manner, the remaining two average mains currents and the dc side output current can be derived as:

$$\bar{i}_{\mathrm{bc}} = \frac{-2}{f_{\mathrm{sw}} L_{\mathrm{l}}} [u_{\mathrm{ab}}\, \xi(t_1 - t_2) + u_{\mathrm{ac}}\, \xi(0 - t_2) - u'_{\mathrm{pn}}\, \xi(t_3 - t_2) - u'_{\mathrm{pn}}\, \xi(t_4 - t_2)\ ] , \quad (15)$$

$$\bar{i}_{\mathrm{ca}} = \frac{2}{f_{\mathrm{sw}} L_{\mathrm{l}}} [u_{\mathrm{ab}}\, \xi(t_1 - 0) + u_{\mathrm{bc}}\, \xi(t_2 - 0) - u'_{\mathrm{pn}}\, \xi(t_3 - 0) - u'_{\mathrm{pn}}\, \xi(t_4 - 0)\ ] \text{ and} \quad (16)$$

$$\bar{i}_{\mathrm{dc}} = \frac{-2}{f_{\mathrm{sw}} L_{\mathrm{l}}} \frac{n_{\mathrm{p}}}{n_{\mathrm{s}}} [u_{\mathrm{ab}}\, \xi(t_1 - t_3) + u_{\mathrm{ab}}\, \xi(t_1 - t_4) + u_{\mathrm{bc}}\, \xi(t_2 - t_3) + u_{\mathrm{bc}}\, \xi(t_2 - t_4) + u_{\mathrm{ac}}\, \xi(0 - t_3) + u_{\mathrm{ac}}\, \xi(0 - t_4)\ ] . \quad (17)$$

Using (14) to (16) the resulting input currents for given voltages and switching times $\vec{t} = [t_1, t_2, t_3, t_4]$ can be calculated, which allows to calculate the resulting instantaneous reactive power Q [24, 25] as:

$$Q = \frac{-1}{\sqrt{3}} \left(u_{\mathrm{a}} i_{\mathrm{bc}} + u_{\mathrm{b}} i_{\mathrm{ca}} + u_{\mathrm{c}} i_{\mathrm{ab}}\right) . \quad (18)$$

In the ideal case, a PFC rectifier creates sinusoidal input currents, in phase with the mains voltages, which implies that no reactive power is created. Setting $Q = 0$ renders (18) an equality constraint that has to be fulfilled by the switching times $\vec{t}$.

C. Conduction Loss Optimal PFC Modulation

It can be seen in the rectifier's schematic shown in Fig. 1(b), that the transformer's primary winding current i_{p} is conducted by four DMC MOSFETs, irrespective of the DMC's conduction state. Similarly, two MOSFETs of the full-bridge conduct the secondary-side transformer current $i_{\mathrm{s}} \approx i_{\mathrm{p}} n_{\mathrm{p}}/n_{\mathrm{s}}$. Neglecting high-frequency effects such as skin and proximity losses, the semiconductor conduction and transformer winding losses are proportional to the square of the rms transformer current $I_{\mathrm{p,rms}}$. In the following a modulation scheme is derived which achieves sinusoidal input currents, in phase with the mains voltage, with minimal $I_{\mathrm{p,rms}}$.

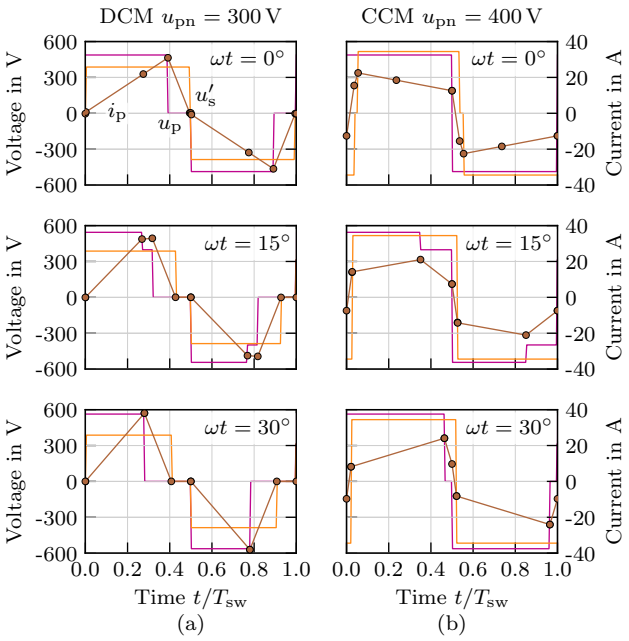

Fig. 6. Ideal transformer voltages and transformer current for $\bar{i}_{\mathrm{dc}} = 20\,\mathrm{A}$ and different mains voltage phase angles ωt. In (a) $u_{\mathrm{pn}} = 300\,\mathrm{V}$ is selected, which leads to Discontinuous Conduction Mode (DCM) were an interval with $i_{\mathrm{p}} = 0$ exists for $\omega t = 15°$ and $\omega t = 30°$. Note that u_{pn} is selected such that the plot for $\omega t = 0°$ shows the boundary case between DCM and Continuous Conduction Mode (CCM). (b) Waveforms for nominal operating conditions as given in Table I, where the rectifier operates in CCM for all values of ωt.

The IMDAB3R's structure and its equivalent circuit [cf. Fig. 2(b)] are similar to a conventional DAB dc-dc converter for which analytic expressions of the conduction loss optimal switching times can be derived as described in [26]. Considering the special case $\omega t = 30°$, the mains line-to-neutral voltage u_{b} is zero [cf. Fig. 2(c)] and hence the rectifier must ensure $i_{\mathrm{b}} = 0$. This implies that line b is not selected by the DMC, resulting in $t_1 = t_2$. Therefore, u_{ac} is the only mains line-to-line voltage used by the DMC to create u_{p} and the rectifier operates like a conventional DAB dc-dc converter. Hence, the optimal switching times derived in [26] are also optimal for the IMDAB3R in this case. Corresponding waveforms for two different output voltages are shown in the bottom row of Fig. 6.

1) Discontinuous Conduction Mode: For low output currents i_{dc} and dc voltages u_{pn} higher or lower than the nominal value, these optimal switching times for $\omega t = 30°$ result in a Discontinuous Conduction Mode (DCM) solution, where i_{p} is zero at the end of each half period at $t = 0$ and $t = 1/2$ as shown in Fig. 6(a). Due to the similarity between the IMDAB3R and the conventional DAB dc-dc converter, it can be assumed that DCM yields the conduction loss optimal switching times for other mains phase angles ωt as well, for output currents i_{dc} below the threshold $i_{\mathrm{dc,DCM,max}}$. For the sake of clarity, DCM switching times are written as $t_{k\mathrm{D}}$ $k \in \{1, 2, 3, 4\}$ in the following.

DCM is characterized by aligned rising or falling edges of

u_p and u'_s and a volt-second balance between primary and secondary-side

$$u_\mathrm{ab}\left(\frac{1}{2}-t_\mathrm{1D}\right)+u_\mathrm{bc}\left(\frac{1}{2}-t_\mathrm{2D}\right)=u'_\mathrm{pn}\left(\frac{1}{2}-t_\mathrm{3D}-t_\mathrm{4D}\right), \tag{19}$$

which leads to $i_\mathrm{p}(t)=0$ at $t=0$ and $t=0.5$. Note that this results in zero current switching (ZCS). For output currents i_dc lower than $\bar{i}_\mathrm{dc,DCM,max}$ an interval with i_p identical to zero can be inserted before $t=0.5$ and $t=1$ as shown in Fig. 6(a) for mains voltage phase angles $\omega t=15°$ and $\omega t=30°$. The calculation of $\bar{i}_\mathrm{dc,DCM,max}$ is described in the following. Numerical results are plotted in Fig. 8 as function of ωt and the dc output voltage u_pn.

Depending on u_pn, either the rising or falling edges of u_p and u'_s have to be aligned in DCM, as shown in Fig. 7(a) to (c). The boundary voltage $u'_\mathrm{pn,b}$, for which rising and falling edges are aligned, can be calculated by setting $Q=0$ to achieve PFC operation and selecting $t_\mathrm{1D}=t_\mathrm{3D}$ and $t_\mathrm{4D}=0$ to align rising and falling edges. Using (18) and (19) an analytic expression for $u'_\mathrm{pn,b}$ can be derived as:

$$u'_\mathrm{pn,b}=2\,\frac{u_\mathrm{ab}^2+u_\mathrm{ab}u_\mathrm{bc}+u_\mathrm{bc}^2}{2u_\mathrm{ab}+u_\mathrm{bc}}\quad. \tag{20}$$

A plot of $u'_\mathrm{pn,b}$ as function of ωt is shown in Fig. 7(d) for nominal mains voltage $U_1=230\,\mathrm{V}$ rms.

To calculate the maximum output current achievable in DCM ($\bar{i}_\mathrm{dc,DCM,max}$) for low output voltage ($u'_\mathrm{pn}\le u'_\mathrm{pn,b}$), the duty cycle of u'_s is maximized and the rising edges of the transformer voltages are aligned by selecting $t_\mathrm{3D}=t_\mathrm{4D}=0$. Equations (18) and (19) can then be solved by a computer algebra system for the required primary-side switching time t_1D to achieve $Q=0$:

$$e_1=u_\mathrm{ab}^2+u_\mathrm{ab}u_\mathrm{bc}+u_\mathrm{bc}^2 \tag{21}$$
$$e_2=u_\mathrm{ab}+u_\mathrm{bc}-u'_\mathrm{pn} \tag{22}$$
$$e_3=e_2\left(u_\mathrm{ab}+2u_\mathrm{bc}\right)\left(2e_1-u'_\mathrm{pn}\left(2u_\mathrm{ab}+u_\mathrm{bc}\right)\right) \tag{23}$$
$$e_4=u'_\mathrm{pn}\left(2u_\mathrm{ab}^2+3u_\mathrm{ab}u_\mathrm{bc}+2u_\mathrm{bc}^2\right) \tag{24}$$
$$t_\mathrm{1D}=\frac{u_\mathrm{ab}e_2\left(2e_1-(2u_\mathrm{ab}+u_\mathrm{bc})u'_\mathrm{pn}\right)+u_\mathrm{bc}u'_\mathrm{pn}\sqrt{e_3}}{4u_\mathrm{ab}(u_\mathrm{ab}+u_\mathrm{bc})e_1-2(u_\mathrm{ab}-u_\mathrm{bc})e_4}\,, \tag{25}$$

where terms e_1 to e_4 are intermediate values without a physical interpretation. Finally, the remaining DCM switching time t_2D can be calculated as

$$t_\mathrm{2D}=\frac{1}{2}-\begin{cases}\frac{1}{\sqrt{2}}\left(\frac{1}{2}-t_\mathrm{1D}\right) & \text{if } u_\mathrm{bc}=0\\ \left(\frac{u'_\mathrm{pn}}{2}-u_\mathrm{ab}\left(\frac{1}{2}-t_\mathrm{1D}\right)\right)\frac{1}{u_\mathrm{bc}} & \text{if } u_\mathrm{bc}>0\end{cases}, \tag{26}$$

which allows to evaluate (17) to find $\bar{i}_\mathrm{dc,DCM,max}$. Example waveforms for $u_\mathrm{ab}=398\,\mathrm{V}$, $u_\mathrm{bc}=146\,\mathrm{V}$ ($\omega t=15°$) and $u'_\mathrm{pn}=300\,\mathrm{V}$ are shown in Fig. 7(a).

Note that in the special case $u_\mathrm{pn}=0$ the equation above result in $t_\mathrm{1D}=t_\mathrm{2D}={}^1\!/_2$, which results in $\bar{i}_\mathrm{dc,DCM,max}=0$. Nevertheless, conduction loss optimal switching times can be found in this case as described in Appendix B.

For $u'_\mathrm{pn}\ge u'_\mathrm{pn,b}$ the primary voltage's duty cycle is maximized by selecting $t_\mathrm{1D}=0$ and the falling edges of the transformer voltages are aligned by selecting $t_\mathrm{3D}=0$. Again

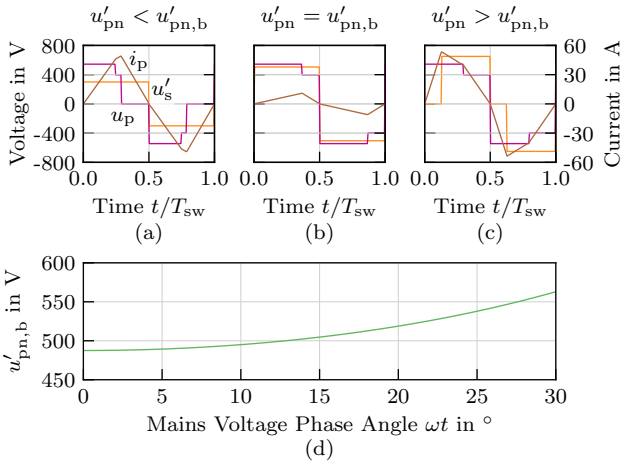

Fig. 7. Transformer voltages and transformer current for $\omega t=15°$, operating with maximum output current $i_\mathrm{dc,DCM,max}$ possible in DCM. In (a) the output voltage $u'_\mathrm{pn}=300\,\mathrm{V}$ is lower than the boundary value $u'_\mathrm{pn,b}=505\,\mathrm{V}$ and therefore the duty cycle of u'_s is maximal and the rising edges of u_p and u'_s are aligned. (b) Shows the case $u'_\mathrm{pn}=u'_\mathrm{pn,b}$, where both u_p and u'_s use the maximum possible duty cycle. (c) For $u'_\mathrm{pn}=650\,\mathrm{V}>u'_\mathrm{pn,b}$ only the duty cycle of u_p is maximal and the falling edges are aligned. In (d) $u'_\mathrm{pn,b}$ is plotted as a function of the mains voltage phase angle ωt for nominal input voltage $U_1=230\,\mathrm{V}$ rms line-to-neutral.

(18) and (19) can be used to find analytic expression of the switching times t_2D and t_4D for DCM with high output voltage as:

$$e_5=u'_\mathrm{pn}\left(2u_\mathrm{ab}+u_\mathrm{bc}\right)\quad, \tag{27}$$
$$e_6=u'_\mathrm{pn}\left(u_\mathrm{ab}^2-u_\mathrm{bc}^2\right)\left(u_\mathrm{ab}-u'_\mathrm{pn}\right)\left(2e_1-e_5\right)\quad, \tag{28}$$
$$t_\mathrm{2D}=\frac{1}{2}\,\frac{u_\mathrm{bc}^3-u_\mathrm{ab}^2u_\mathrm{bc}-\sqrt{e_6}}{u_\mathrm{bc}^2(u_\mathrm{bc}-u_\mathrm{ab})+(2u_\mathrm{ab}^2+u_\mathrm{bc}^2-e_5)u'_\mathrm{pn}}\,, \tag{29}$$
$$t_\mathrm{4D}=\frac{u_\mathrm{ab}}{2u'_\mathrm{pn}}+\frac{u_\mathrm{bc}}{u'_\mathrm{pn}}\left(\frac{1}{2}-t_\mathrm{2D}\right)-\frac{1}{2}\quad. \tag{30}$$

This defines the four switching times for DCM operation with maximum output current for high u'_pn and (17) can be evaluated to calculate $\bar{i}_\mathrm{dc,DCM,max}$ in this case. An example waveform for this case is shown in Fig. 7(c). Note that in the corner case $u'_\mathrm{pn}=u'_\mathrm{pn,b}$ the solutions obtained for low and high output voltages coincide, yielding the waveform shown in Fig. 7(b).

In Fig. 8 $\bar{i}_\mathrm{dc,DCM,max}$ is plotted as function of the input output voltage ratio $u'_\mathrm{pn}/\hat{U}_1$ and the mains voltage phase angle ωt. To create a generic plot that is applicable to any converter, $\bar{i}_\mathrm{dc,DCM,max}$ is referenced to the primary-side and normalized by multiplying with $f_\mathrm{sw}L_1/\hat{U}_1$. Additionally, the boundary voltage $u'_\mathrm{pn,b}(\omega t)$ is plotted, normalized to $\hat{U}_1$. It can be seen that only relatively low output currents can be achieved in DCM for low values of u'_pn and if u'_pn is close to $u'_\mathrm{pn,b}$, which is also the case in a conventional DAB dc-dc converter [26].

The solutions obtained above yield the switching times for the maximum dc output current in DCM. If a current i^*_dc lower than $i_\mathrm{dc,DCM,max}$ has to be created an interval with $i_\mathrm{p}=0$ can be inserted before the end of each half-cycle by rescaling the

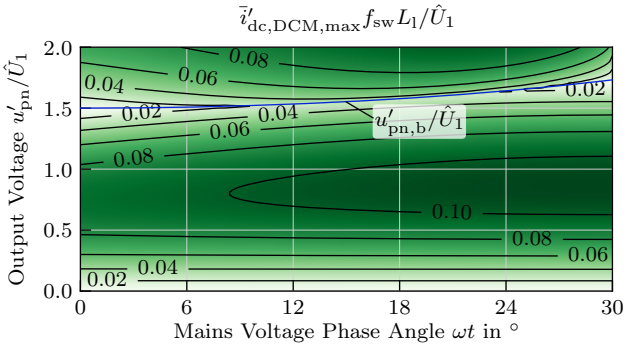

Fig. 8. Contour plot of the maximal output current $\bar{i}'_{\mathrm{dc,DCM,max}}$ achievable in DCM, referenced to the primary-side and normalized by multiplication with $f_{\mathrm{sw}} L_{\mathrm{l}}/\hat{U}_1$, as function of the mains voltage phase angle ωt and the normalized dc voltage (w.r.t. to the primary-side) $u'_{\mathrm{pn}}/\hat{U}_1$. Also shown is the boundary voltage $u'_{\mathrm{pn,b}}$, normalized to $\hat{U}_1$, as function of ωt.

switching times as:

$$t_k(i^*_{\mathrm{dc}}) = \frac{1}{2} - \left(\frac{1}{2} - t_{k\mathrm{D}}\right)\sqrt{\frac{i^*_{\mathrm{dc}}}{\bar{i}_{\mathrm{dc,DCM,max}}}} \quad k \in \{1,2,3\}\,, \tag{31}$$

$$t_4(i^*_{\mathrm{dc}}) = t_{4\mathrm{D}}\sqrt{\frac{i^*_{\mathrm{dc}}}{\bar{i}_{\mathrm{dc,DCM,max}}}} \quad . \tag{32}$$

Note that the switching times are not proportional to i^*_{dc} but to its square root. This is because introducing an interval with $i_{\mathrm{p}} = 0$ reduces the time during which power is transferred between primary and secondary and simultaneously reduces the amplitude of i_{p}.

2) Continuous Conduction Mode: Output currents i^*_{dc} larger than $\bar{i}_{\mathrm{dc,DCM,max}}$ cannot be achieved with DCM, but by Continuous Conduction Mode (CCM). This implies that (19), the volt-second balance between u_{p} and u'_{s}, no longer holds within a switching half cycle . With the output current reference value i^*_{dc} two equality constraints are defined

$$\bar{i}_{\mathrm{dc}}\left(u_{\mathrm{ab}}, u_{\mathrm{bc}}, u_{\mathrm{pn}}, \vec{t}\right) = i^*_{\mathrm{dc}} \quad , \tag{33}$$

$$Q\left(u_{\mathrm{ab}}, u_{\mathrm{bc}}, u_{\mathrm{pn}}, \vec{t}\right) = 0 \quad , \tag{34}$$

for four unknown switching times $\vec{t}$. Like in the conventional DAB dc-dc converter, the additional degrees of freedom offered by the modulation can be used to select a solution which achieves minimal conduction losses by minimizing the squared rms value of transformer current $I^2_{\mathrm{p,rms}}$. This value can be found by calculating the complex valued Fourier series coefficients c_k of i_{p} defined in (11):

$$c_k = \frac{-1}{2\pi^2 k^2 f_{\mathrm{sw}} L_{\mathrm{l}}}\left[u_{\mathrm{ab}}\, e^{j2\pi k t_1} + u_{\mathrm{bc}}\, e^{j2\pi k t_2} + u_{\mathrm{ac}}\, e^{0} - u'_{\mathrm{pn}}\left(e^{j2\pi k t_3} + e^{j2\pi k t_4}\right)\right] \quad , \tag{35}$$

for odd values of k. An approximation of $I^2_{\mathrm{p,rms}}$ can then be found by summing the first M odd harmonics:

$$I^2_{\mathrm{p,rms}} \approx 2\sum_{m=1}^{M} c_{2m-1}\, c^*_{2m-1} \quad . \tag{36}$$

Choosing M between 10 and 100 typically leads to sufficiently precise results. While it might be possible to minimize $I^2_{\mathrm{p,rms}}$ using analytical methods, no closed form solution could be obtained. Instead, numerical optimization algorithms such as Sequential Quadratic Programming (SQP) can be used to find switching times $\vec{t}$ that minimize (36) subject to the equality constraints (33) and (34) [27]. Resulting CCM waveforms for nominal operating conditions and different mains voltage phase angles are shown in Fig. 6(b).

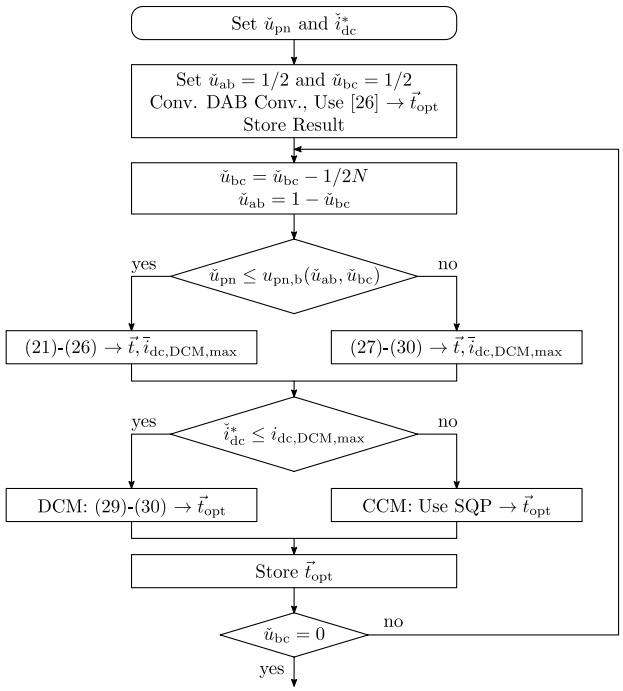

Fig. 9. Algorithm used to calculate the conduction loss optimal switching times $\vec{t}_{\mathrm{opt}}$ for given normalized dc voltage $\breve{u}'_{\mathrm{pn}}$, a normalized output current reference $\breve{i}^*_{\mathrm{dc}}$ and N values of $\breve{u}_{\mathrm{bc}}$ in the range $[0, 1/2]$. The calculation starts with $\breve{u}_{\mathrm{bc}} = 1/2$ ($\omega t = 30°$) in which case the rectifier operates like a conventional DAB dc-dc converter, using analytic equations published in [26]. For all following points DCM is used if possible ($\breve{i}^*_{\mathrm{dc}}$ less than the maximum DCM output current $\bar{i}_{\mathrm{dc,DCM,max}}$), otherwise numerical optimization (SQP) is used to obtain a CCM solution, using the previous switching times as starting point for the optimizer.

D. Normalized Lookup Table

The computing power and memory required for numerical optimization algorithms typically render them unsuitable for real-time execution in a microcontroller used to control a PFC rectifier. Instead, the optimization is performed off-line and the resulting optimal switching times $\vec{t}_{\mathrm{opt}}$ are stored in a lookup table (LUT). By using the normalization

$$\breve{u}_{\mathrm{bc}} = u_{\mathrm{bc}}\frac{1}{u_{\mathrm{ac}}} \quad , \tag{37}$$

$$\breve{u}'_{\mathrm{pn}} = u_{\mathrm{pn}}\frac{n_{\mathrm{p}}}{n_{\mathrm{s}}}\frac{1}{u_{\mathrm{ac}}} \quad , \tag{38}$$

$$\breve{i}^*_{\mathrm{dc}} = i^*_{\mathrm{dc}}\frac{n_{\mathrm{s}}}{n_{\mathrm{p}}}\frac{1}{I_{\mathrm{nom}}} \quad I_{\mathrm{nom}} = \frac{u_{\mathrm{ac}}}{f_{\mathrm{sw}} L_{\mathrm{l}}} \quad , \tag{39}$$

the LUT becomes independent of converter specifications such as nominal voltage levels, $n_{\mathrm{p}}/n_{\mathrm{s}}$, f_{sw}, L_{l}, etc. Equations (37) to (39) again refer to sector 1 of the mains voltage, where $u_{\mathrm{ac}} > u_{\mathrm{ab}} \geq u_{\mathrm{bc}} \geq 0$ holds, and therefore a division by u_{ac} is possible. Equations (37) to (39) are a complete description of

the rectifiers operating conditions, hence a three-dimensional LUT is required. In the following, a LUT with $N = 30$ sampling points per dimension is considered, resulting a total of 27000 entries, each consisting of four switching time values. As the measured voltages and the requested i^*_{dc} will typically not coincide exactly with the sampling points of the LUT trilinear interpolation is used to obtain near-optimal switching times during operation.

To improve the convergence of the numerical optimizer used in CCM, the algorithm outlined in Fig. 9 is used to calculate the LUT. For each pair of normalized dc voltage $\check{u}_{\mathrm{pn}}$ and output current $\check{i}^*_{\mathrm{dc}}$ values, $\omega t = 30°$ ($\check{u}_{\mathrm{ab}} = 1/2$ and $\check{u}_{\mathrm{bc}} = 0$) is considered first as the converter operates like a conventional DAB dc-dc converter in this case. The closed form solution published in [26] is used to calculate the conduction loss optimal switching times $\vec{t}_{\mathrm{opt}}$. In the next step, $\check{u}_{\mathrm{bc}}$ is reduced by $1/2N$ and the highest achievable output current in DCM $\bar{i}_{\mathrm{dc,DCM,max}}$ is calculated. If i^*_{dc} is less or equal to $\bar{i}_{\mathrm{dc,DCM,max}}$ the closed form solutions described in Section II-C1 are used to calculate $\vec{t}_{\mathrm{opt}}$, otherwise a numerical optimizer (SQP) is used and the switching times $\vec{t}_{\mathrm{opt}}$ obtained for the previous point are used as initial guess. The resulting $\vec{t}_{\mathrm{opt}}$ is stored and the calculation continues with the next value $\check{u}_{\mathrm{bc}}$, until $\check{u}_{\mathrm{bc}} = 0$ is reached. The proposed algorithm was implemented in Scientific Python and requires less than five minutes to calculate a complete LUT with a resolution of $N = 30$ on a standard desktop computer [28, 29]. This implementation is available online under an open source license [30].

E. Properties of the Modulation Scheme

1) Varying DC Voltage and Current: Simulation results using the calculated LUT are shown in Fig. 10 with a constant nominal dc voltage of $u_{\mathrm{pn}} = 400\,\mathrm{V}$ and a output current reference i^*_{dc} reducing linearly from 25 A to 0 A within two mains voltage periods. The nominal switching frequency of 31 kHz is used in this simulation. It can be seen that the first order low pass filtered output current $\bar{i}_{\mathrm{dc}}$ (cut-off frequency 2.7 kHz) of the secondary-side full-bridge follows the reference signal closely. Nearly sinusoidal mains currents, in phase with the mains voltages and with a linearly decreasing amplitude result. Further shown are the primary-side transformer current i_{p} (magnetizing inductance neglected) and its local rms value which also decreases almost linearly with i^*_{dc}.

In Fig. 11 similar simulation results are shown for a fixed output current reference of $i^*_{\mathrm{dc}} = 20\,\mathrm{A}$, with a dc voltage ramping down linearly from $u_{\mathrm{pn}} = 500\,\mathrm{V}$ to $u_{\mathrm{pn}} = 0\,\mathrm{V}$. Again, sinusoidal mains input currents with linearly decreasing amplitude result and the first order low-pass filtered secondary-side full-bridge output current $\bar{i}_{\mathrm{dc}}$ remains close to the set point i^*_{dc} independent of u_{pn}. Together Fig. 10 and Fig. 11 demonstrate that the proposed modulation scheme achieves sinusoidal mains input currents i_{a}, i_{b} and i_{c} for different output voltages, mains voltage phase angles and dc currents. Numerical analysis of the LUT shows that sinusoidal input currents, in phase with the mains voltage, are achieved, regardless of the input/output voltage ratio and the output current. This verifies that the modulation scheme is suitable for the implementation of a three-phase PFC rectifier.

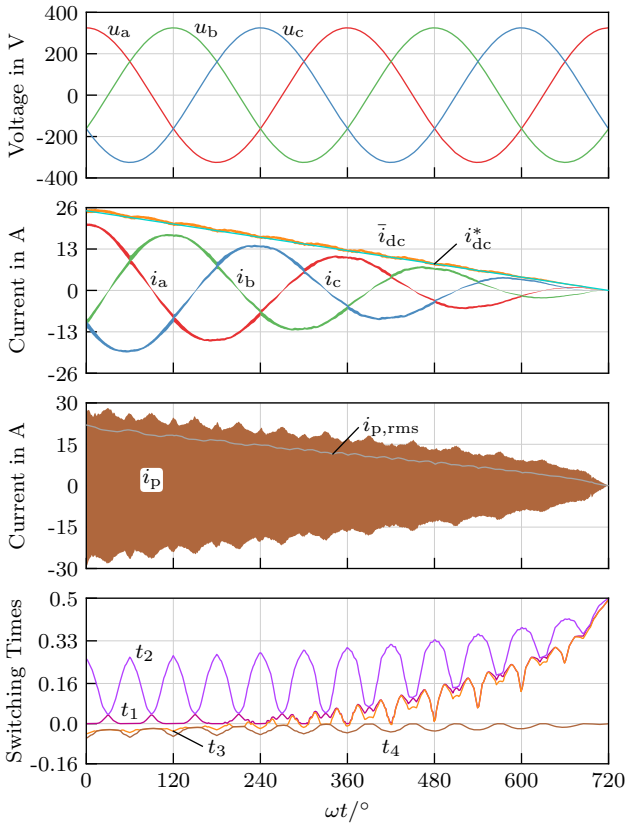

Fig. 10. Simulation results for a linearly decreasing output current reference signal i^*_{dc} with nominal ac and dc voltages. It can be seen that the actual output current i_{dc} tracks the reference closely and that sinusoidal mains currents i_{a}, i_{b} and i_{c} with a linearly decreasing amplitude result. The primary transformer current i_{p}, its local rms value (first order low pass, cut-off frequency 2.7 kHz) and the four switching times $\vec{t}$ are shown as well.

2) Transformer rms Current: It can be seen in the third plot of Fig. 11, that the peak and rms values of the transformer current i_{p} change as function of u_{pn} and the mains voltage phase angle, even though the output current i_{dc} is basically constant. Relatively low peak and rms currents result for u_{pn} values close to the nominal dc voltage of 400 V, as the transformer turns ratio given in Table I is chosen accordingly. For higher ($\approx 500\,\mathrm{V}$) and lower ($\approx 200\,\mathrm{V}$) dc voltages the converter operates in DCM, resulting in triangular current waveforms [cf. Fig. 6(a)] that cause higher rms and peak currents than the trapezoidal current waveforms used in CCM [cf. Fig. 6(b)].

Assuming purely sinusoidal mains voltages and neglecting the magnetizing current, the rms value of i_{p} over a full mains voltage period can be calculated as function of two parameters: The voltage transfer ratio $u'_{\mathrm{pn}}/\hat{U}_1$ between the dc voltage (w.r.t. to the primary) and the mains voltage amplitude $\hat{U}_1$, and the output current with respect to the primary-side $\bar{i}'_{\mathrm{dc}} = \bar{i}_{\mathrm{dc}} n_{\mathrm{s}}/n_{\mathrm{p}}$ normalized by $I_{\mathrm{norm}} = \hat{U}_1/f_{\mathrm{sw}}L_1$. The calculated normalized and denormalized values (for $\hat{U}_1 = 325\,\mathrm{V}$) are plotted in Fig. 12(a) with the nominal operating conditions marked by an orange asterisk. Additionally, Fig. 12(b) shows the ratio between the rms value of i_{p} and the output current w.r.t. the primary-side $\bar{i}'_{\mathrm{dc}}$, which describes the scaling of conduction losses in the switches and transformer windings with $\bar{i}_{\mathrm{dc}}$. For

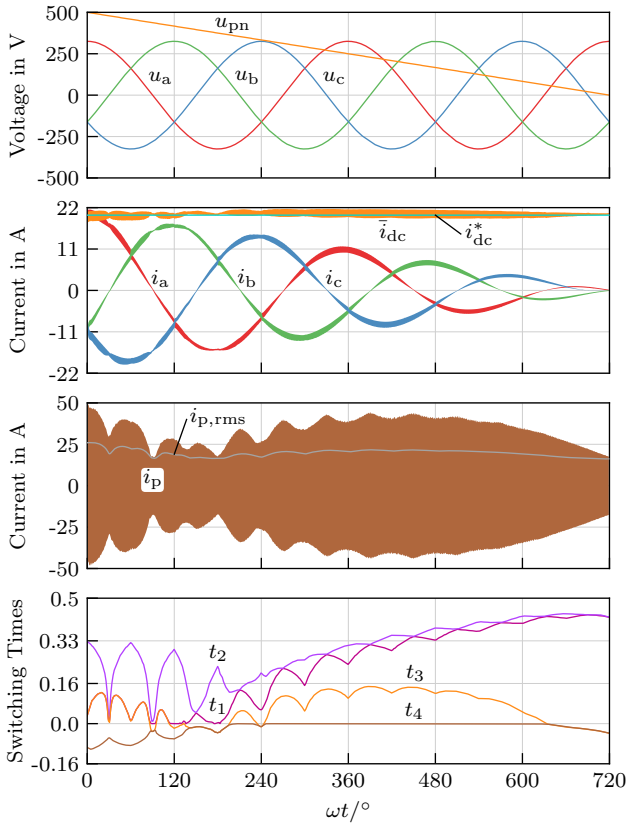

Fig. 11. Simulation results with a constant dc current reference $i^*_{\mathrm{dc}} = 20\,\mathrm{A}$ for a dc voltage which decreases linearly from $u_{\mathrm{pn}} = 500\,\mathrm{V}$ to $0\,\mathrm{V}$. The low pass filtered actual dc current $\bar{i}_{\mathrm{dc}}$ (first order, 2.7 kHz cut-off frequency) stays close to i^*_{dc} for all values of u_{pn}.

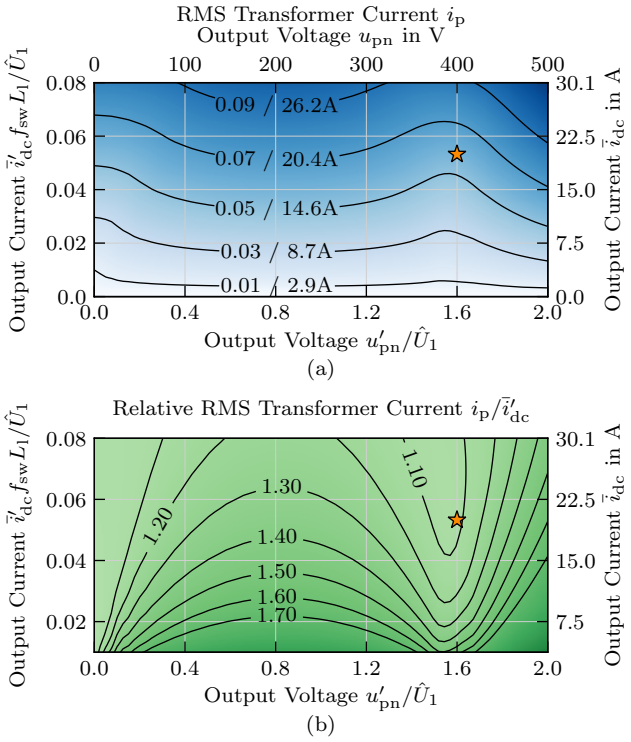

Fig. 12. (a) RMS value of the primary-side transformer current i_{p} (normalized by $f_{\mathrm{sw}} L_1/\hat{U}_1$), as function of the normalized output voltage $u'_{\mathrm{pn}}/\hat{U}_1$ and the output current $\bar{i}'_{\mathrm{dc}} = \bar{i}_{\mathrm{dc}} n_{\mathrm{s}}/n_{\mathrm{p}}$ (w.r.t. the primary-side) normalized by $f_{\mathrm{sw}} L_1/\hat{U}_1$. For reference, denormalized voltage and current values with $\hat{U}_1 = 325\,\mathrm{V}$ are shown at the top and right axes. (b) Ratio of the rms value of i_{p} to the dc current, w.r.t the primary-side, as function of u_{pn} and output current. The orange asterisks indicate nominal operating conditions (cf. Table I).

a given $\bar{i}'_{\mathrm{dc}}$, the transformer current i_{p} becomes minimal at $u_{\mathrm{pn}} = 0$, which is the trivial case as no power is transferred to the output, and for voltage transfer ratios $u'_{\mathrm{pn}}/\hat{U}_1$ in range of 1.5 to 1.6. In this case the average six-pulse rectified mains voltage is close to u'_{pn}, which implies that CCM is used through most or all phase angles ωt of the mains voltage, leading to lower rms values of i_{p} than DCM which dominates for lower and higher voltage transfer ratios (cf. Fig. 8).

3) Output Current Limit: As in a conventional DAB dc-dc converter, the maximum power that can be transferred between primary and secondary, and hence the maximum output current, is limited and depends on the input and output voltages, L_1 and f_{sw}. This is also the case for the IMDAB3R, where the maximum output current $i_{\mathrm{dc,max}}$ also depends on the mains voltage phase angle ωt. To achieve PFC operation, only output currents less or equal to the lowest value of $\bar{i}_{\mathrm{dc,max}}$ over all ωt can be used. For given $\hat{U}_1$, u_{pn} and ωt, $\bar{i}_{\mathrm{dc,max}}$ can be found by numerically maximizing (17) subject to (34), which ensures that the input currents are in phase with the mains voltages. The resulting $\bar{i}_{\mathrm{dc,max}}$, referenced to the primary-side and normalized by $f_{\mathrm{sw}} L_1/\hat{U}_1$, is plotted in Fig. 13 as function of ωt for different voltage transfer ratios $u'_{\mathrm{pn}}/\hat{U}_1$. It can be seen that $\bar{i}'_{\mathrm{dc,max}} f_{\mathrm{sw}} L_1/\hat{U}_1$ reaches the minimum of $3/16 = 0.1875$ for $\omega t = 0$, irrespective of $u'_{\mathrm{pn}}/\hat{U}_1$. This is because the largest line-to-line mains voltage (u_{ab} in sector 1) reaches its minimum of $1.5\,\hat{U}_1$ for $\omega t = 0$ [cf. Fig. 2(c)], which

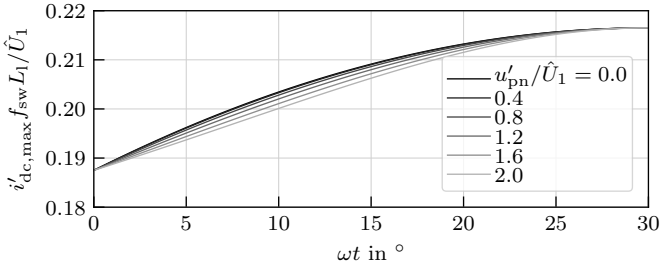

Fig. 13. Normalized maximum output current $\bar{i}'_{\mathrm{dc,max}}$ (w.r.t. primary-side) as a function of the mains voltage phase angle ωt (only sector 1 considered) for different voltage transfer ratios $u'_{\mathrm{pn}}/\hat{U}_1$ in the range $[0, 2]$. It can be seen that for all voltage transfer ratios the minimum occurs at $\omega t = 0$ and that its value ($3/16 = 0.1875$) is independent of $u'_{\mathrm{pn}}/\hat{U}_1$.

implies that the input voltage available for power transfer is minimal in this case. However, operation with output currents $\bar{i}'_{\mathrm{dc}}$ close to the limit $\bar{i}'_{\mathrm{dc,max}}$ is typically not feasible as, like in a conventional DAB converter, high phase shift angles close to 90° between primary and secondary-side result, leading to a high reactive power due to L_1 and hence to a high rms value of i_{p}.

III. Design and Implementation

Conversion losses and the required operating room temperature conditioning and/or cooling are typically significant cost factors in applications that require 24/7 operation, such as data

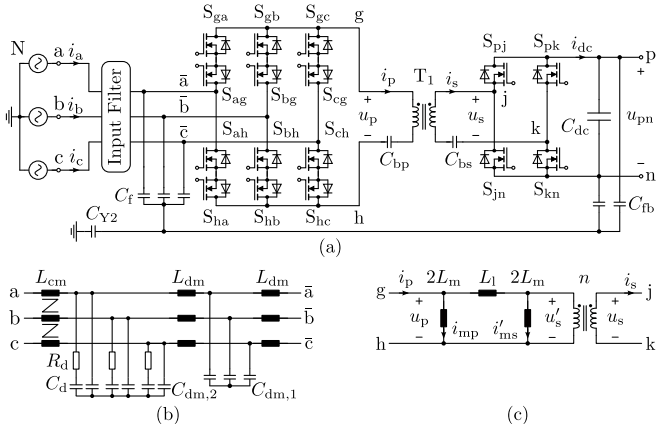

Fig. 14. (a) Schematic of the implemented IMDAB3R prototype, using 900 V, 10 mΩ SiC MOSFETs and an isolation transformer T_1 with built-in inductance L_σ. (b) shows the implemented two-stage EMI filter and (c) shows the Π-type equivalent circuit model of the transformer, with the three parameters L_σ, L_m and n. It can be used to calculate the primary and secondary-side winding currents i_p and i_s, including the magnetizing current caused by the finite magnetizing inductance L_m.

TABLE II
SELECTED COMPONENTS

DMC	*C3M0010090K* 900 V, 10 mΩ
Full-Bridge	*C3M0010090K* 900 V, 10 mΩ
C_{dc}	9× B32774D4106, 10 µF, 450 V
C_f	3× WE 890334026030CS, 1.5 µF, 310 V, X2 rated
C_{bp}	14× KTS500B156M55N0T00, 15 µF, 50 V
C_{bs}	10× KTS250B156M43N0T00, 15 µF, 25 V
T_1	see Table III
EMI Filter	see Table IV

center and telecommunication power supplies. Very efficient rectifiers are therefore highly desirable in this case [10, 11]. Accordingly, an IMDAB3R prototype is designed, striving for the highest possible efficiency at nominal operating conditions, to demonstrate the achievable performance and to serve as a benchmark for comparative evaluations of future research results.

It can be seen in Fig. 12(b) that the rms value of winding current i_p required to create a certain output current $\bar{i}_{dc}$ changes significantly with the ratio between output voltage times turns ratio nu_{pn} and the mains voltage amplitude $\hat{U}_1$. Therefore the turns ratio should be chosen such that $u'_{pn}/\hat{U}_1$ is within, or close to, the range 1.5 to 1.6 for the operating points were the highest efficiency is desired. Furthermore, it can be seen in Fig. 12(b) that higher normalized output currents $\bar{i}_{dc} f_{sw} L_\sigma/\hat{U}_1$ lead to lower rms values of i_p for a given (denormalized) output current $\bar{i}_{dc}$. This implies that the winding current's rms value decreases with increasing inductance L_σ and/or switching frequency f_{sw}. However, increasing the product $f_{sw} L_\sigma$ also reduces the maximum output current $\bar{i}_{dc,max}$.

For the sake of brevity, the performed optimizations cannot be described in full detail, and instead the main steps of the design and implementation are presented in the following.

A. Considered Design

The schematic of the IMDAB3R considered in this section is shown in Fig. 14(a) and the implemented EMI input filter is shown in Fig. 14(b). Like for conventional DAB dc-dc converters, the required inductance L_σ can either be implemented as a separate component, using its own magnetic core, or it can be built into the isolation transformer. The later is selected for the prototype, as this simplifies the mechanical design and eliminates the losses and volume resulting from wire terminations, screws or solder contacts etc.

Ideally, the modulation scheme described in the previous chapter creates winding voltages u_p and u_s that have no dc or low frequency components. However, due to nonidealities such as varying delay times, voltage ripples and/or measurement errors, low-frequency components might occur. These would lead to circulating winding currents, causing additional losses and potentially saturating the transformer. To avoid these currents, low-voltage blocking capacitors C_{bp} and C_{bs} are connected in series with the transformer windings.

Table II lists the main components selected for the IMDAB3R prototype.

B. Transformer

The transformer's parameters (L_σ, L_m and n) significantly influence the winding currents i_p and i_s, which determine the conducted currents and switched currents of all semiconductors. Hence, the transformer design and the resulting parameters must be calculated before the semiconductor losses can be obtained.

In the following, the Π-type equivalent circuit model of the transformer shown in Fig. 14(c) is used, as it allows a direct calculation of the winding currents i_p and i_s, including the magnetizing current components i_{mp} and i_{ms}. As the DMC and the full-bridge apply u_p and u_s, their complex valued Fourier coefficients can be calculated as:

$$c_{mp,k} = \frac{-1}{4\pi^2 k^2 f_{sw} L_m} \left(u_{ab}\, e^{j2\pi k t_1} + u_{bc}\, e^{j2\pi k t_2} + u_{ac}\, e^{0} \right), \tag{40}$$

$$c_{ms,k} = \frac{-n^2 u_{pn}}{4\pi^2 k^2 f_{sw} L_m} \left(e^{j2\pi k t_3} + e^{j2\pi k t_4} \right) . \tag{41}$$

Using the Fourier coefficients c_k, calculated with (35) for the simple DAB model that neglects L_m, the rms value of the k-th harmonic can be calculated as

$$I_{p,rms,k} = \sqrt{2\left(c_k + c_{mp,k}\right)\left(c_k^* + c_{mp,k}^*\right)} , \tag{42}$$

$$I_{s,rms,k} = \sqrt{2\left(nc_k - c_{ms,k}\right)\left(nc_k^* - c_{ms,k}^*\right)} , \tag{43}$$

for odd values of k. This allows to calculate the winding losses, including those resulting from skin and proximity effect, for an operating point given by u_{ab}, u_{bc}, i_{dc} and u_{pn}. The winding currents' squared rms values $I^2_{p,rms}$ and $I^2_{s,rms}$ can be approximated by summing the squares of the first M odd harmonics as:

$$I^2_{p,rms} \approx \sum_{m=1}^{M} I^2_{p,rms,2m-1} , \tag{44}$$

$$I^2_{s,rms} \approx \sum_{m=1}^{M} I^2_{s,rms,2m-1} . \tag{45}$$

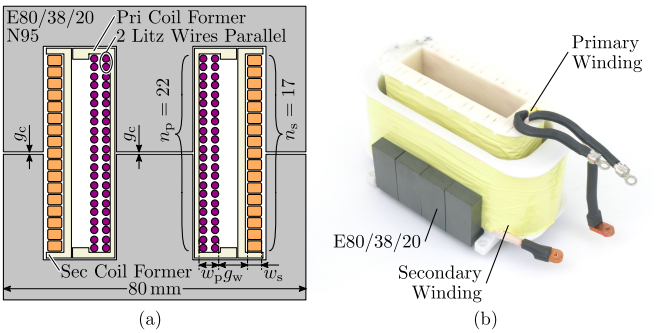

Fig. 15. (a) Scaled cross section drawing of the transformer. To implement the required leakage inductance L_l, the windings are wound on individual, 3D printed coil formers and are separated by a 7 mm wide gap g_w. (b) Picture of the implemented transformer, with the top half of the core removed and the inner, primary-side coil former lifted.

TABLE III
TRANSFORMER DESIGN

Core	EE80/38/20, Epcos TDK N95, 4 pairs stacked
Primary Winding	71 µm litz wire, 630 strands, 2 wires in parallel
Secondary Winding	100 µm litz wire, 900 strands, rectangular
Winding Widths	$w_\mathrm{p} = 7\,\mathrm{mm}$, $w_\mathrm{s} = 4\,\mathrm{mm}$
Winding Separation	$g_\mathrm{w} = 7\,\mathrm{mm}$
Air Gap	$g_\mathrm{c} = 0.3\,\mathrm{mm}$, twice in magnetic path
Turns Ratio	$n = 1.29$
Measured	$L_\mathrm{l} = 36\,\mu\mathrm{H}$, w.r.t. to primary
Measured	$L_\mathrm{m} = 1.45\,\mathrm{mH}$, w.r.t. to primary

Typically, selecting M in the range between 10 and 100 is sufficient. By averaging the resulting losses over approximately 10 points within one mains voltage sector, the transformer's winding losses for the considered values of U_1, u_pn and i_dc can be calculated.

The transformer's core losses are calculated using the improved Generalized Steinmetz Equation (iGSE) [31]. As L_l is built into the transformer as leakage inductance, the voltage drop across L_l creates a significant leakage flux results. This leads to a spatially varying flux density in the core. For each operating point, this is accounted for by evaluating the iGSE twice, once for the flux density created by u_p and once for u_s and averaging the obtained losses.

A drawing of the implemented transformer's cross section is shown in Fig. 15(a) and the chosen design parameters are given in Table III. To implement a sufficiently large leakage inductance L_l, the primary and secondary winding do not occupy the entire core window, but are separated by a gap of $g_\mathrm{w} = 7\,\mathrm{mm}$. While this reduces the available copper cross section and therefore increases the dc resistance of the windings, it also reduces the proximity effect losses, which are approximately proportional to the winding widths w_p and w_s squared [32]. The gap between primary and secondary winding is achieved by using individual coil formers and the primary-side coil former is inserted into the center part of the secondary-side coil former, as can be seen in the picture in Fig. 15(b).

As described, the rectifier's modulation scheme the rms value of i_p varies significantly with the voltage transfer ratio u'_pn/U_1. A turns ratio $n_\mathrm{p}/n_\mathrm{s}$ of 1.29 is selected, which results in $u'_\mathrm{pn}/U_1 \approx 1.6$, yielding low rms values of i_p for a given output current, as can be seen in Fig. 12(b). Due to restricted availability of litz wires and to fully utilize the core window's height, two wires with 630 strands of 71 µm are connected in parallel for the primary-side winding. To avoid circulating currents, the wires are wound in parallel and in close proximity to each other. Measurements confirm a current ratio of 1 : 2, which results in losses that are, surprisingly, only 11 % higher than in the ideal case of equal current sharing. As the wires are wound in close proximity, touching each other, no significant temperature difference between the wires is expected.

The remaining transformer design parameters, such as core size and number stacked, n_p are chosen by numerical optimization to achieve the highest possible efficiency of the whole converter system at nominal operating conditions. Losses of 30 W are measured with a calorimeter in this case, confirming a 99.6 % full-load efficiency of the transformer.

C. Semiconductors

As in any direct matrix converter, the peak reverse voltage applied to the primary-side MOSFETs is defined by the ac mains line-to-line voltage amplitude. Assuming a 20 % margin for overvoltages and the switching frequency ripple of the input filter capacitor voltages $u_\mathrm{\bar{a}}$, $u_\mathrm{\bar{b}}$ and $u_\mathrm{\bar{c}}$, a peak reverse voltage of 680 V results. C3M0010090K SiC MOSFETs from Wolfspeed with a nominal on-state resistance $R_\mathrm{DS(on)}$ of $10\,\mathrm{m\Omega}$ at 25 °C ($+ \approx 2\,\mathrm{m\Omega}$ bond wire resistance) and a breakdown voltage of 900 V are selected for the DMC switches as they offer the lowest available $R_\mathrm{DS(on)}$ in a four-lead TO-247 package at the time of prototype realization.

The peak reverse voltage of the secondary-side switches is given by the maximum dc voltage u_pn and therefore devices with a breakdown voltage of 650 V, such as GaN HEMTs, could be used. To simplify the design and to avoid using different gate driver circuits, the same type of 900 V SiC MOSFETs as on the primary-side is selected for the full-bridge switches.

1) Conduction Losses: It can be seen from the schematic in Fig. 14(a) that the primary-side winding current i_p is conducted by four DMC switches regardless of the DMC's switching state and that two of the four full-bridge switches conduct the secondary-side winding current i_s. The conduction losses can therefore be calculated as

$$P_\mathrm{c} = R_\mathrm{DS(on)} \left(4\, I^2_\mathrm{p,rms} + 2\, I^2_\mathrm{s,rms}\right) \quad , \tag{46}$$

where the primary-side and secondary-side winding current rms values $I_\mathrm{p,rms}$ and $I_\mathrm{s,rms}$ depend on the operating point and transformer parameters as described in Section III-B. mains (U_1) and dc (U_pn) voltages, the output current i_dc, the switching frequency f_sw and the transformer parameters (L_l, L_m and n).

2) Switching Losses: Calculating the DMC semiconductors' switching losses is not as straight forward, because the rectifier changes from ZCS in DCM (at low output current and/or output voltages significantly larger or lower than the nominal value), over incomplete ZVS (iZVS) to complete ZVS in CCM (cf. Fig. 6). Measured switching loss data for a half-bridge configuration of the selected SiC MOSFETs has been published in [33]. The selected devices achieve complete ZVS

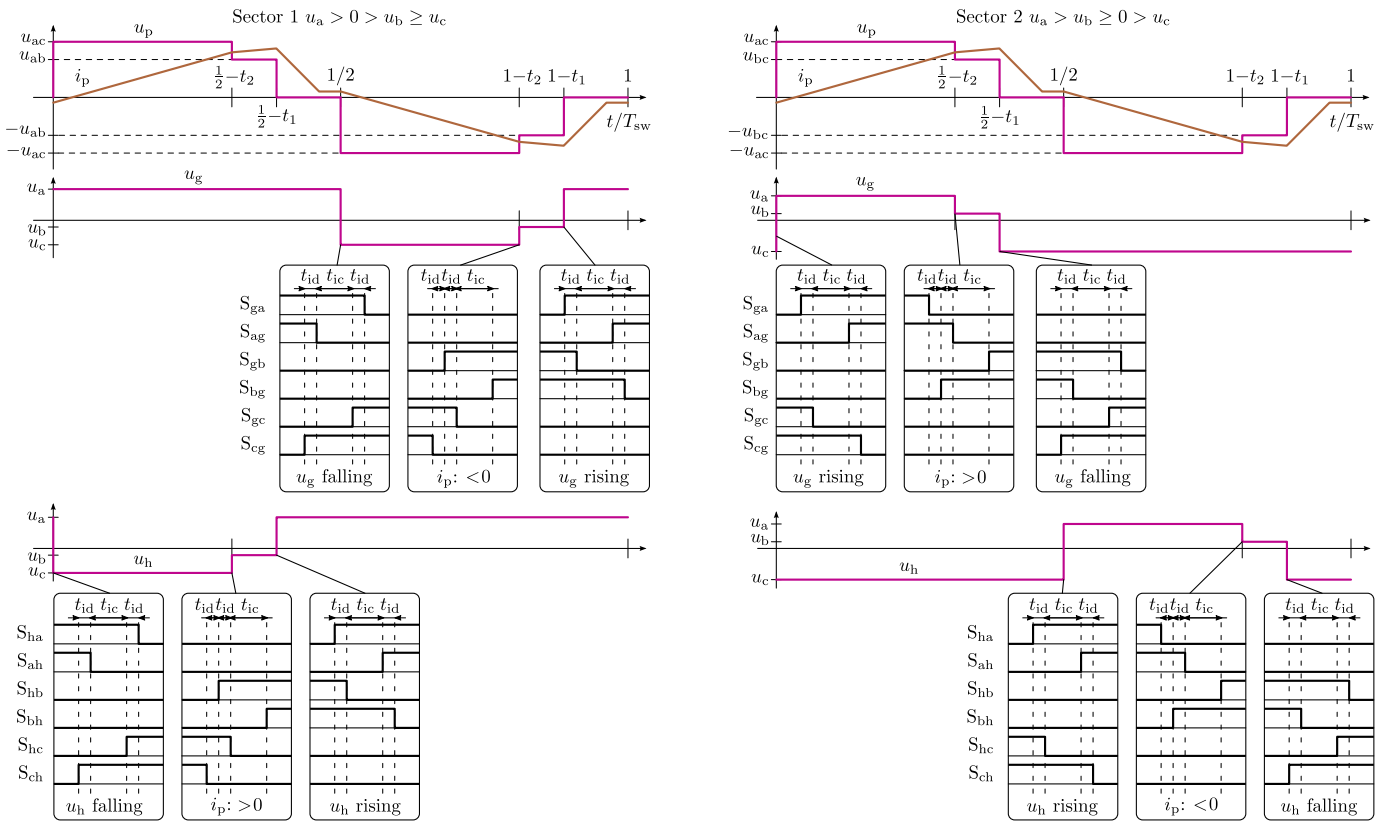

Fig. 16. Drawing of the commutation patterns used for the DMC in sectors 1 (left) and 2 (right). In the free wheeling intervals $1/2 - t_1 \leq t < 1/2$ and $1 - t_1 \leq t < 1$ (i.e. $u_p = 0$) nodes g and h are both connected to the input terminal with the highest absolute value, i.e. input a in sector 1 and input c in sector 2. (Time axes not to scale.)

when switching $\approx 7\,\mathrm{A}$ or more and have ZCS losses that are more than ten times those at complete ZVS. For iZVS the losses are approximated with a quadratic dependence on the switched current [34]. Hence the transformer's magnetizing current typically has a significant impact on the occurring switching losses and it cannot be neglected. Extending the superposition (11) described in Section II-B by using the transformer model shown in Fig. 14(c) the primary and secondary-side winding currents i_p and i_s are calculated as:

$$i_p(t) = i_{p1}(t) + i_{p2}(t) + i_{p3}(t) + i'_{s1}(t) + i'_{s2}(t) + \underbrace{+ \frac{u_{ab}\lambda(t+t_1) + u_{bc}\lambda(t+t_2) + u_{ac}\lambda(t)}{2\,f_{sw}L_m}}_{i_{mp}}, \quad (47)$$

$$i_s(t) = n\,(i_{p1}(t) + i_{p2}(t) + i_{p3}(t) + i'_{s1}(t) + i'_{s2}(t)) - \underbrace{- n\,\frac{u_{pn}}{2\,f_{sw}L_m}\,[\lambda(t+t_3) + \lambda(t+t_4)]}_{i'_{ms}}. \quad (48)$$

Evaluating (47) at $1/2$, $1/2 - t_1$ and $1/2 - t_2$ yields the corresponding currents switched by the DMC MOSFETs with positive values for ZVS. Note that in ZCS and iZVS the charge stored in the output capacitances C_{oss} of the DMC MOSFETs which are constantly turned off during the transition causes additional losses and this has to be accounted for in the calculation of switching losses [35].

The described effects are considered in the converter design and the loss calculations presented in Section IV-D, however a detailed description of the employed models would require too many details and is therefore out of the scope of this paper.

3) DMC Commutation: As the DMC is comprised of six bidirectionally conducting and blocking switches, four-step commutation sequences are required to ensure that no mains line-to-line voltage is shorted and that a valid conduction path for i_p exists at all times [36]. To ensure this, either the sign of i_p, or the sign of the corresponding switching node's voltage edge needs to be known. In total, four sequences can be distinguished: $i_p > 0$, $i_p < 0$, u_g or u_h rising and u_g or u_h falling, where u_g and u_h are the voltages between nodes g or h and the mains neutral. Theoretically, the voltage transition's sign can be determined from the measured mains voltages, however, the matrix converter's input voltages at nodes $\bar{a}$, $\bar{b}$ and $\bar{c}$ exhibit a switching frequency ripple that can lead to sign reversal of the voltage edge. Transitions over the line-to-line voltage with lowest absolute value therefore have to use commutation sequences for a known direction of i_p.

One switching frequency period of the commutation scheme proposed for the IMDAB3R is illustrated in Fig. 16 for sectors 1 (left column) and 2 (right column). Shown are u_g and u_h, an exemplary DCM current i_p, and the twelve MOSFETs' gate signals. At the beginning of a pulse period ($t = 0$) in sector 1 ($u_a > 0 > u_b \geq u_c$) node h is switched from mains input a to c. As u_{ac} is the largest line-to-line voltage, this results in a falling edge of u_h and the corresponding commutation sequence is used for the MOSFETs S_{ha}, S_{ah}, S_{hc} and S_{ch}, which starts by turning on S_{ch}. Assuming that i_p is below

zero, which is the case under ZVS conditions, this does not cause a transition of u_h and the following interlock time t_id is only required to ensure a complete charging of $\mathrm{S_{ch}}$'s gate and to allow for mismatched delay times between different gate drivers. A value of $t_\mathrm{id} = 50\,\mathrm{ns}$ is used in the prototype. The ZVS transition of u_h starts with the turn-off of $\mathrm{S_{ah}}$ and a sufficiently long interlock delay t_ic is required before the subsequent turn-on of $\mathrm{S_{hc}}$. Calculations and measurements indicate that a value of $t_\mathrm{ic} = 300\,\mathrm{ns}$ is required to achieve ZVS or valley switching (incomplete ZVS) if currents of 7 A or lower are switched. Before the last step, the turn-off of $\mathrm{S_{ha}}$ the shorter interlock delay t_id is used again as node h has already reached its final potential.

In the next transition at $t = 1/2 - t_2$, node h is switched from line c to line b. As u_b and u_c are almost equal at the beginning of sector 1, u_h might not be rising in this case. However, as u_p was equal to u_ac since the beginning of the pulse period, it is safe to assume that the primary-side winding current i_p is now positive and the corresponding commutation sequence is used. In this case the third switching event, the turn-off of $\mathrm{S_{hc}}$, initiates the commutation and therefore the first two interlock delays are shorter than the last one. At $t = 1/2 - t_1$ the commutation for a rising edge on u_h is used as node h switches from input b to line a, resulting in a rising edge. In this commutation sequence the turn-off of S_hb starts the ZVS transition and uses the longer interlock delay t_ic. For the second half of the pulse period, node h remains connected to line a and node g performs the same sequence of commutations as node h during the first half period. As before, commutation sequences with know voltage edge directions are used at $t = 1/2$ and $t = 1 - t_1$ and the commutation sequence for $i_\mathrm{p} < 0$ is used at $t = 1 - t_2$.

The right column of Fig. 16 shows the same signals over one pulse period in sector 2 ($u_\mathrm{a} > u_\mathrm{b} \geq 0 > u_\mathrm{c}$, i.e. $30° < \omega t \leq 60°$), which implies that different line-to-line voltages are selected for u_p. To keep the number of required switching transitions at a minimum, nodes g and h are connected to the ac mains line with the largest absolute value (c in sector 2) during the freewheeling intervals $(1/2 - t_2, 1/2)$ and $(1 - t_2, 1)$. This implies that node g is switched during the first half period and node h is switched during the second one in sector 2. In all sectors the transitions at $1/2 - t_2$ and $1 - t_2$ use sequences for known current sign and all others use those for a known voltage edge direction. Switching signals for the remaining ten mains voltage sectors can be derived from those shown in Fig. 16 using symmetry considerations and permuting the mains line voltages. However, the details are not discussed in this paper for the sake of brevity.

If an immediate shutdown of the rectifier is required, for example because the protection circuitry has detected an overcurrent, the transformer needs to be demagnetized without interrupting its winding currents. This implies that the DMC switches cannot be opened immediately. A variation of the procedure described in [37] can be implemented, which ensures that L_l is demagnetized independently of i_p's sign.

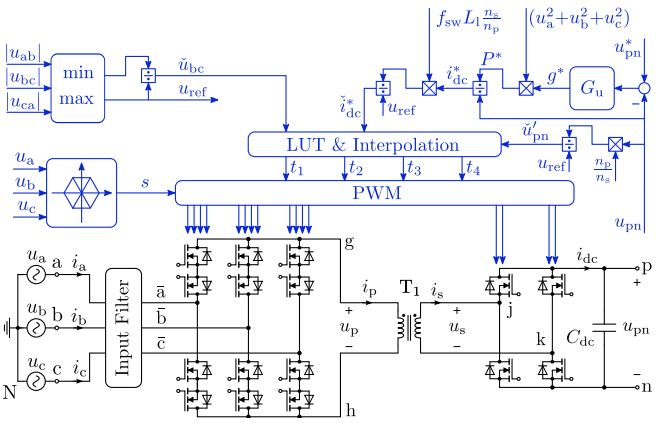

Fig. 17. Schematic of the IMDAB3R, including a block diagram of the implemented closed loop control. The output voltage controller G_u determines the required equivalent three-phase conductance g^* that is rescaled to the normalized dc output current reference signal $\check{i}^*_\mathrm{dc}$. The measured dc voltage u_pn and the minimum of the measured absolute line-to-line ac voltages are normalized and fed in the lookup table (LUT). Measured mains voltages are used to determine the sector s required by the pulse width modulator (PWM).

D. Switching Frequency

The winding currents i_p and i_s, and therefore the conducted and switched currents, vary significantly with the waveforms of u_p and u_s that depend on $\hat{U}_1$, ωt, u_pn and i_dc. However, the output current i_dc that results for given waveforms also depends on the switching frequency f_sw. Increasing f_sw results in a higher normalized current reference $\check{i}^*_\mathrm{dc}$ (cf. (39)), generally leading to lower rms values for i_p and i_s as can be seen in Fig. 12(b). Additionally the transformer's core losses typically reduce with increasing f_sw due to the lower peak flux density, while the proximity and skin effect losses in the windings and the switching losses increase. Hence, an optimal value for f_sw can be found that minimizes the conversion losses for a given operating point. This is verified by measurement results and discussed in more detail in Section IV-D.

E. Output Voltage Control

A block diagram of the proposed dc output voltage control scheme is shown in Fig. 17. First the measured output voltage u_pn is compared to the set point value u^*_pn and fed into a controller G_u to determine the required equivalent line-to-neutral conductance value g^* of each phase that has to be created at the three-phase input. Multiplying g^* with the sum of the measured mains line-to-neutral voltages squared $(u_\mathrm{a}^2+u_\mathrm{b}^2+u_\mathrm{c}^2)$, the required input power P^* results. Dividing P^* by u_pn yields the required output current i^*_dc, which is normalized by multiplying it with the constant $f_\mathrm{sw} L_\mathrm{l} n_\mathrm{s}/n_\mathrm{p}$ and dividing by u_ref as described in Section II-D. The required normalization voltage u_ref is derived by selecting the maximum absolute value of the measured line-to-line voltages u_ab, u_bc, u_ca. Similarly, the minimal absolute line-to-line voltage (u_bc in sector 1) is divided by u_ref to calculate the normalized signal $\check{u}_\mathrm{bc}$ required by the LUT. The measured dc voltage u_pn is rescaled to the primary-side and divided by u_ref to obtain the normalized voltage $\check{u}'_\mathrm{pn}$ that is also fed into the LUT. Using these normalized signals, the surrounding data points in the 3D-LUT are obtained and trilinear interpolation is used to

TABLE IV
EMI FILTER COMPONENTS

C_f	4.5 µF	3× WE 890334026030CS, 1.5 µF, 310 V, X2 rated
$C_{\mathrm{dm},1}$	3.0 µF	2× WE 890334026030CS, 1.5 µF, 310 V, X2 rated
$C_{\mathrm{dm},2}$	1.5 µF	WE 890334026030CS, 1.5 µF, 310 V, X2 rated
C_d	1.5 µF	WE 890334026030CS, 1.5 µF, 310 V, X2 rated
C_fb	2.2 nF	Epcos TDK B32021A3222, 2.2 nF, 300 V, Y2 rated
R_d	3.3 Ω	2 W SMD Resistor
L_dm	15 µH	WE 7443641500

determine the relative switching times t_1, t_2, t_3 and t_4. The measured mains voltages are also used to determine the sector s, which is fed to the pulse width modulator together with the four relative switching times to control the primary-side and secondary-side MOSFETs.

As the mains input currents are created by open loop control only no current sensors are required by the proposed control scheme. This is an advantage for high-efficiency converters as corresponding sensor losses can be avoided.

F. Further Design Considerations

To allow a fair comparison in terms of volumetric power density and efficiency with other three-phase PFC rectifiers, an EMI filter is included in the prototype, however, for the sake of brevity it is not designed specifically for this converter. Instead, a filter similar to the one used for a three-phase buck-type SWISS Rectifier with the same voltage and power rating [38] is used. The schematic of the implemented filter is shown in Fig. 14(b). The filter consists of a two-stage, fourth-order, differential-mode filter formed by L_dm, $C_{\mathrm{dm},1}$ and $C_{\mathrm{dm},2}$. Note that only the second stage contains an R-C damping element formed by R_d and C_d, to avoid the damping resistor losses due to switching frequency voltage ripples in the first filter stage [38].

Due to parasitic coupling capacitances between the transformer's primary and secondary windings, a common-mode current flows from the DMC to the full-bridge. Feedback capacitors C_fb enable this current to return the star point of the input capacitors C_f. A capacitor $C_{\mathrm{Y}2}$ is added between this star point and the converter's aluminum base plate or casing to provide a return path for currents resulting from parasitic capacitances between switching nodes, transformer windings, etc. and the base or casing. Depending on the load's ground capacitance or grounding scheme an additional common-mode filter inductor L_cm might be required to comply with EMI regulations, but this was not implemented in the prototype. As the core of L_cm is not subject to switching frequency voltages or currents, it exhibits only mains frequency conduction losses, which are typically $\approx 1\,\mathrm{W}$.

As the design procedure of the IMDAB3R's EMI filter is essentially not different from that for other buck or buck-boost type PFC rectifiers, it is not discussed here further for the sake of brevity.

G. Designed Prototype

A picture of the hardware prototype is shown in Fig. 18: With outer dimensions of $312\,\mathrm{mm} \times 80\,\mathrm{mm} \times 80\,\mathrm{mm}$ ($12.3\,\mathrm{in} \times 3.15\,\mathrm{in} \times 3.15\,\mathrm{in}$) a total volume of $2\,\mathrm{dm}^3$ results, which corresponds to a power density of $4\,\mathrm{kW\,dm^{-3}}$ ($66\,\mathrm{W\,in^{-3}}$). The distribution of calculated losses for nominal input and output voltages, full load ($i_\mathrm{dc} = 20\,\mathrm{A}$) and $f_\mathrm{sw} = 31\,\mathrm{kHz}$ is shown in Fig. 19(a). Almost half of the total losses ($\approx$ 37 W) occur in the semiconductors, of which 8 W are switching losses and 29 W are due to current conduction. The transformer causes 28 W of losses, approximately equally split between primary winding, secondary winding and the core. The FPGA, gate driver, fans and the auxiliary power supply (three-phase mains to 5 V) consume about 7 W. Conduction losses in the EMI filter inductors cause less than 5 W of losses and other components, such as PCBs and capacitors account for approximately 3 W.

A share of 46 % of the rectifier's total volume is occupied by the transformer and $\approx$ 22 % by the EMI input filter. The heat sinks, fans and MOSFETs require another 16 % of the total volume. The remaining volume holds the control board and gate drivers, as well as the dc output capacitors.

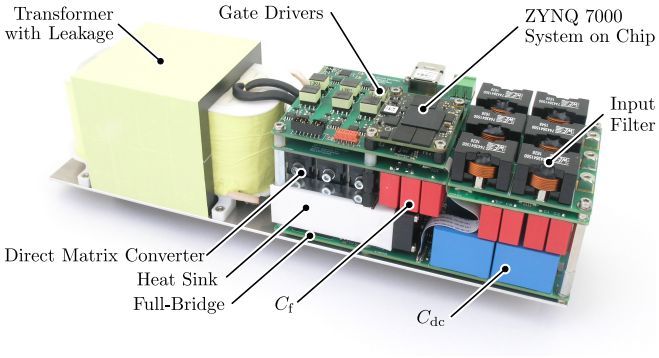

Fig. 18. Picture of the implemented 8 kW prototype, measuring 312 mm × 80 mm × 80 mm, which results in a power density of $4\,\mathrm{kW\,dm^{-3}}$ ($66\,\mathrm{W\,in^{-3}}$).

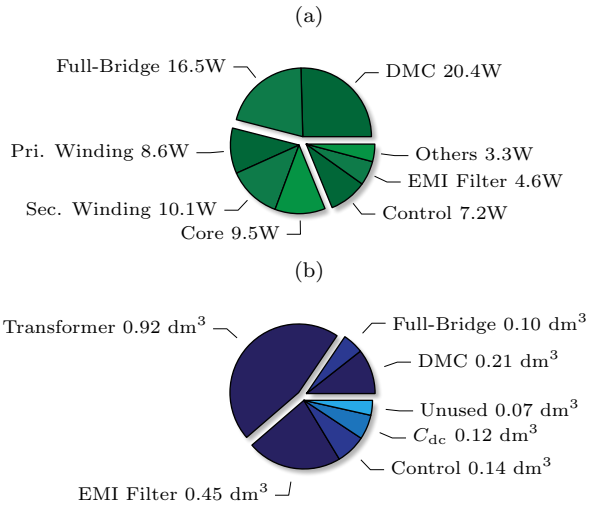

Fig. 19. (a) Breakdown of calculated losses for nominal operation and (b) boxed volumes of the corresponding components ($1\,\mathrm{dm^3} = 61\,\mathrm{in^3}$). The control losses include an FPGA, gate drivers, cooling fans, and a 600 V to 5 V LLC-based auxiliary power supply.

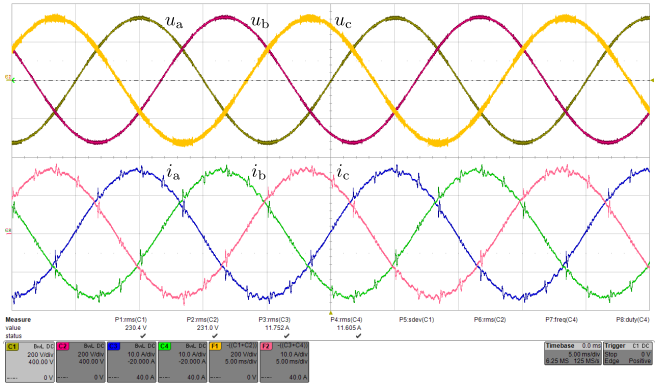

Fig. 20. Measured mains line voltages u_a, u_b and u_c (200 V / div, 5 ms / div) and input currents i_a, i_b and i_c (10 A / div) for nominal operating conditions and $f_{sw} = 33$ kHz. An input current THD of 3.0 % results. Only the quantities of phases a and b are measured directly, those of phase c are created by postprocessing using $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

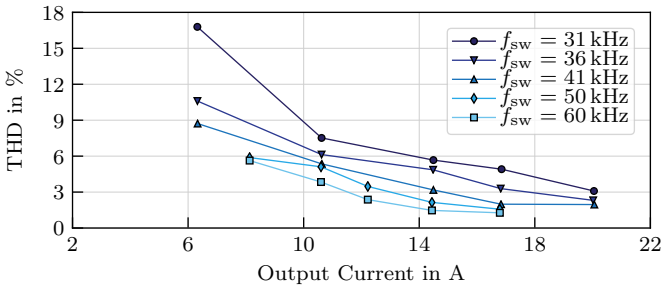

Fig. 21. Input current total harmonic distortion (maximum of phases) for different dc currents and switching frequencies, measured with a *Yokogawa WT3000* power analyzer.

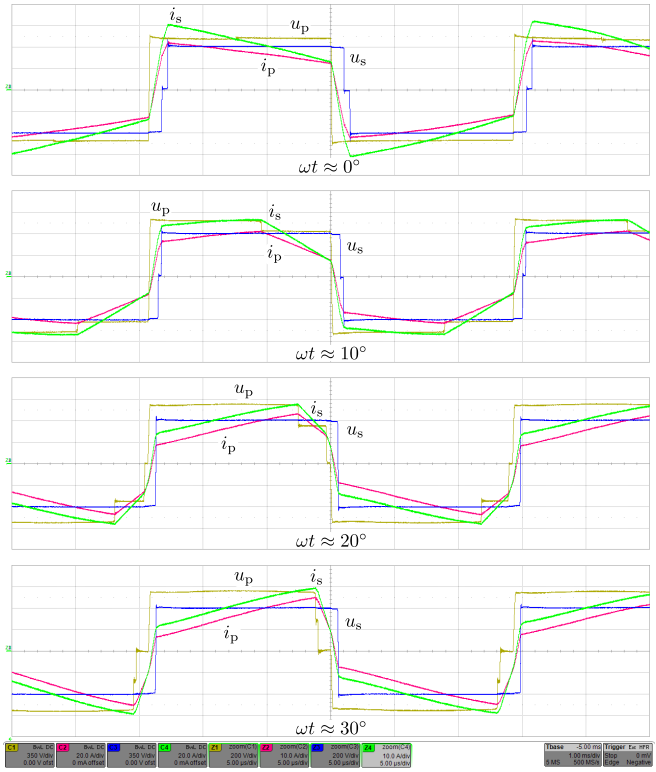

Fig. 22. Measured transformer voltages u_p, u_s (200 V / div, 5 µs / div) and currents i_p, i_s (10 A / div) for nominal operation, $f_{sw} = 35$ kHz and different mains phase angles ωt. It can be seen that all falling edges of u_p and all rising edges of u_s occur with positive transformer currents, which implies that ZVS is achieved. Note: Calculations show that the primary side magnetizing current has an amplitude of ≈ 3 A.

IV. Measurement Results

Measurement results taken on the 8 kW IMDAB3R prototype shown in Fig. 18 are presented in the following.

A. Mains Input Currents

In Fig. 20 the measured ac mains line-to-neutral voltages u_a, u_b and u_c, as well as the corresponding ac input currents i_a, i_b and i_c are shown for nominal operating conditions as defined in Table I. The input currents are sinusoidal and in phase with the mains voltages but show slight distortions at the 30° mains voltage sector boundaries resulting in an input current total harmonic distortion (THD) of 3.0 %. The IMDAB3R acts as a current source for the input filter, causing a relatively large switching frequency voltage ripple at the input capacitors C_f. This voltage ripple affects u_p, which in turn changes the shape of i_p and causes a mismatch between actual and ideal mains input currents. Together with the change of the switching pattern at the sector boundary, this starts a short, damped ringing of the input filter. Similar ac input current distortions exist in buck-type three-phase rectifiers [38–41].

Input current THD values, measured with a *Yokogawa WT3000* power analyzer for different output currents i_{dc} and switching frequencies, are shown in Fig. 21. Generally, the THD values decrease with increasing f_{sw} because errors caused by the switching frequency input voltage ripple and by the dead time between calculating $\vec{t}$ and the actual switching actions, etc. are reduced. This effect is more pronounced for low output currents i_{dc} because the rectifier changes between CCM and DCM operation in every mains voltage sector for low switching frequencies. Relatively long interlock delays (≈ 300 ns) are required to achieve ZVS in CCM, which causes additional dead time and pulse width distortion in DCM and hence repeated transitions between CCM and DCM lead to input current distortions. By increasing f_{sw} the normalized current reference $\check{i}'_{dc}$ increases [cf. (39)] and the converter operates in CCM for longer period during each mains voltage sector. Simulation results suggest that an adaptive selection of interlock delay times, based on the operating conditions (mains voltage, u_{pn}, i_{dc}, etc.) could be used to improve THD at low output currents without loosing complete ZVS in high load conditions. For the sake of brevity this is not discussed further in this paper.

B. Transformer Waveforms

Measured transformer voltages u_p and u_s and the corresponding winding currents i_p and i_s are shown in Fig. 22 for four different mains voltage phase angles ωt. The plots were recoded under nominal operating conditions and with 20 A load current, as specified in Table I. It can be seen that the primary-side winding voltage's falling edges and the secondary-side voltage's rising edges occur entirely with positive winding currents i_p and i_s, which implies that complete ZVS is achieved.

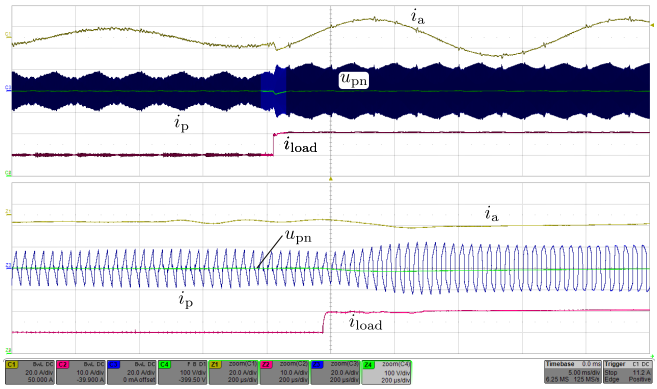

Fig. 23. Measurement results (5 ms / div) for a load transient from half to rated load current. Shown are the mains input current i_a (20 A / div), the primary-side transformer current i_p (20 A / div), the dc output voltage u_{pn} (100 V / div) and the load current i_{load} (10 A / div). The bottom plot (200 µs / div) shows a zoom around the load step.

C. Load Step

In Fig. 23 the measured mains input current i_a, the primary-side winding current i_p, the dc output voltage u_{pn} and the load current i_{load} are shown for a load step from $i_{load} = 10\,A$ to $i_{load} = 20\,A$. This step causes a transient of u_{pn} with a peak voltage drop of 15 V, which is 3.5 % of the set point value. The amplitude of i_p increases during the transient, but i_p stays balanced around zero.

D. Efficiency

Measured rectifier efficiencies and losses are plotted in Fig. 24 as markers, together with calculation results shown as solid lines, for different output currents i_{dc} and nominal voltages ($U_1 = 230\,V$ rms, $U_{pn} = 400\,V$). As the losses vary significantly with f_{sw}, five different curves are shown with switching frequencies between 31 kHz and 60 kHz.

For $i_{dc} \approx 20\,A$ losses of 80 W are achieved with $f_{sw} = 31\,kHz$, resulting in a full-load efficiency of 99 %. Increasing the switching frequency to 36 kHz or 41 kHz reduces the efficiency due to increasing ZVS losses. At a lower load current of $i_{dc} \approx 17\,A$ incomplete ZVS results for $f_{sw} = 31\,kHz$ and the rectifier's total losses can be reduced by increasing the switching frequency to $f_{sw} = 36\,kHz$ as complete ZVS is again achieved. Increasing f_{sw} even further has the contrary affect as higher switching losses result. This frequency dependence is even more pronounced for $i_{dc} \approx 10.5\,A$, as the rectifier operates in DCM for almost the entire mains voltage period with $f_{sw} = 31\,kHz$, but in CCM for $f_{sw} = 60\,kHz$. Besides reducing the switching losses due to ZVS instead of ZCS, this also reduces the rms value of i_p from 10.4 A to 9.1 A, which reduces the conduction losses in the MOSFETs and windings by 23 %. When i_{dc} is reduced further to $\approx 6.5\,A$, the switching frequency required to keep CCM over the whole mains period exceeds 80 kHz. The resulting ZVS switching losses and the increasing skin and proximity effect losses in the transformer windings lead to total rectifier losses that are higher than those at $f_{sw} = 31\,kHz$, as can be seen in Fig. 24. Selecting f_{sw} for minimal losses at the required output current i_{dc}, an efficiency of 99 % results for $12\,A \leq i_{dc} \leq 20\,A$. At

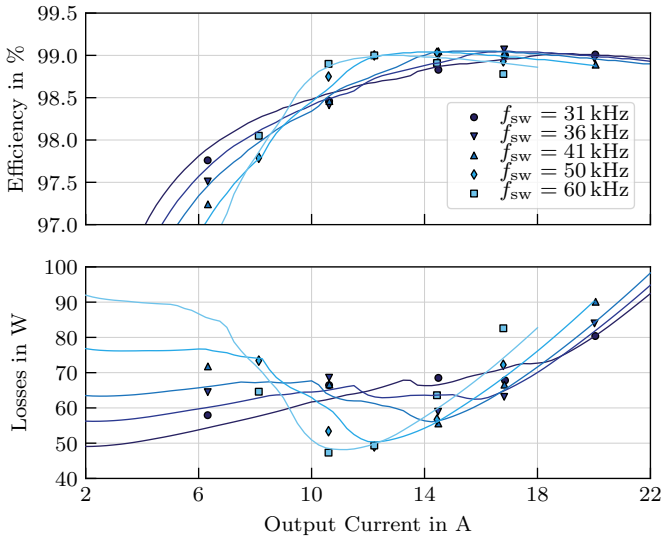

Fig. 24. Measured (markers) and calculated (solid lines) efficiency and losses of the rectifier as a function of the output current i_{dc}, for nominal input ($U_1 = 230\,V$ rms) and output ($U_{pn} = 400\,V$) voltages and various switching frequencies.

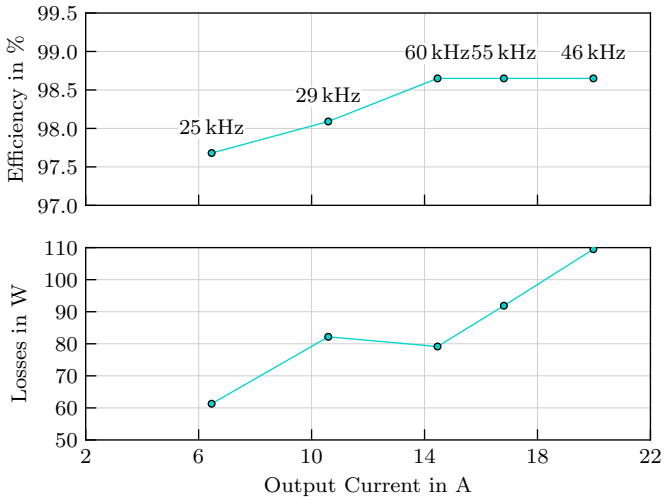

Fig. 25. Measured efficiency and losses as a function of the output current, for a reduced mains voltage of $U_1 = 207\,V$ rms (line-to-neutral) and nominal output voltage ($U_{pn} = 400\,V$). The switching frequency which minimized losses is chosen in each operating point and written above the corresponding markers in the top plot.

half the rated load ($i_{dc} \approx 10.6\,A$) an efficiency of 98.9 % is measured at $f_{sw} = 60\,kHz$.

Measured efficiencies and losses for a 10 % lower mains voltage of $U_1 = 207\,V$ rms and $u_{pn} = 400\,V$ are shown in Fig. 25 for different output currents. In each point the switching frequency which results in the highest efficiency is selected and written on top of the corresponding marker. Compared to nominal voltages, higher switching frequencies are required to achieve minimal losses for a given value of i_{dc}, as the border between DCM and CCM occurs for higher values of i_{dc}. This reduces the achievable peak efficiency to 98.6 % for output currents between 14.4 A and 20 A.

All loss measurements plotted in Fig. 24 and Fig. 25 are taken with a *Yokogawa WT3000* power analyzer. For every

operating point and switching frequency the rectifier was allowed to reach thermal steady state in an ambient temperature of 30 °C (±3 °C). As electrical loss measurements are difficult at such high efficiencies, two operating points, $i_{\mathrm{dc}} = 20\,\mathrm{A}$ at $f_{\mathrm{sw}} = 31\,\mathrm{kHz}$ and $i_{\mathrm{dc}} = 14.5\,\mathrm{A}$ at $f_{\mathrm{sw}} = 41\,\mathrm{kHz}$, are verified by a calorimetric loss measurement. The converter is placed inside a calorimeter which measures the rectifier's heat dissipation thermally at a controlled ambient temperature of $40\,^{\circ}\mathrm{C}$ with a precision of $2\,\%$ (i.e. $1.6\,\mathrm{W}$) [42]; $86\,\mathrm{W}$ and $58\,\mathrm{W}$ of losses are measured, which is only $7.5\,\%$ and $5.4\,\%$ higher than the electrical measurements. As a significant amount of the rectifier's losses are due to conduction losses in the MOSFETs and transformer windings, approximately $4\,\%$ of this difference is likely due to the increased ambient temperature.

V. Summary and Conclusions

This paper analyzes the Isolated Matrix-Type DAB Three-Phase PFC Rectifier (IMDAB3R), which was originally proposed as vehicle-to-grid interface. Due to its structural similarity to the conventional dual active bridge (DAB) converter, an isolation transformer with sufficiently large leakage inductance is the only magnetic component required, except for the EMI filter. This simplifies the mechanical design and potentially reduces cost and/or volume. Additionally, the IMDAB3R does not require any current sensors, as satisfactory mains input current THD values of $3\,\%$ are achieved with open loop control of the transformer current.

A conduction loss optimal modulation scheme for the IMDAB3R, achieving zero current or zero voltage switching, is proposed and thoroughly analyzed in this paper. The required switching times are derived analytically for discontinuous conduction mode and by numerical optimization for continuous conduction mode. This allows to achieve sinusoidal mains currents, in phase with the line voltages for arbitrary dc output currents and voltages. As the time required for the switching time calculation is longer than the cycle time of a typical control loop, off-line optimized switching times for all combinations of mains and dc voltages and output current are stored in a normalized, three-dimensional lookup table. It is used by the digital control circuit to determine near optimal switching times using trilinear interpolation. An implementation of the required optimization routines is published as open source software together with this paper.

To verify the theoretical considerations and to provide a benchmark for the highest achievable efficiency, an $8\,\mathrm{kW}$ isolated three-phase PFC rectifier is designed, implemented and tested. Using novel $900\,\mathrm{V}$ $10\,\mathrm{m\Omega}$ SiC MOSFETs and a transformer with litz wire windings, the prototype achieves a power density of $4\,\mathrm{kW\,dm^{-3}}$. At nominal operating conditions, with $230\,\mathrm{V}$ rms line-to-neutral mains and $400\,\mathrm{V}$ dc output voltage an efficiency of $99\,\%$ is measured for load currents between $12\,\mathrm{A}$ and $20\,\mathrm{A}$, using a load current dependent switching frequency in the range of $31\,\mathrm{kHz}$ to $60\,\mathrm{kHz}$. A mains current THD of less than $4\,\%$ is achieved in this range, which is within usual regulatory restrictions for PFC rectifiers. At full load, $46\,\%$ of the total losses occur in the semiconductors, $35\,\%$ in the transformer and $19\,\%$ are caused by the input filter, control, gate drivers, fans, PCBs and the auxiliary power supply. A $10\,\%$ lower mains voltage ($207\,\mathrm{V}$ rms) leads to higher transformer currents, reducing the efficiency slightly to $98.7\,\%$.

Compared to hard switching circuit topologies, this rectifier's efficiency has a stronger dependence on the operating conditions (i.e. input and output voltages and currents) and the switching frequency, as the rectifier achieves complete ZVS only in a relatively narrow set of operating conditions. This implies that the switching frequency should be changed online, according to the current operating conditions, to achieve the best performance, which complicates the control and modulation circuit. Alternatively the transformer's magnetizing current could be increased to extend the range of operating conditions for which ZVS is achieved with a given switching frequency. However, this also increases conduction losses under nominal operating conditions, reducing the achievable peak efficiency. Further research could address this trade-off. In terms of efficiency and power density, the presented prototype achieves a performance that is close to non-isolated high efficient three-phase PFC rectifiers [11, 35, 38, 52–54]. Note that these converters use semiconductors operated in hard switching and therefore show much flatter efficiency curves as function of input voltage and output current. However, a detailed comparison between isolated and non-isolated high-efficiency rectifiers is out the scope of this paper.

Measured full-load efficiency values of other isolated three-phase rectifiers are summarized in Table V. Even though most of these were not optimized for maximum efficiency, it can be seen that the prototype presented in this paper achieves a reduction of losses by a factor of 2 or more, also compared to systems utilizing state-of-the-art wide bandgap devices. As the isolation transformer is the only magnetic component loaded by switching frequency voltages, this increase in efficiency is not at the expense of power density as can also be seen from Table V.

While this paper focuses on rectifier operation, the derived modulation scheme and the optimized switching times could, in principle, also be used for inverter operation. To do so, the sequence of switching states would have to be reversed, creating a rising stair-case type voltage at the primary winding with a phase leading secondary-side winding voltage. Further research could also address different implementation options for the inductive isolation network, such as using a separate inductor and transformer. To increase the efficiency even further the switching frequency could also be varied within the mains voltage period. Additionally the interlock delays used by the PWM modulators could be varied, ensuring valley switching under incomplete ZVS, and reducing dead time in ZCS switching. This could potentially reduce the input current THD at light load conditions and might also enable a slight reduction of losses as the conduction times of body diodes can be reduced in certain operating points.

Acknowledgment

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TABLE V
COMPARISON TO OTHER ISOLATED THREE-PHASE PFC RECTIFIERS

Topology	Technology	Rated Power	DC Voltage	Meas. Efficiency	Power Density
Phase-Modular SEPIC [43]	Si IGBT & Si Diodes	4 kW	400 V	90 %	unknown
Isolated Full-Bridge Boost [44]	Si IGBT	1.7 kW	200 V	91 %	unknown
Swiss-Forward [21]	SiC MOSFET & SiC Schottky	3 kW	270 V	93.5 %	0.44 kW dm^{-3}
Matrix-Type Isolated Inverter [45]	SiC MOSFET	1.3 kW	400 V	94.1 %	unknown
IMDAB3R [46]	SiC MOSFET & SiC Schottky	1.2 kW	180 V	94.4 %	unknown
Phase-Modular & Scott Transformer [47]	Si IGBT & Si Diode	12 kW	400 V	95.1 %	1.33 kW dm^{-3}
Phase-Modular Ćuk [48]	SiC MOSFET & Si Diode	2 kW	400 V	95.1 %	unknown
Phase-Modular PFC & LLC [49]	Si MOSFET & SiC Diode	10 kW	300 V	95.5 %	unknown
IMDAB3R [14]	SiC MOSFET	1 kW	230 V	96.0 %	unknown
Isolated Matrix-Type Δ Rectifier [50]	SiC MOSFET & SiC Schottky	7.5 kW	400 V	97.2 %	1.03 kW dm^{-3}
Phase-Modular PFC & LLC [51]	GaN HEMT	22 kW	400 V	98 %	3.3 kW dm^{-3}
This Work	SiC MOSFET	8 kW	400 V	99.0 %	4.0 kW dm^{-3}

APPENDIX A
DERIVATION OF EQUATIONS FOR THE MAINS INPUT CURRENTS

In the following equations for the average input currents of the DMC are derived as a function of the voltages u_{ab}, u_{bc} and u'_{pn} and the switching times t_1 to t_4,. It can be seen in Fig. 26 that switch $\mathrm{S_h}$ [cf. Fig. 2(a)] connects node h to the DMC's input terminal c during $0 \leq t \leq 1/2 - t_2$. This implies that the primary-side winding current i_{p} flows into terminal c during this interval. Using the half-wave symmetry of i_{p} this allows to calculate the average of the DMC input current i_{c} over one switching frequency period as:

$$\bar{i}_c = -2 \int_0^{1/2-t_2} i_{\mathrm{p}}(t)\, dt \quad . \tag{49}$$

Note that the time t is normalized to the switching frequency period $T_{\mathrm{sw}} = 1/f_{\mathrm{sw}}$ and is therefore dimensionless.

Inserting (11) we obtain:

$$\bar{i}_c = \frac{-2}{f_{\mathrm{sw}} L_{\mathrm{l}}} \int_0^{1/2-t_2} u_{\mathrm{ab}}\lambda(t+t_1) + u_{\mathrm{bc}}\lambda(t+t_2) + u_{\mathrm{ac}}\lambda(t) - u'_{\mathrm{pn}}\lambda(t+t_3) - u'_{\mathrm{pn}}\lambda(t+t_4)\, dt \tag{50}$$

Using $\xi(t)$, the antiderivative of $\lambda(t)$ given in (13), integration by substitution yields:

$$\begin{aligned}\bar{i}_c = \frac{-2}{f_{\mathrm{sw}} L_{\mathrm{l}}} \Big[& u_{\mathrm{ab}} \left(\xi(\tfrac{1}{2} - t_2 + t_1) - \xi(0 + t_1) \right) \\ & + u_{\mathrm{bc}} \left(\underbrace{\xi(\tfrac{1}{2} - t_2 + t_2)}_{\to 0} - \xi(0 + t_2) \right) \\ & + u_{\mathrm{ac}} \left(\xi(\tfrac{1}{2} - t_2) - \underbrace{\xi(0)}_{\to 0} \right) \\ & - u'_{\mathrm{pn}} \left(\xi(\tfrac{1}{2} - t_2 + t_3) - \xi(0 + t_3) \right) \\ & - u'_{\mathrm{pn}} \left(\xi(\tfrac{1}{2} - t_2 + t_4) - \xi(0 + t_4) \right) \Big] \quad . \end{aligned} \tag{51}$$

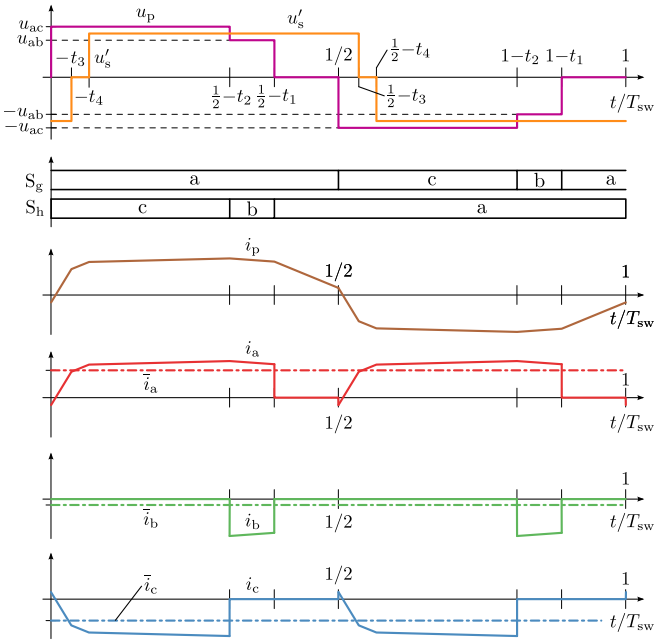

Fig. 26. Drawing (not to scale) of the DMC's input currents i_{a}, i_{b} and i_{c} during one switching frequency period. These would result as mains input currents if no EMI filter and no input filter capacitors C_{f} were installed. It can be seen that i_{c} equals $-i_{\mathrm{p}}$ during $0 < t < 1/2 - t_2$ because the selector switch $\mathrm{S_h}$ [cf. Fig. 2(a)] connects node h to terminal c. Likewise i_{b} equals $-i_{\mathrm{p}}$ during $1/2 - t_2 < t < 1/2 - t_1$.

Considering (13) and Fig. 5, the following properties of $\xi(t)$ can be found:

$$\xi(0) = \xi\left(\frac{1}{2}\right) = \xi(1) = 0 \quad \text{and} \tag{52}$$

$$\xi\left(t + \frac{1}{2}\right) = -\xi(t) \quad . \tag{53}$$

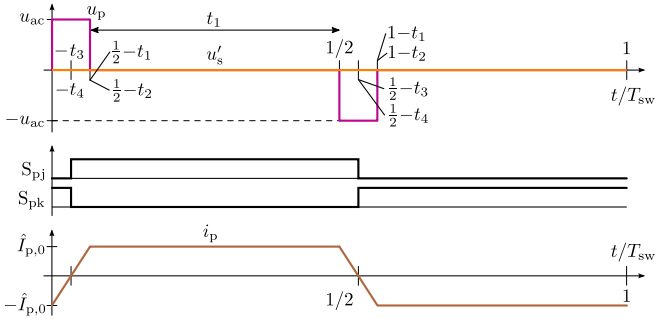

Fig. 27. Drawing (not to scale) of the transformer voltages u_p and u'_s and the primary side winding current i_p for $u'_\mathrm{pn} = 0$. In this case $t_1 = t_2$ and $t_3 = t_4$ is selected, irrespective of the mains voltage phase angle ωt.

This allows to write (51) as:

$$\begin{aligned}\bar{i}_c = \frac{2}{f_\mathrm{sw}\, L_\mathrm{l}} \big[& u_\mathrm{ab}\left(\xi(t_1 - t_2) + \xi(t_1)\right) \\ & + u_\mathrm{bc}\xi(t_2) \\ & + u_\mathrm{ac}\left(\xi(0 - t_2)\right) \\ & - u'_\mathrm{pn}\left(\xi(t_3 - t_2) + \xi(t_3)\right) \\ & - u'_\mathrm{pn}\left(\xi(t_4 - t_2) + \xi(t_4)\right) \big] \quad . \end{aligned} \tag{54}$$

Using Kirchoff's current law on the left part of Fig. 4(a), the current i_c can be calculated as:

$$\bar{i}_\mathrm{c} = \bar{i}_\mathrm{ca} - \bar{i}_\mathrm{bc} \quad . \tag{55}$$

Inserting (15) and (16) into (55) yields the same result as (54). This shows that the derivation described in Section II-B and the one shown here are equivalent. Similar calculations can be performed for $\bar{i}_\mathrm{b}$ and $\bar{i}_\mathrm{a}$, but they are omitted here for the sake of brevity.

Appendix B
Switching Times with Zero DC Output Voltage

In the special case $u'_\mathrm{pn} = 0$, for example during startup of the rectifier, the secondary-side winding voltage u'_s has no impact on the transformer's winding current i_p. As no power can be transferred to the output (due to $u'_\mathrm{pn} = 0$), no power will be drawn from the mains, i.e. $\bar{i}_\mathrm{a} = \bar{i}_\mathrm{b} = \bar{i}_\mathrm{c} = 0$.

To create the desired dc output current i^*_dc a trapezoidal winding current i_p is created by selecting $t_2 = t_1$ as shown in Fig. 27. The secondary side full-bridge switches are controlled with $50\,\%$ duty cycle signals that lead u_p by $1/4$ (i.e. 90°):

$$t_3 = t_4 = \frac{t_1}{2} - \frac{1}{4} \tag{56}$$

and the amplitude $\hat{I}_{\mathrm{p},0}$ of i_p can be calculated as:

$$\hat{I}_{\mathrm{p},0} = \frac{1}{2}\frac{u_\mathrm{ac}}{f_\mathrm{sw}\, L_\mathrm{l}}\left(\frac{1}{2} - t_1\right) \quad . \tag{57}$$

This allows to calculate the resulting dc output current as:

$$\bar{i}_\mathrm{dc} = \hat{I}_{\mathrm{p},0}\left(2\,t_1 + \frac{1}{2} - t_1\right) \quad . \tag{58}$$

By setting $\bar{i}_\mathrm{dc} = i^*_\mathrm{dc}$, the required switching time value t_1 can be found as:

$$t_2 = t_1 = \sqrt{\frac{1}{4} - 2\frac{i^*_\mathrm{dc}\, f_\mathrm{sw}\, L_\mathrm{l}}{u_\mathrm{ac}}} \quad . \tag{59}$$

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