CarrICool: Interposer supporting optical signaling, liquid cooling, and power conversion for 3D chip stacks

Project info
- EU FP7 project
  - Project: 619488
- Begin: Jan. 2014

WP5: Interposer platform
WP2: Heat removal
WP6: Demonstrator
WP3: Power delivery
WP4: Optical signalling

Project partners

Toke M. Andersen¹,², Pedro A. M. Bezerra¹,², Florian Krismer², Johann W. Kolar², Arvind Sridhar², Thomas Brunschwiler², Thomas Toifl², Caroline Rabot³, Zoran Pavlovic³, Cian O’Mathuna³, Sophie Gaborieau⁴, Catherine Bunel⁴

¹ETH Zurich, Switzerland; ²IBM Research Zurich, Switzerland; ³Tyndall National Institute, Ireland; ⁴IPDIA, France
CarrICool project objectives

Functional interposer

- Power conversion
- Optical signaling
- Liquid cooling

CarrICool target demonstrator

Development phases

- Power conversion
- Optical signaling
- Liquid cooling

Power converter (iVRM)

- Deep submicron technology
- L and C on interposer
- Switches and control on CPU

TSV inductors

Inductance Density in nH/mm²

Load Current in A

Target

Embedded Inductors

Discrete Inductors

iVRM demonstrator
### Power management IC – 32nm vs 14nm SOI CMOS

#### Converter specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specifications for 14nm implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>1.7V</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>0.6V to 1.1V</td>
</tr>
<tr>
<td>Efficiency</td>
<td>90%</td>
</tr>
<tr>
<td>PMIC power density</td>
<td>30W/mm²</td>
</tr>
<tr>
<td>Interposer power density</td>
<td>4W/mm²</td>
</tr>
<tr>
<td>$V_{out,peak}$ (steady state)</td>
<td>0.2% of $V_{out}$</td>
</tr>
<tr>
<td>$V_{out,transient}$ (transient)</td>
<td>10mV</td>
</tr>
</tbody>
</table>

- Nominal output voltage is $V_{out,peak}$=650mV. Nominal $V_{in}$ is twice $V_{out,peak}$.
- Variable output voltage to support DVFS.
- Maximum efficiency to be optimized for full load assuming high CPU utilization application.
- Corresponding to <1% CPU area.
- CPU power density is assumed to be 2W/mm². Allowing 50% interposer area to passive gives 4W/mm² interposer power density.
- Transient load conditions are 50% -> 100% $I_{peak}$ load step in 5ns.

---

#### Optimization procedure

- Buck converter
- Adaptive deadtime
- Without inductor losses
- With inductor losses
TSV inductor structures and modeling

**Comparison of analytical model and FEA simulation at 50 MHz (2 µm thick flat core)**

<table>
<thead>
<tr>
<th>Turn number</th>
<th>Toroidal inductor structure</th>
<th>Helical inductor structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Calculation</td>
<td>Maxwell</td>
<td>Calculation</td>
</tr>
<tr>
<td>(nH)</td>
<td>(nH)</td>
<td>(nH)</td>
</tr>
<tr>
<td>8</td>
<td>3.707</td>
<td>3.787</td>
</tr>
</tbody>
</table>

**Comparison of analytical model and FEA simulation**

TSV diameter: 75 µm (half filled vias)

TSV spacing: 50 µm

TSV depth: 200 µm

Cu thickness: 3 µm

<table>
<thead>
<tr>
<th>Turn number</th>
<th>Calculation</th>
<th>Maxwell</th>
</tr>
</thead>
<tbody>
<tr>
<td>(mΩ)</td>
<td>(mΩ)</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>381</td>
<td>385</td>
</tr>
<tr>
<td>12 (10um Cu)</td>
<td>133</td>
<td>136</td>
</tr>
<tr>
<td>8</td>
<td>226</td>
<td>218</td>
</tr>
<tr>
<td>8 (10um Cu)</td>
<td>80</td>
<td>84</td>
</tr>
</tbody>
</table>

**Comparison of analytical model and FEA simulation**

TSV diameter: 75 µm (half filled vias)

TSV spacing: 50 µm

TSV depth: 200 µm

Cu thickness: 3 µm

<table>
<thead>
<tr>
<th>Turn number</th>
<th>Calculation</th>
<th>Maxwell</th>
</tr>
</thead>
<tbody>
<tr>
<td>(mΩ)</td>
<td>(mΩ)</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>817</td>
<td>805</td>
</tr>
<tr>
<td>12 (10um Cu)</td>
<td>695</td>
<td>693</td>
</tr>
<tr>
<td>8</td>
<td>573</td>
<td>572</td>
</tr>
<tr>
<td>8 (10um Cu)</td>
<td>451</td>
<td>452</td>
</tr>
</tbody>
</table>
Deep trench capacitors

- Capacitor density up to 500nF/mm²
- Low leakage current < 1nA/µF, FIT << 1
- Excellent temperature and voltage linearity
- Low ESR & low ESL

3D Capacitors + TSV

Z vs Freq

S21 vs Freq

Ceq vs Freq

Leq vs Freq