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The New High-Efficiency Hybrid Neutral-Point-Clamped Converter

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The New High-Efficiency Hybrid Neutral-Point-Clamped Converter

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***Abstract*—This paper introduces a novel three-level voltage-source converter (VSC) as an alternative to known three-level topologies, including the conventional neutral-point-clamped converter (NPCC), many T-type VSCs, and active NPCC. It is shown that, operating in the low converter dc-link voltage range, this new solution not only can achieve higher efficiency than many typical three-level structures but also can overcome their drawback of asymmetrical semiconductor loss distribution for some operating conditions. Therefore, a remarkable increase of the converter output power capability and/or system reliability can be accomplished. The switching states and commutations of the converter, named here as hybrid NPCC (H-NPCC), are analyzed, and a loss-balancing scheme is introduced. Five- and seven-level H-NPCC topologies with loss-balancing features are also presented. Finally, a semiconductor-area-based comparison is used to further evaluate many three-level VSC systems. Interestingly, the total chip area of the proposed H-NPCC is already the lowest for low switching frequencies.**

***Index Terms*—Neutral-point-clamped converter (NPCC), space vector modulation (SVM), three-level voltage-source converters (VSCs).**

I. Introduction

THREE-LEVEL voltage-source converters (VSCs), particularly the neutral-point-clamped converter (NPCC), are widely used in industrial medium-voltage-range applications (e.g., rolling mills, fans, pumps, marine appliances, mining, tractions, and renewable energy) [1]–[5]. Recent investigations have shown that the NPCC is also a promising alternative for low-voltage applications [6], [7].

Compared to the two-level VSC shown in Fig. 1(a), the three-level NPCC [cf. Fig. 1(b)] features two additional active switches, two extra isolated gate drivers, and four more diodes per phase leg. The three-phase three-level NPCC allows 27 switch states in the space vector diagram, whereas the two-level VSC allows eight switch states only [4]. Hence, the clearly superior controllability of the phase currents and the dc-link voltage U_{dc} is the most distinct advantage over the two-level converter [4]. Additionally, in applications such as photovoltaic grid inverters, rectifiers, motor drives, and active filters, three-level NPCC and/or T-type VSC systems, e.g., that in Fig. 1(c), can achieve lower losses than two-level converters if the switching frequency is high enough [7], [8].

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The main disadvantages of the three-level NPCC and/or T-type VSCs are the relatively high cost, the necessary partial dc-link-voltage-balancing control, and the commonly uneven loss distribution across the bridge-leg semiconductors.

The semiconductor chips assembled in a three-level NPCC bridge-leg module are mostly dimensioned neglecting the loss distribution to the specific elements. This often results in an oversized design with an expensive and weakly utilized semiconductor area [8]. In addition, the typical uneven loss distribution and the resulting different-junction-temperature operation of the individual chip devices could lead to unacceptably high thermal stresses on some power devices, and thermomechanical damage can arise, thus reducing the system reliability [9], [10].

A three-level active NPCC (A-NPCC), which features loss-balancing capability between the power devices, is shown in Fig. 1(d). The two extra active switches per phase leg added to the three-level NPCC, i.e., T_{Ax3} and T_{Ax4}, allow a substantial improvement in the semiconductor loss distribution, while the system efficiency remains nearly unchanged [11].

In this paper, a novel three-level VSC is introduced as an alternative to many three-level topologies, e.g., the conventional NPCC, T-type VSCs, and the A-NPCC. This converter shown in Fig. 1(e) is named hybrid NPCC (H-NPCC). It combines the operating properties of different VSC topologies, having the freedom to control the system in a two- or three-level manner. It is shown that, operating in the low converter dc-link voltage range, this new solution not only can achieve higher efficiency than many typical three-level structures but also can overcome their drawback of extremely asymmetrical loss distribution for some operating conditions. Therefore, a remarkable increase of the converter output power capability and/or system reliability can be accomplished.

This paper is organized as follows. Section II presents a survey of three-level VSC topologies, including the conventional NPCC, the A-NPCC, and various T-type VSC systems. The loss distribution problem of the three-level converters is investigated, and the space vector modulation (SVM) scheme proposed in [14], which incorporates an optimal clamping of the phase, is used to improve the system performance. This strategy can be used to maximize the efficiency of the three-phase three-level systems and/or to improve the distribution of the component losses such that the variation of the power/thermal cycling of the individual elements in a bridge leg is minimized. Subsequently, the novel three-level H-NPCC is introduced in Section III, where the switching states and commutations of the converter are analyzed. A loss-balancing scheme suitable for enhancing the temperature distribution over the employed semiconductor devices is presented. In Section IV, an efficiency comparison between the studied topologies for 10-kVA 50-Hz inverter operation in the switching frequency range of 5–48 kHz

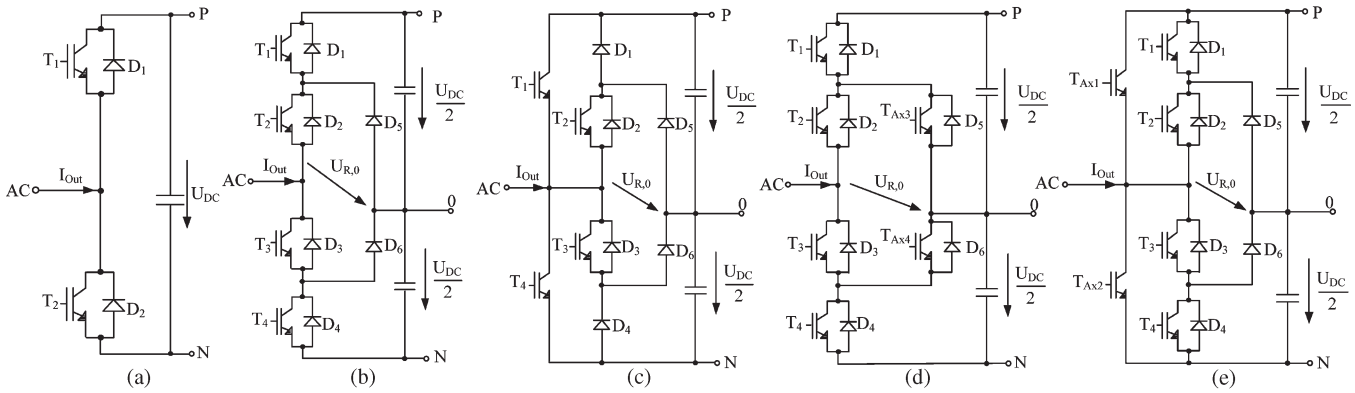

Fig. 1. VSCs. (a) Two-level VSC. (b) Conventional NPCC. (c) Three-level T-type NPCC. (d) Three-level A-NPCC. (e) Three-level H-NPCC.

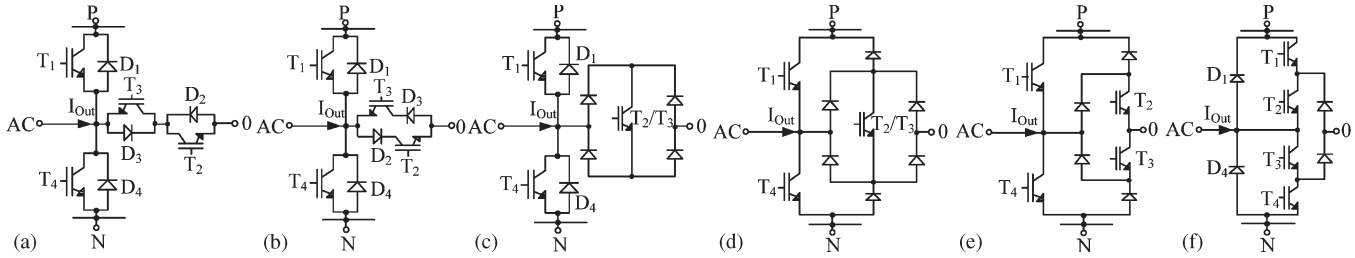

Fig. 2. (a)–(f) T-type VSC topologies. In (a), the four-quadrant midpoint switches could be assembled with common emitter.

and low dc-link voltage level is presented to demonstrate the performance and feasibility of the novel three-level H-NPCC. Additionally, analytical expressions for loss calculation of the H-NPCC semiconductor devices are presented. Finally, in Section V, a semiconductor-area-based comparison is used to further evaluate many three-level VSC systems.

II. Survey on Three-Level VSC Topologies

Fig. 1 shows the bridge-leg structures of three-phase VSCs in two- and three-level configurations, including the two-level VSC, the conventional NPCC, the T-type NPCC, the A-NPCC, and the proposed H-NPCC.

A typical three-level T-type converter constitutes a standard two-level VSC with an active bidirectional switch connecting the ac terminal with the dc-link midpoint "0." Figs. 1(c) and 2 show several arrangements of T-type VSCs. For low rated dc-link voltage level in the range of 700–1000 V, as for the two-level VSC, the T-type topologies shown in Fig. 2(a)–(e) would require 1200-V insulated-gate bipolar transistors (IGBTs) for the top and bottom switches, i.e., T_1 and T_4. The systems shown in Fig. 2(a)–(c) and (f) also need 1200-V diodes for the top and bottom switches, i.e., D_1 and D_4. Since the bidirectional midpoint switches have to block only half of the dc-link voltage, 600-V IGBT and diodes can be used.

The three-level NPCC topology is most often used for medium-voltage-range applications. The factors preventing the NPCC from being successful in the low-voltage market are increased costs and complexity. For low dc-link voltage level, six diodes and four IGBTs per phase leg rated at 600 V are required. However, the number of IGBTs and isolated gate drives is twice that of the two-level VSC. Compared to the T-type NPCC [cf. Fig. 1(c)], which allows the connection of two IGBTs with a common emitter, the NPCC needs one more isolated gate drive per phase leg.

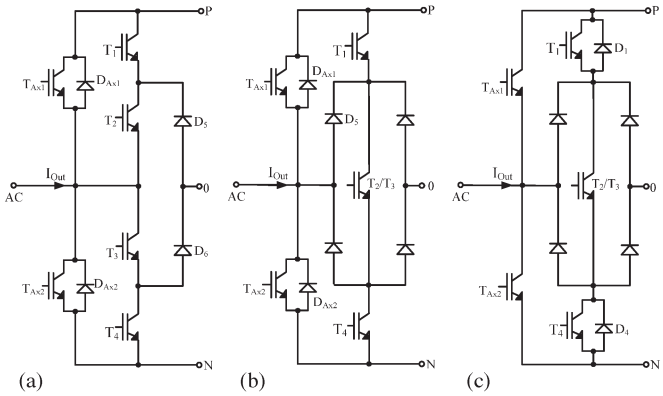

Fig. 3. (a)–(c) New three-level hybrid VSCs.

Two substantial disadvantages of the conventional NPCC and T-type VSCs are the commonly uneven loss distribution across the semiconductor devices and the resulting asymmetrical temperature distribution over their junctions [13]. Adding two extra active switches to each phase leg of the conventional NPCC allows a substantial improvement to loss distribution, utilizing the additional switching states and new commutation possibilities [cf. Fig. 1(d)] [11]. This configuration, known as A-NPCC, permits a specific utilization of the upper and lower paths of the neutral tap and, thus, affects the distribution of conduction and switching losses among the semiconductor devices [11], [13]. When compared to the conventional NPCC, the A-NPCC requires two extra active switches and one isolated gate driver per phase leg (T_{Ax3} and T_{Ax4}).

As for the A-NPCC, the three-level H-NPCC, shown in Fig. 1(e), requires two extra switches when compared to the conventional NPCC (T_{Ax1} and T_{Ax2}) or the T-type NPCC. The strategically placed auxiliary switches allow the topology to operate equally to the conventional NPCC [cf. Fig. 1(b)] and/or the T-type NPCC [cf. Fig. 1(c)]. For operation in the low voltage

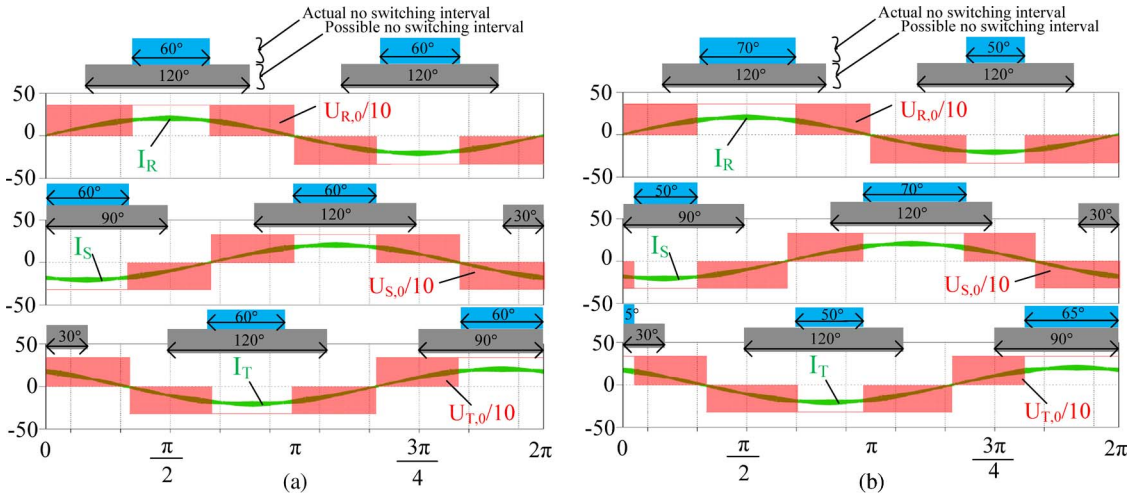

Fig. 4. Loss-minimized SVM for three-phase three-level VSC topologies: (a) Optimal clamping of the phases, where $P_{\rm NS} = 60°$ and $N_{\rm NS} = 60°$, and (b) clamping strategy during unbalanced dc-link capacitor voltages, where $P_{\rm NS} = 70°$ and $N_{\rm NS} = 50°$.

converter range, 1200-V devices are necessary, in contrast to the A-NPCC, which requires 600-V auxiliary switches. Other circuit implementations of the three-level H-NPCC are shown in Fig. 3. Note that the auxiliary switches could also be added to the A-NPCC. The H-NPCC shown in Fig. 1(e) is analyzed thoroughly in Section III.

In order to address the loss distribution issue of the three-level conventional NPCC and T-type VSCs, an SVM scheme incorporating an optimal clamping of the phase is used in Section II-A.

A. *Loss-Minimized SVM*

Several modulation and control strategies exist for the three-level NPCC, which could be used not only in the A-NPCC and T-type VSCs but also in the proposed three-level H-NPCC. Rodriguez *et al.* [13] provide a survey of NPCCs, where many suitable strategies are listed.

For the systems presented in this paper, an SVM scheme incorporating an optimal clamping of the phase, as described in [14], is considered for analysis. The output voltage vector is always formed with the three nearest discrete voltage space vectors. Since the three-level topology offers redundant space vectors on the inner hexagon, it is possible to implement an optimal clamping strategy in order to reduce switching losses.

For the whole vector space, the possible no-switching interval can be described as shown in Fig. 4(a). The switching operation of each phase leg of a three-phase three-level VSC can be stopped for 120° in one period, generating almost the same distorted output currents as typical sinusoidal pulsewidth modulation (SPWM) methods [14]. When aiming for high efficiency, particularly during high operating frequency, the "no-switching interval" can be set to match the phase leg with the highest current values. With regard to the symmetry of three phases, the no-switching duration must be 60° for positive and negative load currents. The optimal clamping scheme allows a phase shift drift φ_{vi} of up to 30° between the fundamental output voltage $U_{\rm Out}$ and current $I_{\rm Out}$. For $\varphi_{vi} > 30°$, the effect of reducing the switching loss will be somewhat decreased [14].

Although, under the optimum clamping condition, the dc-link capacitor voltages naturally balance over one fundamental cycle, asymmetries in the semiconductor characteristics, different gate delay times, dynamic load changes, and/or unbalanced loads can cause a steady drift of the neutral-point potential [4]. In order to keep the balancing of the dc-link capacitor voltages, while the optimal clamping of the current is partially maintained, a proper selection of the no-switching interval is required.

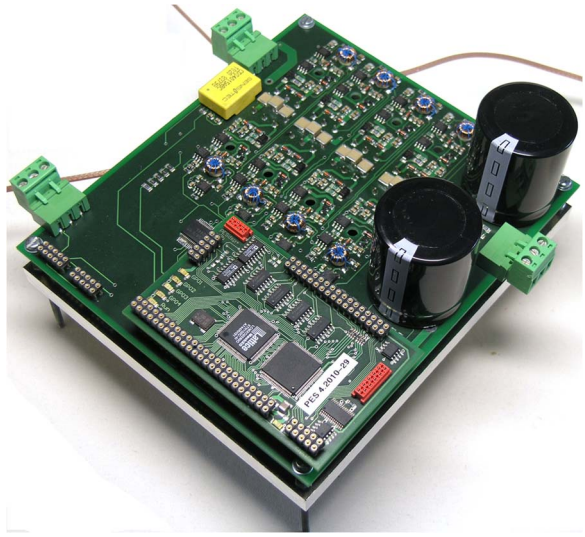

Fig. 5. Single-phase hardware specifically designed to enable operation of any of the VSC topologies shown in Fig. 1.

An asymmetric modulation, where the no-switching intervals differ in each phase for the positive and negative output currents, can be used for the balancing control as shown in Fig. 4(b). It is desirable to keep the current clamping schemes in each phase equal in order to keep the average losses among them even; thus, the positive $P_{\rm NS}$ and negative $N_{\rm NS}$ no-switching intervals for each phase must fulfill $P_{\rm NS} + N_{\rm NS} = 120°$. Typically, for $P_{\rm NS} < 60°$, the upper dc-link capacitor is charged while the bottom capacitor is discharged. When $P_{\rm NS} > 60°$, the capacitor charging cycle is changed. Therefore, it is possible to maintain the stability of the neutral-point potential with no additional circuitry and no additional switching transitions. In the case of severe dc-link voltage imbalance, the redundant zero vectors of the inner hexagon are selected to

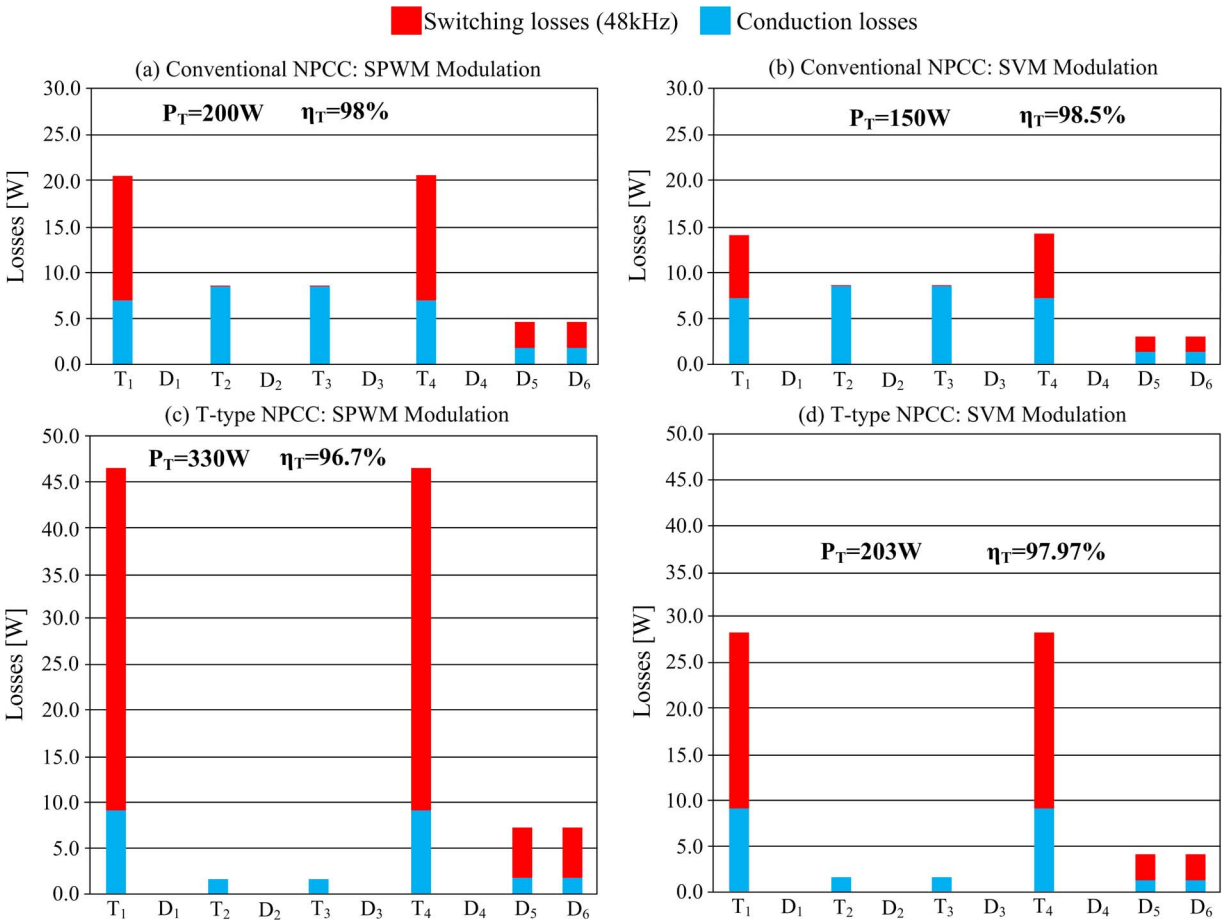

Fig. 6. Phase-leg component loss distribution for three-phase three-level inverters operating with conventional NPCC (a) SPWM and (b) SVM and with T-type NPCC (c) SPWM and (d) SVM. Note that, for the analyzed operating point, D_1, D_2, D_3, and D_4 do not conduct current.

ensure the stability of the system, without paying attention to the optimal clamping of the phase (cf. [8]).

It should be understood that, due to the lower switching losses when compared to conventional SPWM [15], the optimal clamping strategy can provide substantial improvement to the loss distribution of the three-level topologies. For inverters based on three-level NPCC and T-type NPCC, operating at high switching frequency (f_s), maximum output current, high modulation index (M), and unitary power factor $(\varphi_{vi} = 0^\circ)$, the outer switches are normally the most stressed devices. These devices experience very high switching losses, while the inner switches display virtually only conduction losses. Therefore, in the case that all switches of the inverter are similarly rated and/or assembled within a power module, the difference between the operating junction temperatures of these devices could considerably differ for the conventional SPWM. Hence, during critical operating points, a derating of the converter could become mandatory to ensure the system stability [4].

In order to quantify the feasibility of the studied loss-minimized SVM, simulations are performed for two 3-phase 3-level inverters, one based on a conventional NPCC and another derived from a T-type NPCC. These systems, rated to 10 kVA, are set to operate at 48-kHz switching frequency and the following specifications: $\hat{U}_{\mathrm{Out}} = 325$ V, $\hat{I}_{\mathrm{Out}} = 20.5$ A/ 50 Hz, $\varphi_{vi} = 0^\circ$, and $U_{\mathrm{dc}} = 700$ V. The Infineon IGBTs 600-V IKW30N60T and 1200-V IGW25T120 are selected for the assessment, and their loss characteristics are determined with a test setup specifically designed to enable operation of any of the single-phase topologies shown in Fig. 1 (cf. Fig. 5).

An optimized heat sink with a thermal resistance of $Rth = 0.1$ K/W has been designed and considered in the thermal analysis. The thermal models of the devices are obtained directly from the datasheet, including the thermally conductive insulating material Hi-Flow from Bergquist $(Rth \approx 0.4$ K/W). For comparative purposes, two modulation schemes are analyzed: the conventional SPWM in which there is no reduction of switching losses and the SVM with optimal clamping.

For each inverter, the resulting averaged power loss distribution and the operating junction temperature T_J of the individual elements in a phase leg are shown in Figs. 6 and 7, respectively. In Fig. 7, a constant ambient temperature T_A of 50 °C is assumed in the analysis. The temperature distribution across the heat sink T_{HS} is regarded as uniform. It can be seen that the systems operating with SPWM yield the lowest efficiency η_T as total semiconductor losses P_T of 200 and 330 W exist for the conventional NPCC and the T-type NPCC, respectively. By avoiding switching currents with high values, the SVM obtains expressive loss reduction as it provides 25% and 38.5% less power dissipation for the conventional NPCC and the T-type NPCC, respectively. Additionally, the operating junction temperatures of the upper, bottom, and inner IGBTs are always better balanced for the SVM. Finally, for both systems employing SVM, the operating junction temperature ripples and maximum values of the outer transistors T_1/T_4 and

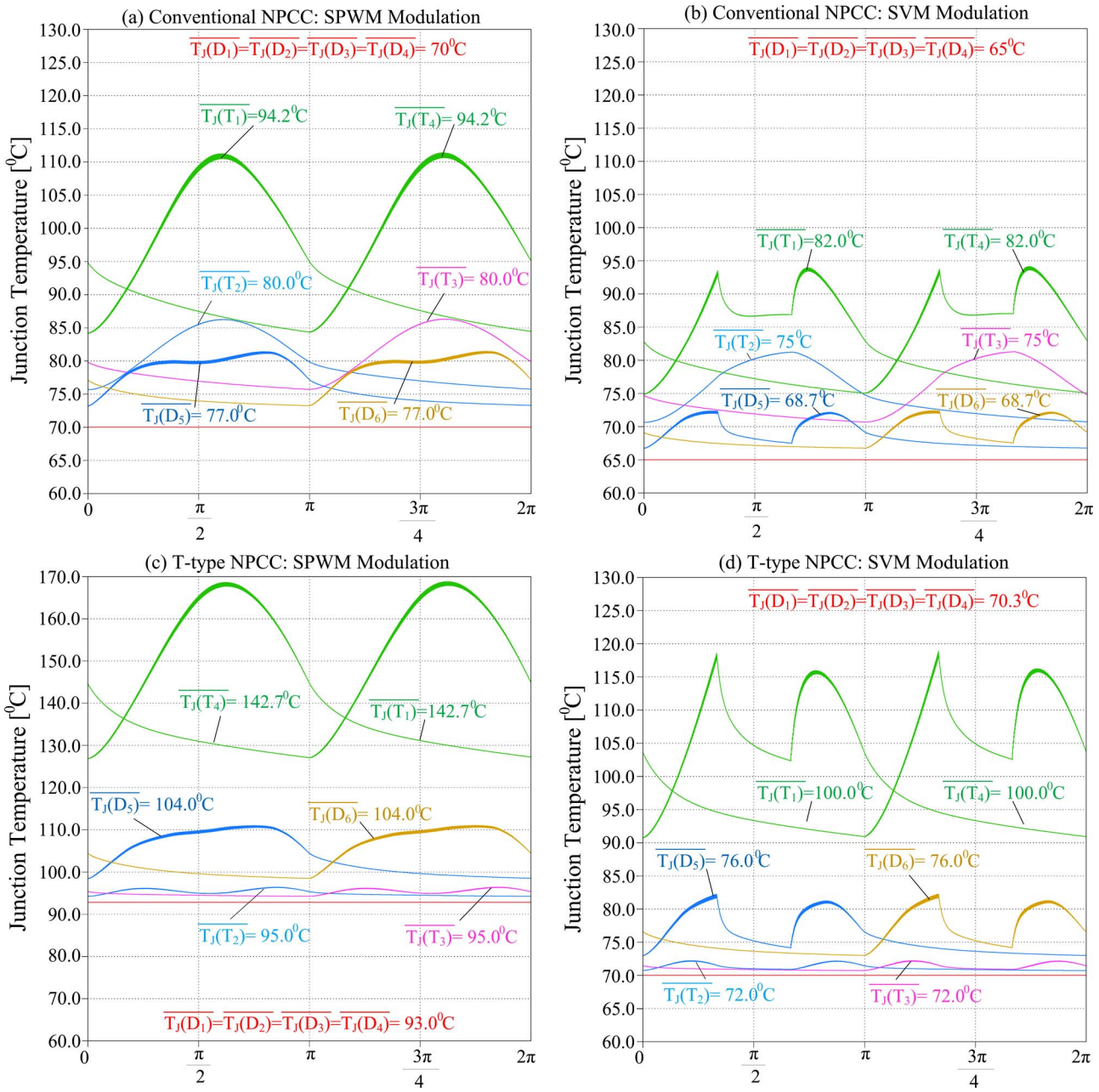

Fig. 7. Phase-leg component operating junction temperature for three-phase three-level inverters operating with conventional NPCC (a) SPWM and (b) SVM and with T-type NPCC (c) SPWM and (d) SVM. Note that the averaged junction temperature of each device is given.

clamping diodes D_5/D_6 are always smaller than those for the SPWM (cf. Fig. 7).

It is important to point out that, for the inverter operation considered in this analysis, the T-type structures shown in Figs. 1(c) and 2(a), (b), and (e) would display very similar efficiencies and loss distributions across the components. This is particularly true because the commutations during switching transitions and the numbers of components conducting in the current path, including device technologies, are always the same for all these topologies.

III. H-NPCC

As for the A-NPCC, the proposed H-NPCC requires two extra switches when compared to the conventional NPCC or the T-type NPCC (per phase leg). The power supplies of the isolated gate drives for T_2 and T_4 can be advantageously used for T_{Ax1} and T_{Ax2}, respectively. In contrast to the A-NPCC, for operation in the low dc-link voltage converter range, 1200-V devices are employed as auxiliary switches [see T_{Ax1} and T_{Ax2} in Fig. 1(e)]. The A-NPCC would require two extra 600-V-rated active switches per phase leg [see T_{Ax3} and T_{Ax4} in Fig. 1(d)].

The strategically placed auxiliary switches T_{Ax1} and T_{Ax2} allow the system to operate like the conventional NPCC [cf. Fig. 1(b)], the T-type NPCC [cf. Fig. 1(c)], and/or the two-level VSC. In contrast to the A-NPCC, which offers extra redundant zero states to the conventional NPCC (central tap "0"), the new switches create redundant switch states to the "P" and "N" potentials. Therefore, the losses across the devices within the phase leg can be strategically distributed.

TABLE I
SWITCH STATES OF THE THREE-LEVEL H-NPCC

Device	T_1	T_2	T_3	T_4	T_{Ax1}	T_{Ax2}	Operating mode
State P1	1	1	0	0	0	0	NPCC
State P2	0	1	0	0	1	0	T-type NPCC
State P3	1	1	0	0	1	0	NPCC/T-type
State 0	0	1	1	0	0	0	NPCC/T-type
State N1	0	0	1	1	0	0	NPCC
State N2	0	0	1	0	0	1	T-type NPCC
State N3	0	0	1	1	0	1	NPCC/T-type

During T-type NPCC operation, conduction losses can be drastically reduced, as fewer devices exist in the current path. This characteristic allows higher efficiency operation when compared to the conventional NPCC and/or the A-NPCC, which always contains two conducting devices. In fact, the losses for the A-NPCC are similar to those for the conventional NPCC, and the main advantages in the use of this more complex structure are the loss balance control capability and the voltage clamping possibility which guarantees an equally shared voltage between the main devices T_1/T_2 and T_3/T_4.

In inverter operation, by proper selection of the redundant "P" and "N" switching states, it is possible to improve the efficiency of the three-level H-NPCC. The losses of the system can be distributed such that the auxiliary switches T_{Ax1} and T_{Ax2} mainly display conduction losses while the outer switches T_1 and T_4 are mostly stressed with switching losses. Hence, transistors with excellent ON-state features could be selected for the auxiliary switches, while high-speed devices would be more suitable for the outer switches.

A. Switching States and Commutations

A single phase leg of the H-NPCC, shown in Fig. 1(e), is taken into consideration. The switching states of the proposed system are given in Table I. As can be noted, the redundant switch states "P1" and "N1" define the conventional NPCC operation, while the states "P2" and "N2" express the T-type NPCC operation. The states "P3" and "N3" characterize a hybrid operation of the system, where T-type and NPCC operations are blended in order to improve the system efficiency. Note that the direct commutation to or from the terminals "P" and "N" (P $\leftrightarrow$ N), using "P1," "P2," "P3," "N1," "N2," or "N3," describes the two-level VSC operation.

The commutations to or from the new states, incorporated in the conventional NPCC, determine the distribution of power losses across the semiconductor devices. As for the conventional NPCC and the A-NPCC, all commutations take place between one active switch and one diode; even if more than two devices turn on or off, only one active switch and one diode experience essential switching losses [4].

Assuming the operating conditions where the ac terminal has impressed positive or negative current ($I_{\rm Out} > 0$ or $I_{\rm Out} < 0$) and positive output voltage $U_{\rm Out}$, the commutations to or from "P1," "P2," and "0" are given in the following.

1) Commutation "P1" to "0" (P1 $\rightarrow$ 0): This commutation starts when T_1 is turned off and finishes after a dead time when T_3 is turned on. If $I_{\rm Out} < 0$, as shown in Fig. 8(a), the current $I_{\rm Out}$ commutates from T_1 to D_5 after T_1 is turned off, and essential turn-off losses occur at T_1. If $I_{\rm Out} > 0$, as shown in Fig. 8(b), the current $I_{\rm Out}$ commutates from D_1/D_2 to T_3 and D_6 after T_3 is turned on. Hence, T_3 faces turn-on losses, while D_1 suffers recovery losses.
2) Commutation "0" to "P1" (0 $\rightarrow$ P1): This commutation starts when T_3 is turned off and finishes after a dead time when T_1 is turned on. If $I_{\rm Out} < 0$, as shown in Fig. 8(a), the current $I_{\rm Out}$ commutates from D_5 to T_1 during the turn-on of T_1. In this case, T_1 and D_5 experience turn-on and recovery losses, respectively. If $I_{\rm Out} > 0$, as shown in Fig. 8(b), the current $I_{\rm Out}$ commutates from D_6/T_3 to D_1/D_2 during the turn-off of T_3. Therefore, essential turn-off losses occur at T_3.
3) Commutation "P2" to "0" (P2 $\rightarrow$ 0): This commutation starts when T_{Ax1} is turned off and finishes after a dead time when T_3 is turned on. If $I_{\rm Out} < 0$, as shown in Fig. 9(a), during the turn-off of T_{Ax1}, the current $I_{\rm Out}$ commutates from T_{Ax1} to T_2 and D_5, and essential turn-off losses occur at T_{Ax1}. If $I_{\rm Out} > 0$, as shown in Fig. 9(b), the current $I_{\rm Out}$ commutates from D_1/D_2 to T_3 and D_6 after T_3 is turned on. Thus, T_3 and D_1 experience turn-on and recovery losses, respectively.
4) Commutation "0" to "P2" (0 $\rightarrow$ P2): This commutation starts when T_3 is turned off and finishes after a dead time when T_{Ax1} is turned on. If $I_{\rm Out} < 0$, as shown in Fig. 9(a), the current $I_{\rm Out}$ commutates from T_2 and D_5 to T_{Ax1} after T_{Ax1} is turned on. In this case, T_{Ax1} and

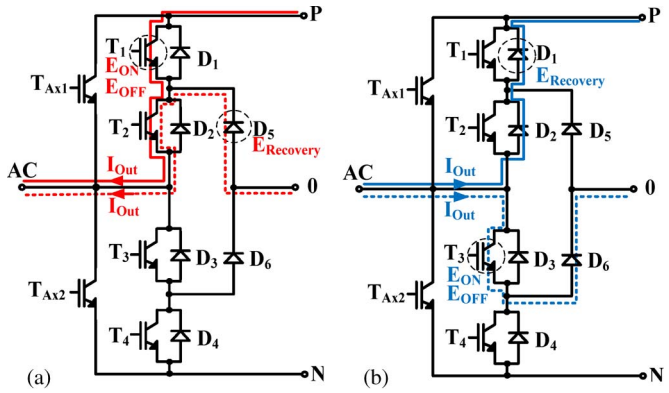

Fig. 8. Commutation (P1 $\leftrightarrow$ 0) in the three-level H-NPCC for conventional NPCC operation mode: (a) $I_{\rm Out} < 0$ and (b) $I_{\rm Out} > 0$.

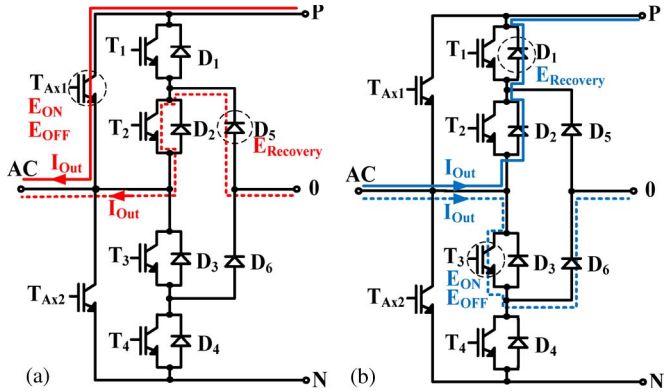

Fig. 9. Commutation (P2 $\leftrightarrow$ 0) in the three-level H-NPCC for T-type NPCC operation mode: (a) $I_{\rm Out} < 0$ and (b) $I_{\rm Out} > 0$.

D_5 experience turn-on and recovery losses, respectively. If $I_{\mathrm{Out}} > 0$, as shown in Fig. 9(b), the current I_{Out} commutates from D_6/T_3 to D_1/D_2 after T_3 is turned off. Thus, essential turn-off losses occur at T_3.

For the switch states "P3" and "N3," particular attention has to be paid to the current distribution between the two redundant paths. For instance, in the event that T_1 and T_{Ax1} are turned on at once, the ON-state characteristics of these devices, the prior switching state, etc., would strongly influence the current distribution between these components, and their losses would not be precisely defined.

In order to take advantage of the commonly good switching performance of the path T_1/T_4 and the usually superior ON-state characteristic of the path T_{Ax1}/T_{Ax2}, the switching commutation to or from "P3" and "0" (P3 $\leftrightarrow$ 0), shown in Fig. 10(a), is recommended. Therein, the optimum current transitions between T_1 and T_{Ax1} are shown, where T_1 displays mainly switching losses (turn-off: $t_5 \rightarrow t_6$; turn-on: $t_7 \rightarrow t_8$). T_1 suffers conduction losses only during the times t_{d1} and t_{d2}. These time intervals must be selected taking into account the current "tail" of the slow switch in order to preserve the soft-switching feature in T_{Ax1}. Note that the interval $t_0 \rightarrow t_2$, with $t_1 \rightarrow t_2$ being very short, must be much bigger than $t_3 \rightarrow t_5$ in order to ensure that the conduction losses during "P3" are mainly dissipated across T_{Ax1}. This commutation was implemented in the prototype shown in Fig. 5, and the experimental result is shown in Fig. 10(b).

Another commutation possibility for (P3 $\leftrightarrow$ 0) is shown in Fig. 10(c), where the turn-on time interval during the "P3" state for T_1 overlaps that of T_{Ax1} in order to ensure that the switching transitions are performed only by T_1 and the current conduction is executed mainly by T_{Ax1}.

An alternative to the desired commutations, (P3 $\leftrightarrow$ 0) or (N3 $\leftrightarrow$ 0), is achieved if, during the optimal clamping interval of the SVM, the system operates only as T-type NPCC and, during all other intervals, the system operates solely as the conventional NPCC. Therefore, T_{Ax1}/T_{Ax2} only displays conduction losses, while T_1/T_4 is mainly stressed with switching losses.

Table II summarizes the aforementioned commutation descriptions, where the distribution of the main switching losses for positive and negative currents is shown.

B. Loss-Balancing Control

As for the A-NPCC, the general approach used to optimize the distribution of the losses over the power semiconductors and/or to equalize their junction temperatures is to always keep the hottest devices as cool as possible [4]. For real-time optimization, the junction temperatures of the main semiconductors need to be estimated or measured at every sampling time. Based on the temperatures and phase current information, a simple algorithm could then select the appropriate commutations in order to alleviate losses from the hottest device for the coming switching period. Therefore, a substantial improvement in the loss distribution can be achieved, enhancing the reliability and/or power capability of the system. This feedback-controlled loss-balancing method was previously proposed for the A-NPCC in [4] and can be simply adapted to the proposed three-level H-NPCC by the use of a decision chart for the commutations shown in Table III.

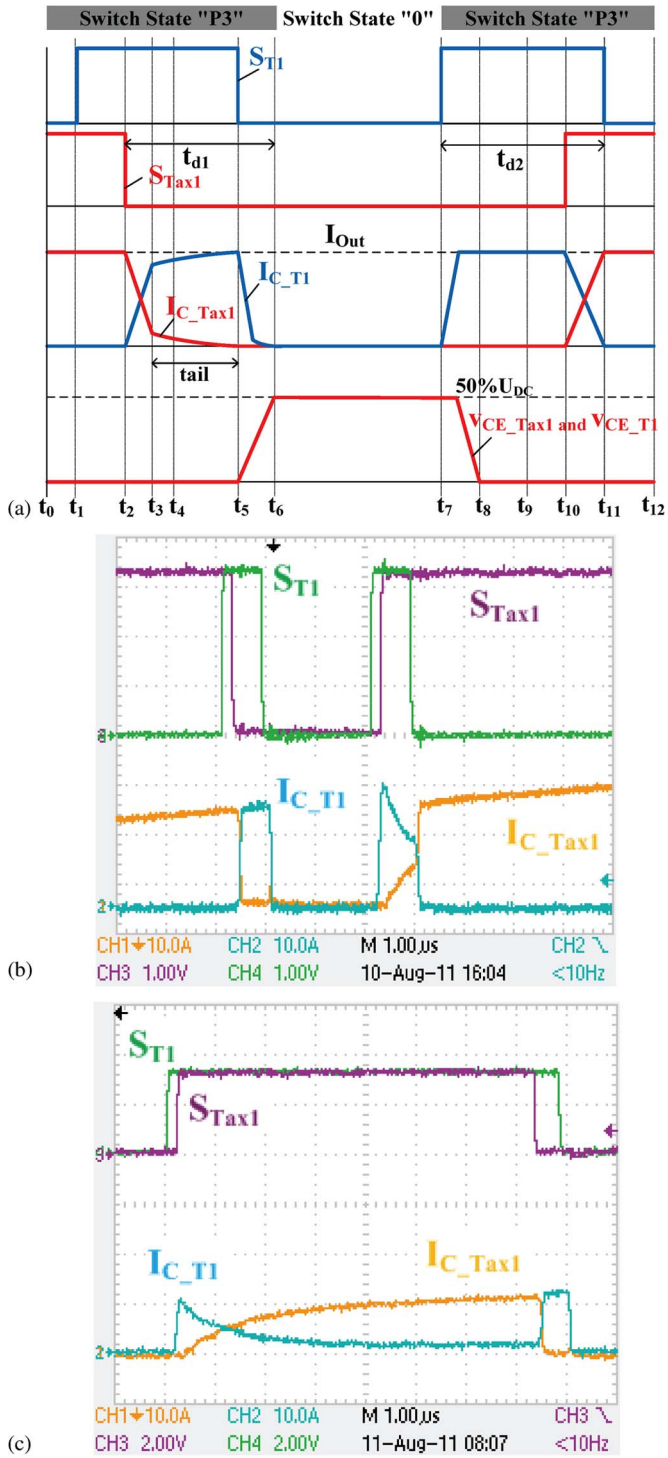

Fig. 10. Commutations (P3 $\leftrightarrow$ 0). (a) Ideal; (b) and (c) experimental waveforms for (P3 $\leftrightarrow$ 0). S_{T1} and S_{Tax1} are the switch commands for T_1 and T_{Ax1}, respectively. I_{C_T1} and I_{C_Tax1} are the collector currents of T_1 and T_{Ax1}, respectively. $V_{\mathrm{CE\_Tax1}}$ is the collector–emitter voltage across T_{Ax1}.

An alternative strategy to the loss-balancing control proposed in [4] is given in [16], where the calculations of the losses and device temperatures are performed offline for all relevant operation points, assuming a specific control and modulation strategy. Thus, the optimal ratio between the different types of commutations can be identified online as a function of the modulation index M and the operating power factor using a feedforward controller and a stored lookup table [16]. In this

TABLE II
DEVICE SWITCHING LOSSES IN THE THREE-LEVEL H-NPCC

Device	T_1	D_1	T_2	D_2	T_3	D_3	T_4	D_4	D_5	D_6	T_{Aux1}	T_{Aux2}	Commutation type
$I_{out}>0$													
(P1 ↔ 0)	X								X				Type 1
(P2 ↔ 0)									X		X		Type 2
(P3 ↔ 0)	X								X				Type 3
(N1 ↔ 0)			X					X					Type 4
(N2 ↔ 0)			X					X					Type 5
(N3 ↔ 0)			X					X					Type 6
$I_{out}<0$													
(P1 ↔ 0)		X			X								Type 1
(P2 ↔ 0)		X			X								Type 2
(P3 ↔ 0)		X			X								Type 3
(N1 ↔ 0)							X			X			Type 4
(N2 ↔ 0)										X		X	Type 5
(N3 ↔ 0)							X			X			Type 6

TABLE III
DECISION CHART FOR THE THREE-LEVEL H-NPCC

Commutation	Phase current	Junction temperatures		Operation
(P ↔ 0)	$I_{out}>0$	$\Delta T_{j\_T1}>\Delta T_{j\_T2}$	$\Delta T_{j\_T1}>\Delta T_{j\_Tax1}$	Ttype NPCC
			$\Delta T_{j\_T1}<\Delta T_{j\_Tax1}$	Conv. NPCC
		$\Delta T_{j\_T2}>\Delta T_{j\_T1}$	$\Delta T_{j\_T2}>\Delta T_{j\_Tax1}$	Ttype NPCC
			$\Delta T_{j\_T2}<\Delta T_{j\_Tax1}$	Conv. NPCC
	$I_{out}<0$	$\Delta T_{j\_T1}>\Delta T_{j\_T2}$		Type or NPCC
		$\Delta T_{j\_T2}>\Delta T_{j\_T1}$		Type or NPCC
(N ↔ 0)	$I_{out}>0$	$\Delta T_{j\_T4}>\Delta T_{j\_T3}$		Type or NPCC
		$\Delta T_{j\_T3}>\Delta T_{j\_T4}$		Type or NPCC
	$I_{out}<0$	$\Delta T_{j\_T4}>\Delta T_{j\_T3}$	$\Delta T_{j\_T4}>\Delta T_{j\_Tax2}$	Ttype NPCC
			$\Delta T_{j\_T4}<\Delta T_{j\_Tax2}$	Conv. NPCC
		$\Delta T_{j\_T3}>\Delta T_{j\_T4}$	$\Delta T_{j\_T3}>\Delta T_{j\_Tax2}$	Ttype NPCC
			$\Delta T_{j\_T3}<\Delta T_{j\_Tax2}$	Conv. NPCC

method, a substantially simplified implementation of the loss-balancing system can be achieved, as the complex real-time estimation of junction temperature is avoided. It is important to note that the efficiency of both loss-balancing schemes is strongly related to the operating switching frequency [18], [19].

C. H-NPCC With Five and Seven Levels

Multilevel VSCs, with loss-balancing control characteristics, can be derived from the proposed three-level H-NPCC version shown in Fig. 1(e). For example, Fig. 11(a) and (b) shows the five- and seven-level VSCs, respectively. Note that the blocking voltage of the auxiliary switches is always twice that of the conventional multilevel NPCCs.

IV. INVERTER SYSTEM COMPARATIVE EVALUATION

In order to quantify the feasibility of the proposed three-level H-NPCC, operating with the loss-minimized SVM or the conventional SPWM, an efficiency comparison between this system and other 10-kVA-rated three-phase inverters derived from the two-level VSC, the conventional NPCC, the T-type NPCC, and the A-NPCC is presented. Suitable commercial semiconductors are considered in the analysis (IGBTs IGW25T120 and

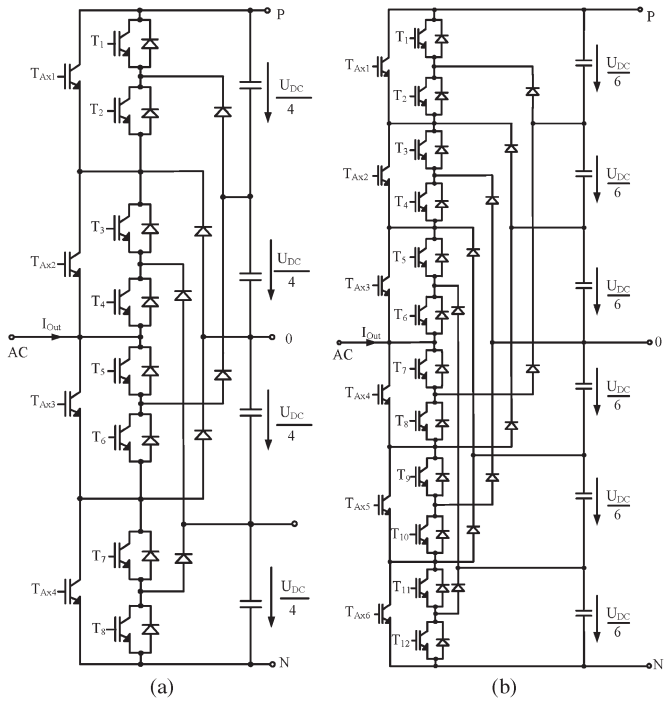

Fig. 11. Novel multilevel H-NPCCs: (a) Five- and (b) seven-level versions.

IKW30N60T), where the loss data are obtained with the test setup shown in Fig. 5. Note that, for an accurate analysis of the switching losses, the information from the datasheets only would not be enough to enable a fair comparison of the studied systems. Due to the mismatch of voltage-rated devices, e.g., during the T-type NPCC operation, the turn-on energy of the 1200-V IGBTs will be lower if the commutating diode is only 600 V rated because of the considerably lower reverse-recovery charge. Similarly, the 600-V-diode turn-off loss energy will be higher due to the commutating 1200-V IGBT.

For the three-level H-NPCC, the following two operation modes are considered in the analysis.

1) High-efficiency operation (mode 1): The losses of the system are distributed in such a way that the auxiliary switches T_{Ax1} and T_{Ax2} only display conduction losses while T_1 and T_4 are mainly stressed with switching losses.
2) Loss-balanced operation (mode 2): The operation mode, T-type NPCC or conventional NPCC, is defined by the real-time calculation of the junction temperatures of the switches following the algorithm presented in Table III.

In Fig. 12, the pure semiconductor efficiency of the inverters under study is shown for operation in the switching frequency range of 5–48 kHz and low dc-link voltage level ($U_{\rm dc} = 700$ V). The resulting averaged power loss of the individual elements in a phase leg for 48-kHz switching frequency is shown in Figs. 6 and 13.

The simulated junction temperatures for the three-level H-NPCC in mode 2 operating at 48 and 20 kHz with SPWM and SVM are shown in Figs. 14 and 15, respectively.

The H-NPCC, operating in mode 1, can always achieve the highest efficiency (cf. Fig. 12). This happens because this system suffers the lowest conduction and switching losses among all analyzed topologies. However, in contrast to the A-NPCC,

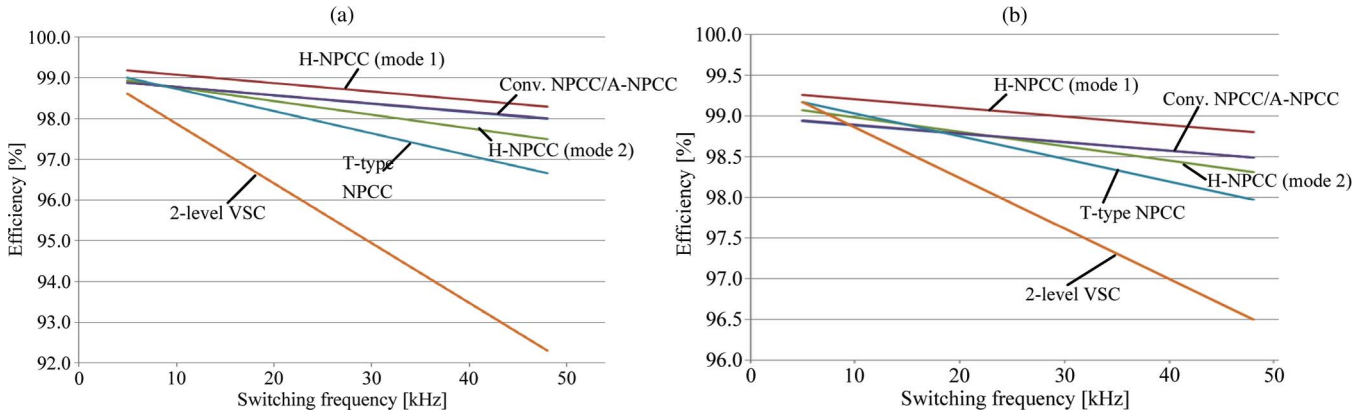

Fig. 12. Efficiency comparison between the different topologies of 10-kVA inverters employing commercial semiconductors (operation: unity power factor, fundamental output voltage peak $\hat{U}_{\mathrm{Out}} = 325$ V, and $\hat{I}_{\mathrm{Out}} = 20.5$ A). (a) SPWM. (b) SVM.

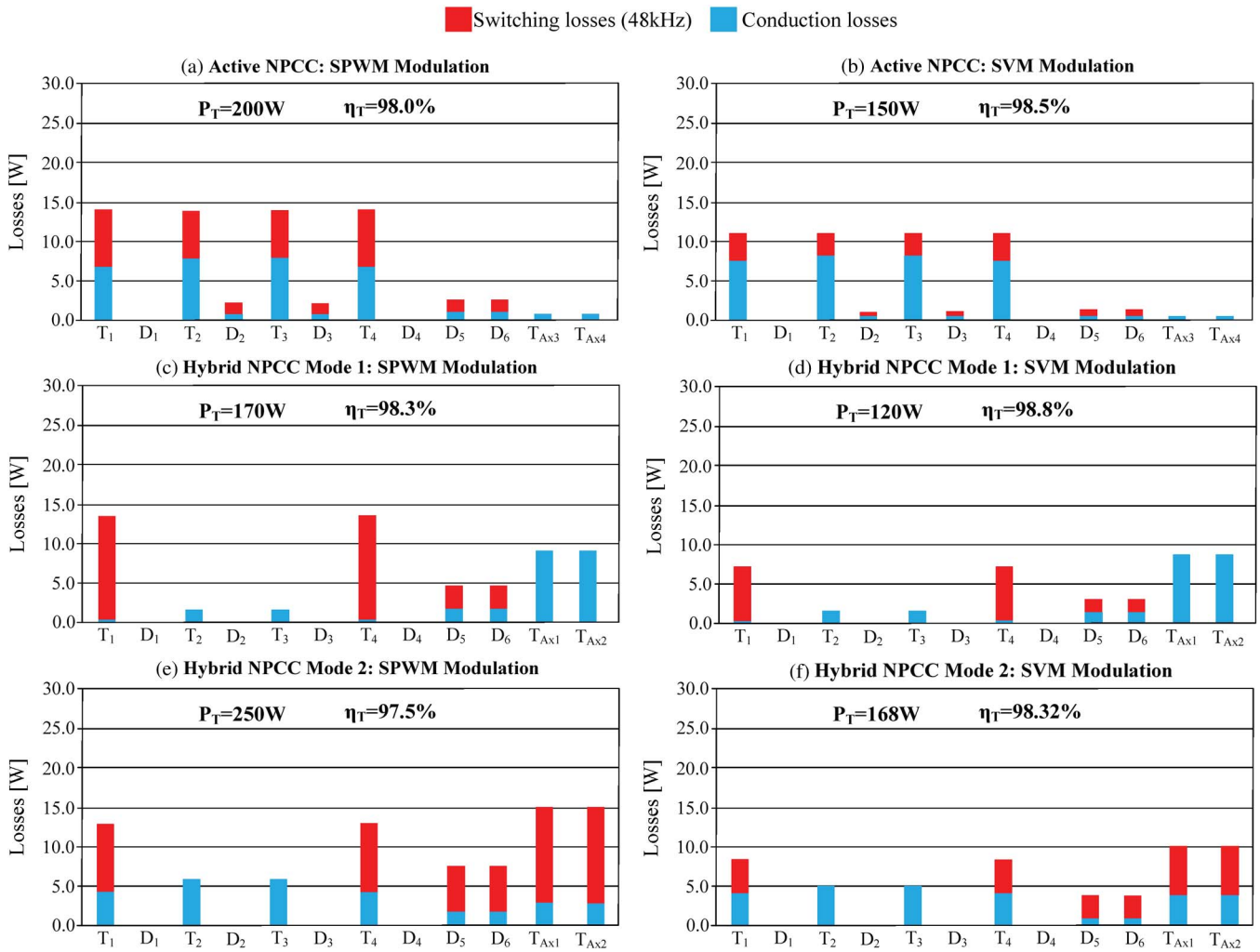

Fig. 13. Phase-leg component loss distribution. A-NPCC (a) SPWM and (b) SVM. H-NPCC mode 1 (c) SPWM and (d) SVM. H-NPCC mode 2 (e) SPWM and (f) SVM.

the power losses across the transistors T_1, T_2, T_3, and T_4 are not equalized (cf. Fig. 13).

As for the A-NPCC, a substantial improvement in the loss and junction temperature distribution across the devices of the phase leg can be achieved with the three-level H-NPCC. As can be seen in Fig. 12, the H-NPCC inverter in mode 2 only displays better efficiency than the A-NPCC for switching frequencies below 25 kHz for the SVM and below 8 kHz for the SPWM. Due to the fact that the A-NPCC cannot balance the losses across the auxiliary switches, a better thermal distribution among all the devices could be achieved with the new system. Note that the loss-balancing algorithm in Table III aims to

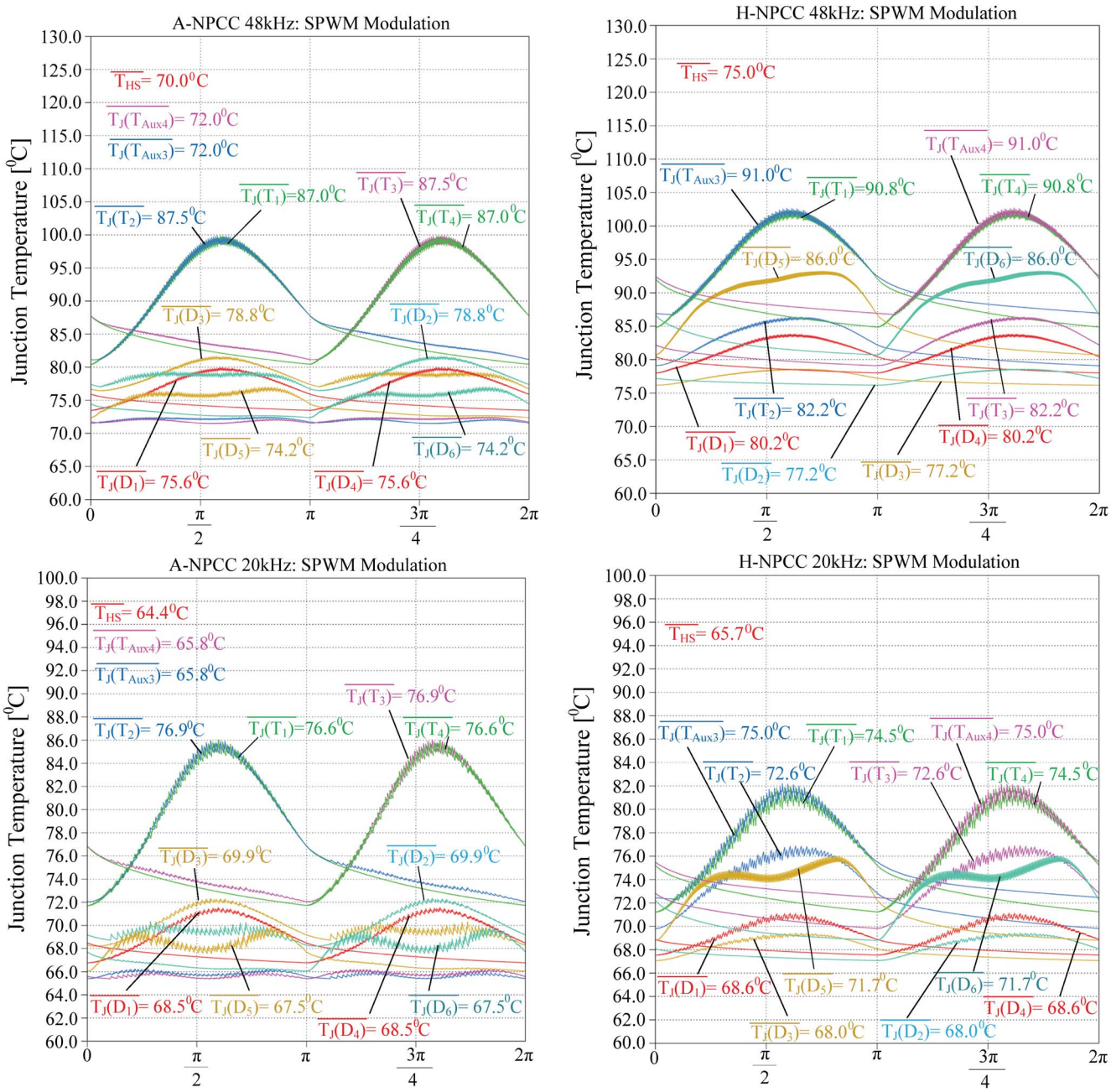

Fig. 14. Phase-leg component operating junction temperature for three-phase three-level inverters based on A-NPCC and H-NPCC operating with SPWM. Note that the averaged junction temperature of each device is given.

distribute the losses between T_1 and T_2 (T_3 and T_4), but it does not permit the auxiliary switches to be more thermally stressed than these devices. This is the reason that the junction temperatures across the NPCC switches are not even for the 48-kHz operation (cf. Figs. 14 and 15). On the other hand, for the 20-kHz operation, a much better performance is achieved. In fact, without the loss limitation of the auxiliary switches, the thermal profiles of the NPCC switches would be equalized; however, the auxiliary switches would face very high losses during high operating switching frequency.

From the results compiled in Fig. 12, it becomes clear that the main advantage of the H-NPCC over the conventional VSCs is the possibility to achieve higher efficiency. Therefore, in Sections IV-A and IV-B, the advantages of this operating condition are analyzed further, and analytical expressions for loss calculation of the H-NPCC (mode 1) showing the effects of the modulation index, the power factor, etc., are derived. The accuracy of the power loss is verified with the hardware shown in Fig. 5.

A. H-NPCC Mode 1: Analytical Model and Semiconductor Power Loss for SPWM

In order to analytically determine the losses of the semiconductors used in the conventional NPCC, the T-type NPCC, and the H-NPCC (mode 1), the current rms and average values of each device have to be calculated, and therefore, mathematical expressions are required. Herein, for each converter, simple expressions and means to calculate the semiconductor's power losses within a phase leg are given as functions of the

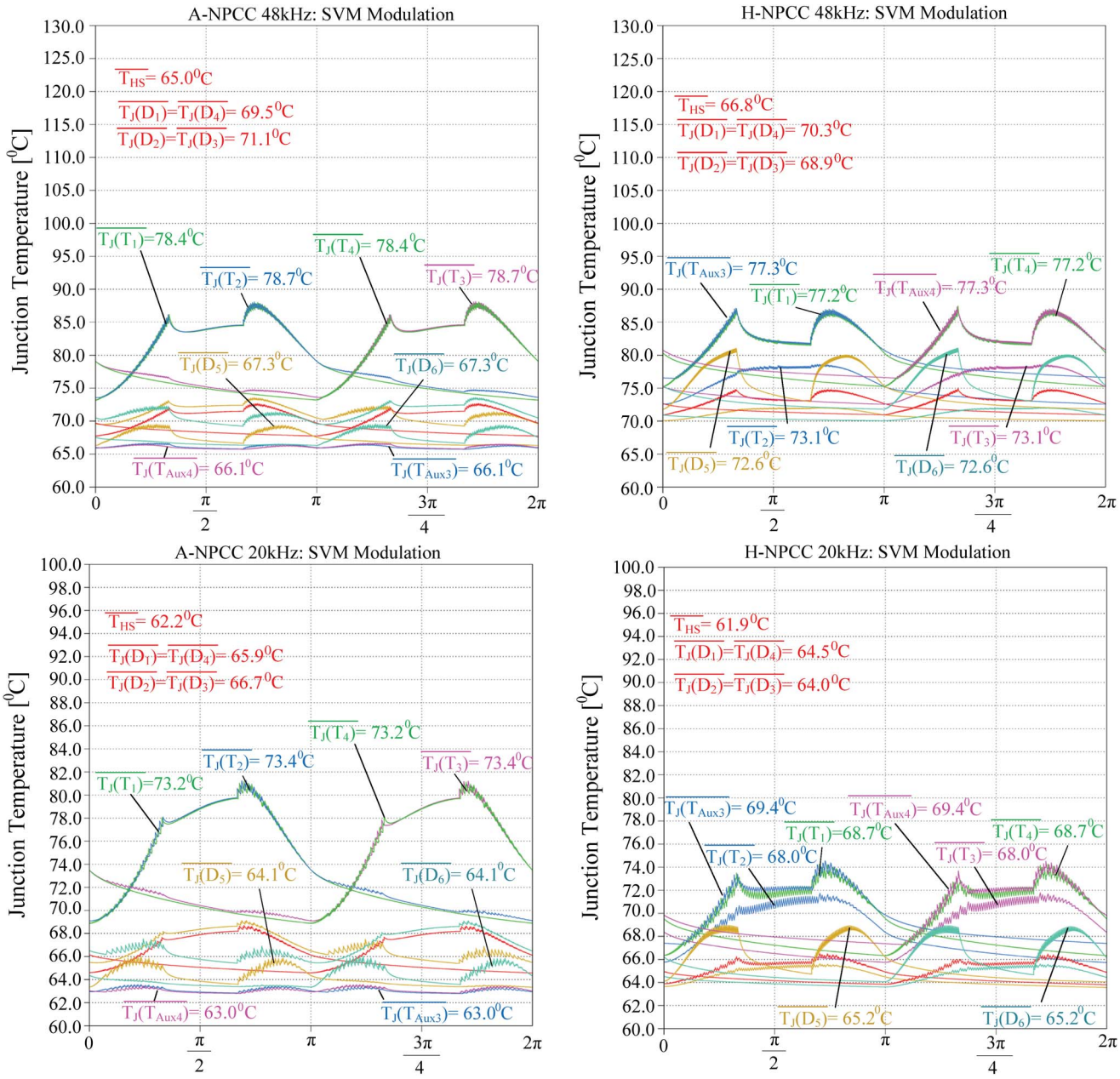

Fig. 15. Phase-leg component operating junction temperature for three-phase three-level inverters based on A-NPCC and H-NPCC operating with SVM.

modulation index M, the peak values of the ac terminal voltage $\hat{U}_{\mathrm{Out}}$ and current $\hat{I}_{\mathrm{Out}}$, the dc-link voltage level U_{dc}, and the phase shift between the ac terminal voltage and current φ_{vi}. The derived models are only valid for the conventional SPWM; however, for an in-depth description of the analytical model derivation for the loss-minimized SVM, the reader is referred to [20]. Additionally, for the real-time power loss calculations of the A-NPCC, see [4].

For the following calculations, it is assumed that the converter has a purely sinusoidal phase current shape and operates with a constant switching frequency being much higher than the mains frequency f_N ($f_s \gg f_N$).

1) Semiconductor Current Stresses: With a defined modulation index given by

$$M = \frac{2\hat{U}_{\mathrm{Out}}}{U_{\mathrm{dc}}} \tag{1}$$

the average and rms currents of the IGBTs and diodes forming a phase leg of the following converters are finally as follows.

1) Conventional NPCC

$$I_{T1/T4,\mathrm{avg}} = \frac{\hat{I}_{\mathrm{Out}} M \left[\sin(\varphi_{vi}) + (\pi - \varphi_{vi})\cos(\varphi_{vi})\right]}{4\pi} \tag{2}$$

$$I_{T1/T4,\mathrm{rms}} = \hat{I}_{\mathrm{Out}} \sqrt{\frac{M\left[1 + \cos^2(\varphi_{vi}) + 2\cos(\varphi_{vi})\right]}{6\pi}} \tag{3}$$

$$I_{T2/T3,\mathrm{avg}} = \hat{I}_{\mathrm{Out}} \left[\frac{1}{\pi} - \frac{M\left[\sin(\varphi_{vi}) - \varphi_{vi}\cos(\varphi_{vi})\right]}{4\pi}\right] \tag{4}$$

$$I_{T2/T3,\mathrm{rms}} = \hat{I}_{\mathrm{Out}}\sqrt{\frac{1}{4} - \frac{M\left(4\sin^2\left(\frac{\varphi_{vi}}{2}\right) - \sin^2(\varphi_{vi})\right)}{6\pi}} \quad (5)$$

$$I_{D1/D2/D3/D4,\mathrm{avg}} = \frac{\hat{I}_{\mathrm{Out}}M\left(\sin(\varphi_{vi}) - \varphi_{vi}\cos(\varphi_{vi})\right)}{4\pi} \quad (6)$$

$$I_{D1/D2/D3/D4,\mathrm{rms}} = \hat{I}_{\mathrm{Out}}\sqrt{\frac{M\left(4\sin^2\left(\frac{\varphi_{vi}}{2}\right) - \sin^2(\varphi_{vi})\right)}{6\pi}} \quad (7)$$

$$I_{D5/D6,\mathrm{avg}} = \frac{\hat{I}_{\mathrm{Out}}M\left(-2\sin(\varphi_{vi}) + (2\varphi_{vi} - \pi)\cos(\varphi_{vi}) + \frac{4}{M}\right)}{4\pi} \quad (8)$$

$$I_{D5/D6,\mathrm{rms}} = \hat{I}_{\mathrm{Out}}\sqrt{\frac{3\pi - 8M + 4M\sin^2(\varphi_{vi})}{12\pi}}. \quad (9)$$

2) T-type NPCC

$$I_{Tax1/Tax4,\mathrm{avg}} = \frac{\hat{I}_{\mathrm{Out}}M\left[\sin(\varphi_{vi}) + (\pi - \varphi_{vi})\cos(\varphi_{vi})\right]}{4\pi} \quad (10)$$

$$I_{Tax1/Tax4,\mathrm{rms}} = \hat{I}_{\mathrm{Out}}\sqrt{\frac{M\left[1 + \cos^2(\varphi_{vi}) + 2\cos(\varphi_{vi})\right]}{6\pi}} \quad (11)$$

$$I_{T2/T3D5/D6,\mathrm{avg}} = \frac{\hat{I}_{\mathrm{Out}}M\left(-2\sin(\varphi_{vi}) + (2\varphi_{vi} - \pi)\cos(\varphi_{vi}) + \frac{4}{M}\right)}{4\pi} \quad (12)$$

$$I_{T2/T3D5/D6,\mathrm{rms}} = \hat{I}_{\mathrm{Out}}\sqrt{\frac{3\pi - 8M + 4M\sin^2(\varphi_{vi})}{12\pi}} \quad (13)$$

$$I_{D1/D2/D3/D4,\mathrm{avg}} = \frac{\hat{I}_{\mathrm{Out}}M\left(\sin(\varphi_{vi}) - \varphi_{vi}\cos(\varphi_{vi})\right)}{4\pi} \quad (14)$$

$$I_{D1/D2/D3/D4,\mathrm{rms}} = \hat{I}_{\mathrm{Out}}\sqrt{\frac{M\left(4\sin^2\left(\frac{\varphi_{vi}}{2}\right) - \sin^2(\varphi_{vi})\right)}{6\pi}}. \quad (15)$$

3) H-NPCC in mode 1

Considering that T_1 and T_4 suffer conduction losses only during a time $t_d = t_{d1} + t_{d2}$ as shown in Fig. 10(a), (16)–(25), shown at the bottom of the page, model the rms and average values of each semiconductor of the H-NPCC operating in mode 1.

2) Semiconductor Power Losses: The conduction losses of the IGBTs and diodes of each converter can be approximated by

$$P_{T/D,c} = I^2_{T/D,\mathrm{rms}}\left[r_{T/D}(1 + a_r T_{J,T/D})\right] + I_{T/D,\mathrm{avg}}\left[V_{T/D}(1 + a_v T_{J,T/D})\right] \quad (26)$$

where $r_{T/D}$ and $V_{T/D}$ are the ON-state characteristics of the selected commercial power devices (IGBT/diode), while a_r and a_v are the fitting coefficients to adjust the values of $r_{T/D}$ and $V_{T/D}$ according to the semiconductor junction temperature $T_{J,T/D}$. $I_{T/D,\mathrm{avg}}$ and $I_{T/D,\mathrm{rms}}$ are obtained from (1)–(25).

$$I_{Tax1/Tax4,\mathrm{avg}} = \frac{\hat{I}_{\mathrm{Out}}M\left[\sin(\varphi_{vi}) + \left(\pi - \varphi_{vi} - \frac{2t_d f_s}{M}\right)\cos(\varphi_{vi}) - \frac{2t_d f_s}{M}\right]}{4\pi} \quad (16)$$

$$I_{Tax1/Tax4,\mathrm{rms}} = \hat{I}_{\mathrm{Out}}\sqrt{\frac{M\left[1 + \cos^2(\varphi_{vi}) + 2\cos(\varphi_{vi})\right]}{6\pi} - \frac{t_d f_s\left[\frac{\pi}{2} - \frac{\varphi_{vi}}{2} + \frac{\sin(2\varphi_{vi})}{4}\right]}{2\pi}} \quad (17)$$

$$I_{T1/T4,\mathrm{avg}} = \frac{\hat{I}_{\mathrm{Out}}t_d f_s\left(\cos(\varphi_{vi}) + 1\right)}{2\pi} \quad (18)$$

$$I_{T1/T4,\mathrm{rms}} = \hat{I}_{\mathrm{Out}}\sqrt{\frac{t_d f_s\left[\frac{\pi}{2} - \frac{\varphi_{vi}}{2} + \frac{\sin(2\varphi_{vi})}{4}\right]}{2\pi}} \quad (19)$$

$$I_{T2/T3,\mathrm{avg}} = \frac{\hat{I}_{\mathrm{Out}}\left[4 - 2M\sin(\varphi_{vi}) + 2t_d f_s + (2M\varphi_{vi} - \pi M + 2t_d f_s)\cos(\varphi_{vi})\right]}{4\pi} \quad (20)$$

$$I_{T2/T3,\mathrm{rms}} = \hat{I}_{\mathrm{Out}}\sqrt{\frac{6\pi + 8M\left(\sin^2(\varphi_{vi}) - 2\right) + f_s t_d\left(-6\varphi_{vi} + 3\sin(2\varphi_{vi}) + 6\pi\right)}{24\pi}} \quad (21)$$

$$I_{D5/D6,\mathrm{avg}} = \frac{\hat{I}_{\mathrm{Out}}M\left(-2\sin(\varphi_{vi}) + (2\varphi_{vi} - \pi)\cos(\varphi_{vi}) + \frac{4}{M}\right)}{4\pi} \quad (22)$$

$$I_{D5/D6,\mathrm{rms}} = \hat{I}_{\mathrm{Out}}\sqrt{\frac{3\pi - 8M + 4M\sin^2(\varphi_{vi})}{12\pi}} \quad (23)$$

$$I_{D1/D2/D3/D4,\mathrm{avg}} = \frac{\hat{I}_{\mathrm{Out}}M\left(\sin(\varphi_{vi}) - \varphi_{vi}\cos(\varphi_{vi})\right)}{4\pi} \quad (24)$$

$$I_{D1/D2/D3/D4,\mathrm{rms}} = \hat{I}_{\mathrm{Out}}\sqrt{\frac{M\left(4\sin^2\left(\frac{\varphi_{vi}}{2}\right) - \sin^2(\varphi_{vi})\right)}{6\pi}} \quad (25)$$

The switching losses of the IGBTs T_{Ax1}, T_{Ax2}, T_1, and T_4 and the diodes D_5 and D_6 can be calculated by (27), shown at the bottom of the page, where b_0, b_1, and b_2 correspond to the fitting coefficients which, for the IGBTs, model the turn-on and turn-off energies as functions of the forward current I_S and the applied reverse voltage U_B, e.g., $E_{T,\mathrm{ON+OFF}}(I_S, U_B, T_{J,T}) = b_0 + b_1 I_S + b_2 I_S^2$, and, for the diodes, model the reverse-recovery energy as a function of the forward current I_D of the diode and the applied reverse voltage U_B, e.g., $E_{rr}(I_D, U_B, T_{J,D}) = b_0 + b_1 I_D + b_2 I_D^2$. a_0, a_1, and a_2 are the fitting coefficients to adjust the values of b_0, b_1, and b_2 according to the semiconductor junction temperature $T_{J,T/D}$. The switching losses of the IGBTs T_2 and T_3 and the diodes D_1 and D_4 can be estimated by (28), shown at the bottom of the page. The diodes D_2 and D_3 do not suffer switching losses. Note that, for the H-NPCC in mode 1, the switching losses of T_{Ax1} and T_{Ax2} will be very small if t_d is set high enough and, thus, can be neglected (cf. Fig. 10).

Finally, the total averaged power loss of each semiconductor P_T can be determined using

$$P_T = P_{T/D,c} + P_{T/D,s}. \tag{29}$$

3) Power Loss Model Accuracy: In order to verify the accuracy of the derived power loss models, the single-phase hardware shown in Fig. 5 is set to operate as an inverter at 20 kHz with SPWM and the following specifications: $U_{\mathrm{dc}} = 700$ V, $\hat{I}_{\mathrm{Out}} = 10.0$ A/50 Hz, $0.5 < M < 0.95$, and $\varphi_{vi} \approx 3°$. The prototype losses for operation as the conventional NPCC, the T-type NPCC, and the H-NPCC (mode 1 with $t_d = 2$ μs) have been measured with a Yokogawa WT3000 precision power analyzer (basic power accuracy of 0.02%). The measurements were conducted with an RL load, where the value of the ac inductor was fixed ($L = 2$ mH) while the resistor value was varied to adjust the ac current amplitude for different modulation indices. Fig. 16 shows the calculated and measured semiconductor power losses as a function of the modulation index. The loss data used to compute the power losses of the utilized commercial semiconductors (IKW30N60T and IGW25T120) are presented in Table IV. Due to the fact that the power analyzer results include not only the semiconductor losses but also the circuit losses such as those from the printed circuit board tracks, inductors, and connections, these external loss quantities have to be predicted and subtracted from the measurements. As can be seen, the calculated semiconductor losses are slightly lower than those measured. The deviation can be explained by the approximate linear models of the conduction/switching losses or because of the prediction of the other circuit losses. In general, it can be seen that the loss results obtained by calculation correspond very well with those obtained by measurement, and therefore, (1)–(29) will be used in Section IV-B to compare the studied three-level VSCs for different operating points.

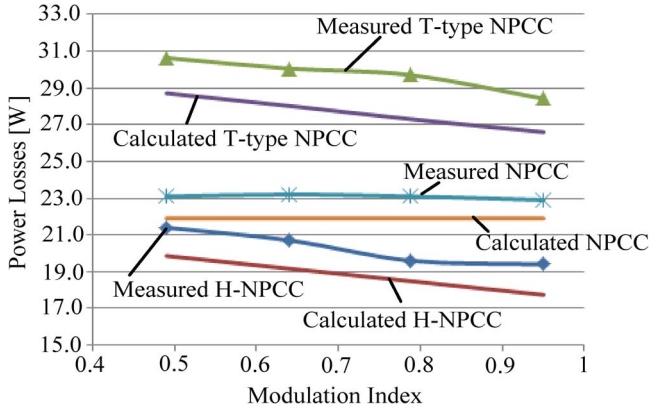

Fig. 16. Phase-leg semiconductor total power loss. Comparison between the calculated and the measured losses at $f_s = 20$ kHz, $U_{\mathrm{dc}} = 700$ V, and $\hat{I}_{\mathrm{Out}} = 10$ A.

TABLE IV
LOSS DATA FOR IKW30N60T AND IGW25T120

	1200 V IGBT	600 V IGBT	600 V Diode
Conduction Loss:	V_T=0.85V and r_T=48.7mΩ	V_T=0.85V and r_T=28.5mΩ	V_D=0.85V and r_D=21.7mΩ
Switching Loss I: $a_0 = a_1 = a_2 = 0$	U_b=600V, b_0=0, b_1=200.2µ, b_2=411.3n.	U_b=400V, b_0=0, b_1=60.2µ, b_2=48.3n.	U_b=400V, b_0=0, b_1=12.9µ, b_2=30.0n.
Switching Loss T-type Op.: $a_0 = a_1 = a_2 = 0$	U_b=600V, b_0=0, b_1=200.2µ, b_2=411.3n.	U_b=400V, b_0=0, b_1=60.2µ, b_2=48.3n.	U_b=400V, b_0=0, b_1=19.5µ, b_2=21.5n.
t_d	1µs	0	0

B. H-NPCC Mode 1: Extended Comparative Evaluation

In order to extend the comparison of the VSCs for different operating points, the analytical expressions (1)–(29) are used. The systems are compared according to the pure semiconductor efficiency achieved as functions of the modulation index and the phase shift between the ac terminal voltage and current (φ_{vi}), when a three-phase inverter operation is considered. These systems, rated to 10 kVA, are set to operate at 20-kHz switching frequency and the following specifications:

$$P_{T/D,s} = \left[\frac{\hat{I}_{\mathrm{Out}}^2 b_2 (1 + a_2 T_{J,T/D})}{4\pi} \left(\pi - \varphi_{vi} + \frac{1}{2}\sin(2\varphi_{vi}) \right) + \frac{\hat{I}_{\mathrm{Out}} b_1 (1 + a_1 T_{J,T/D}) (1 + \cos(\varphi_{vi})) - b_0 (1 + a_0 T_{J,T/D})(\varphi_{vi} - \pi)}{2\pi} \right] f_s \frac{\frac{1}{2} U_{\mathrm{dc}}}{U_B} \tag{27}$$

$$P_{T/D,s} = f_s \frac{\frac{1}{2} U_{\mathrm{dc}}}{U_B} \left[\frac{\hat{I}_{\mathrm{Out}}^2 b_2 (1 + a_2 T_{J,T/D})}{8\pi} (2\varphi_{vi} - \sin(2\varphi_{vi})) + \frac{\hat{I}_{\mathrm{Out}} b_1 (1 + a_1 T_{J,T/D})}{\pi} \sin^2\left(\frac{\varphi_{vi}}{2}\right) + \frac{b_0 (1 + a_0 T_{J,T/D}) \varphi_{vi}}{2\pi} \right] \tag{28}$$

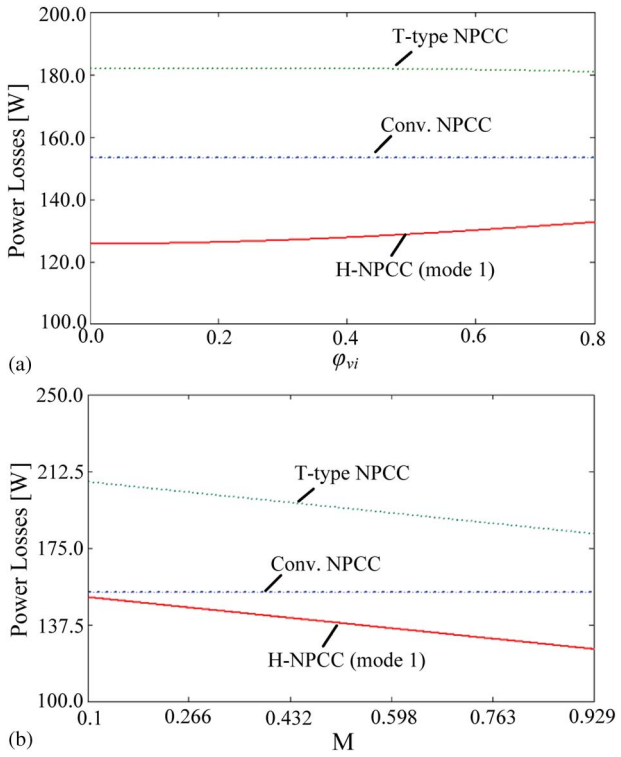

Fig. 17. Total semiconductor power loss for three-phase inverters as a function of (a) φ_{vi} (in radians) (at $M = 0.929$) and (b) M (at $\varphi_{vi} = 0°$). Operating conditions: $f_s = 20$ kHz, $U_{\rm dc} = 700$ V, and $\hat{I}_{\rm Out} = 20.5$ A.

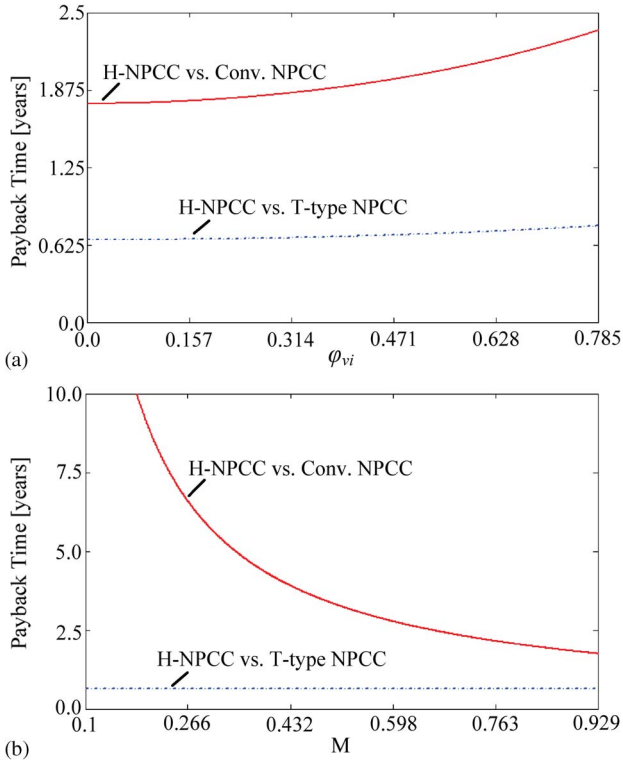

Fig. 18. Payback time in years as a function of (a) φ_{vi} (in radians) (at $M = 0.929$) and (b) M (at $\varphi_{vi} = 0°$). Operating conditions: $f_s = 20$ kHz, $U_{\rm dc} = 700$ V, and $\hat{I}_{\rm Out} = 20.5$ A.

$U_{\rm dc} = 700$ V, $\hat{I}_{\rm Out} = 20.5$ A/50 Hz, $0.1 < M < 0.929$ (at $\varphi_{vi} = 0°$), and $0° < \varphi_{vi} < 45°$ (at $M = 0.929$). The Infineon IGBTs 600-V IKW30N60T and 1200-V IGW25T120 are utilized for the assessment, and the coefficients given in Table IV model their power losses.

Fig. 17 shows the calculated power loss results. As can be seen, the H-NPCC in mode 1 is the solution which achieves the best performance for all analyzed operating points, particularly at high modulation index and unitary power factor ($\varphi_{vi} = 0°$).

Fig. 18 shows the payback time related to the additional cost of the auxiliary switches/gate driver incorporated to the NPCC and T-type NPCC and the energy cost reduction due to the power savings. The analysis considers the following: 24-h operation (365 days), U.K. energy cost of £0.07/kWh, costs of six IGW25T120 and six IKW30N60T IGBTs of £18.1 and £11.2, respectively, and gate driver cost of £12.0. As can be noted, the payback time for operation at $M > 0.6$ and/or $\varphi_{vi} < 45°$ is lower than 2.5 years, which is much less than the typical lifetime of a converter. Therefore, the implementation of a high-efficiency H-NPCC inverter is justified.

V. Chip-Area-Based Comparison

In the previous section, for the SPWM and the SVM, an efficiency comparison between three-phase inverters derived from the two-level VSC and many three-level structures employing commercial semiconductors was presented. As can be observed in Figs. 6 and 13, for a specific load and operating point, the three-level systems display very different loss distributions across the devices within the phase leg. Therefore, a pure efficiency comparison between them would not be absolutely reasonable as each system would display different reliability features. For a fair evaluation, the chip sizes of each system could be adapted for a given operating point such that the maximum or average IGBT and diode junction temperatures $T_{J,T/D}$ are equal to or less than a predefined maximum value, i.e., $T_{J,\max} = 125$ °C. This strategy not only guarantees optimal chip area partitioning and semiconductor material usage but also provides a common basis for comparisons [17]. Additionally, the chip area enables the semiconductor costs of the systems to be determined.

Due to their good documentation and data availability, the Infineon Trench and Field Stop 1200-V IGBT4 and 600-V IGBT3 series have been chosen as the data basis. With a statistical analysis of many commercial-device datasheets and manufacturer data, the chip die sizes $A_{S,T/D}$ depending on their current rating I_N are linearly fitted, and the resulting expressions are shown in [7], [17]

$$A_{S,\rm T1200V}(I_N) = 0.95\ \frac{\rm mm^2}{\rm A} I_N + 3.2\ \rm mm^2 \tag{30}$$

$$A_{S,\rm D1200V}(I_N) = 0.47\ \frac{\rm mm^2}{\rm A} I_N + 3.6\ \rm mm^2 \tag{31}$$

$$A_{S,\rm T600V}(I_N) = 0.55\ \frac{\rm mm^2}{\rm A} I_N - 0.32\ \rm mm^2 \tag{32}$$

$$A_{S,\rm D600V}(I_N) = 0.27\ \frac{\rm mm^2}{\rm A} I_N + 0.41\ \rm mm^2. \tag{33}$$

The IGBT and diode ON-state parameters, which are used to determine the semiconductor conduction losses, are modeled with nominal chip area $A_{N,T/D}$, forward voltage drop $U_{\rm CE/F}$, and differential resistance $R_{{\rm on},T/D}$. The resulting IGBT or

diode chip conduction losses P_{cond} can then be calculated according to

$$P_{\text{cond}}(A_{S,T/D}, i_{\text{avg}}, i_{\text{rms}}) = U_{\text{CE/F}} \cdot i_{\text{avg}} + \frac{R_{\text{on},T/D} \cdot A_{N,T/D}}{A_{S,T/D}} \cdot i_{\text{rms}}^2 \quad (34)$$

as a function of the average and rms currents which flow across the device, i.e., $i_{\text{avg/rms}}$.

For the switching loss energies $E_{\text{T/Don}}/E_{\text{T/Doff}}$, the datasheet values with the proposed gate resistors are linearly scaled to the same switched current i and commutating voltage u and proportionally fitted over the chip area $A_{S,T/D}$. In general, the switching losses scaled to the same current do not vary much with the chip size because a large chip is usually switched faster with a smaller gate resistor. The switching loss energy expressions for each component adapted to the area are presented in [7]

$$E_{\text{Ton},1200\,\text{V}}(A_{S,T}, u, i) = (-5.4 \cdot 10^{-10} \cdot A_{S,T} + 1.9 \cdot 10^{-7}) \cdot u \cdot i \quad (35)$$

$$E_{\text{Toff},1200\,\text{V}}(A_{S,T}, u, i) = (-4.3 \cdot 10^{-10} \cdot A_{S,T} + 2.1 \cdot 10^{-7}) \cdot u \cdot i \quad (36)$$

$$E_{D,1200\,\text{V}}(A_{S,D}, u, i) = (-1.6 \cdot 10^{-9} \cdot A_{S,D} + 1.2 \cdot 10^{-7}) \cdot u \cdot i \quad (37)$$

$$E_{\text{Ton},600\,\text{V}}(A_{S,T}, u, i) = (6.8 \cdot 10^{-10} \cdot A_{S,T} + 4.4 \cdot 10^{-8}) \cdot u \cdot i \quad (38)$$

$$E_{\text{Toff},600\,\text{V}}(A_{S,T}, u, i) = (3.1 \cdot 10^{-10} \cdot A_{S,T} + 5.7 \cdot 10^{-8}) \cdot u \cdot i \quad (39)$$

$$E_{D,600\,\text{V}}(A_{S,D}, u, i) = (9.3 \cdot 10^{-11} \cdot A_{S,D} + 2.7 \cdot 10^{-8}) \cdot u \cdot i. \quad (40)$$

By multiplying the energy loss by the switching frequency f_s, the IGBT/diode switching losses can be determined. For the T-type system analysis, the switching loss energy curves obtained from the datasheets are shifted proportionally to the point determined with the test setup shown in Fig. 5.

Finally, the thermal resistance from the junction to the heat sink $R_{\text{th,JS}}$ and the averaged junction temperature of each device T_J can be determined respectively by

$$R_{\text{th,JS}}(A_{S,T/D}) = 23.94 \, \frac{\text{K}}{\text{W} \cdot \text{mm}^2} \cdot A_{S,T/D}^{-0.88} \quad (41)$$

$$T_{J,T/D} = T_{\text{HS}} + R_{\text{th,JS}}(A_{S,T/D}) \cdot P_T(A_{S,T/D}). \quad (42)$$

In (41), the chip-area-dependent thermal resistance is derived based on manufacturer data for a standard power module assembly with a 3-mm Cu base plate and a 380-μm Al_2O_3 direct copper bonding (DCB) ceramic substrate and has been verified by thermal simulations [17].

In each cycle of the chip area optimization procedure proposed in [7], the conduction and switching loss model, including the thermal model of the bridge-leg semiconductors, has to be adapted according to the variation of chip area. An algorithm incorporating the studied modulation schemes is used to calculate the relative turn-on times/switching transitions of the components in one phase leg. In this manner, for each switching period, the averaged conduction and switching losses of the devices are determined for their new chip size. The optimization algorithm calculates the losses of each topology and the chip sizes until the average junction temperature of each semiconductor chip reaches $T_J = 125\,^{\circ}\text{C}$, assuming a heat sink temperature of $T_{\text{HS}} = 80\,^{\circ}\text{C}$. For the analysis, the chip area of each element is limited to a minimum of $A_{\text{Smin}} = 2\,\text{mm}^2$. This restriction is due to the limits in the bonding technology and also to prevent unconsidered side effects that become dominant in small chip sizes [7]. Finally, by summing up all optimized chip sizes, the total chip area, the semiconductor costs, the total efficiency for a topology, and the corresponding operation point can be found.

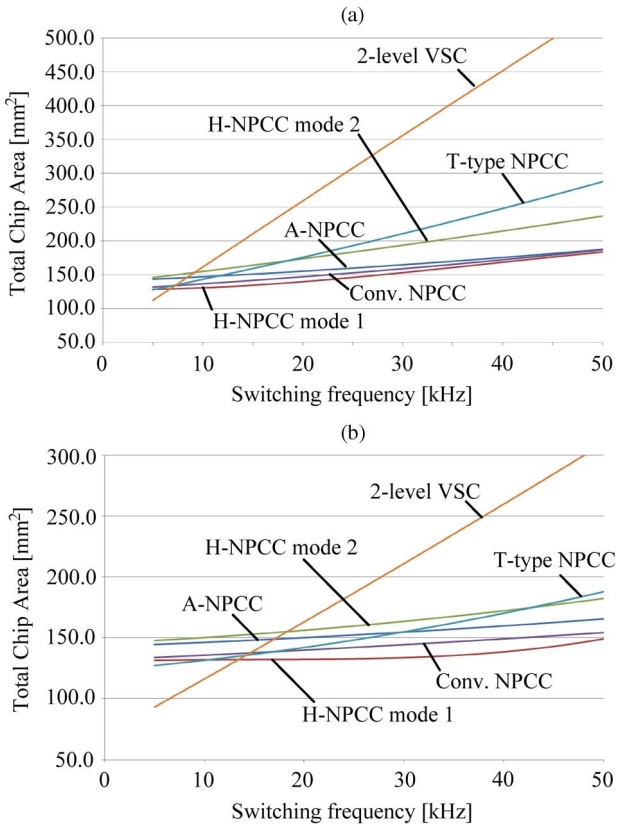

Fig. 19. Comparison of the total chip area usage depending on the frequency for inverter operation with (a) SPWM and (b) SVM.

The optimization results for all studied 10-kVA three-phase inverters operating with SPWM and SVM are shown in Fig. 19. For each system, the total chip area is calculated depending on the switching frequency.

As can be observed in Fig. 19, the total chip area of all three-level topologies is already lower than that of the two-level VSC for switching frequencies above 10 kHz for SPWM and 20 kHz for SVM. Under SPWM operation at 48 kHz, the necessary chip area of the two-level VSC is about three times larger than the area of the three-level H-NPCC (mode 1). For SVM at 48 kHz, the two-level system requires twice the area of the three-level H-NPCC (mode 1).

The increase in the required chip area with increasing switching frequency is the lowest for the three-level NPCC, A-NPCC, and H-NPCC (mode 1) because of the intrinsic small increase in switching losses. Interestingly, the loss distribution features of the three-level H-NPCC (mode 1) permit the minimum chip area limit of $A_{\text{Smin}} = 2\,\text{mm}^2$ to be reached for a large range of switching frequencies for most phase-leg devices.

It is important to point out that the chip area algorithm aims to equalize the average junction temperatures of all devices

of a phase leg. Therefore, the loss-balancing properties of the A-NPCC and the H-NPCC will not be essential. For the chip area comparison, mainly in low-switching-frequency operation, these topologies will commonly display worse results than the other three-level systems because of the extra chip area of their auxiliary semiconductors. However, the A-NPCC can display better performance than the conventional NPCC, if the considered switching frequency is high enough. Intrinsically, the A-NPCC operates distributing the switching losses among the outer and the inner devices; thus, the increment of the chip area in correlation to the switching frequency can be slightly reduced when compared with the conventional NPCC. This statement is also valid when comparing the H-NPCC with the T-type NPCC. Comparing both topologies with loss-balancing control, the H-NPCC (mode 2) will require less chip area than the A-NPCC only for very low switching frequencies.

Finally, this study shows that, among the analyzed inverter systems, the proposed three-level H-NPCC (mode 1) would already need the smallest silicon area for switching frequencies above 7 kHz with SPWM and 14 kHz with SVM. The part count is increased, but the total required chip area can be expressively smaller. This will definitely have a positive impact on the costs of an optimized three-level H-NPCC power module.

VI. Conclusion

This paper has presented several three-level VSC topologies, including the conventional NPCC, the A-NPCC, and various T-type systems. The problem of loss and junction temperature distribution across the semiconductors in the three-level NPCC and T-type VSCs has been investigated. An SVM scheme incorporating an optimal clamping of the phase has been proposed in order to maximize the efficiency of these typical three-level systems and/or to improve the distribution of the component losses, such that the variation of power/thermal cycling of the individual elements in a bridge leg is minimized.

A novel three-level H-NPCC has been introduced, where the switch states and commutations of the converter have been thoroughly analyzed. It has been shown that this new solution not only can achieve higher efficiency than many typical three-level structures but also can overcome their drawback of asymmetrical semiconductor loss distribution. Therefore, a remarkable increase of the converter output power capability and/or system reliability can be accomplished.

An efficiency comparison between the studied topologies for 10-kVA inverter operation in the switching frequency range of 5–48 kHz and low dc-link voltage level has been presented to demonstrate the performance and feasibility of the novel three-level VSC solution. Finally, a semiconductor-area-based comparison was used to further evaluate the studied three-level systems. Interestingly, at low dc-link voltage level, the total silicon chip area of the proposed three-level H-NPCC is already the smallest for switching frequencies above 8 kHz when considering SPWM and above 13 kHz for SVM.

References

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[2] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[3] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010.

[4] T. Brückner, S. Bernet, and H. Güldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, Jun. 2005.

[5] P. Lezana, J. Pou, T. A. Meynard, J. Rodriguez, S. Ceballos, and F. Richardeau, "Survey on fault operation on multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2207–2218, Jul. 2010.

[6] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low voltage drives, traction, and utility applications," *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 855–865, May 2005.

[7] M. Schweizer, I. Lizama, T. Friedli, and J. W. Kolar, "Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies," in *Proc. 36th Annu. IEEE IECON*, 2010, pp. 391–396.

[8] T. Soeiro, M. Schweizer, J. Linner, P. Ranstad, and J. W. Kolar, "Comparison of 2- and 3-level active filters with enhanced bridge-leg loss distribution," in *Proc. 8th Int. Conf. ECCE/ECCE*, 2011, pp. 1835–1845.

[9] A. Stupar, D. Bortis, U. Drofenik, and J. W. Kolar, "Advanced setup for thermal cycling of power modules following definable junction temperature profiles," in *Proc. IPEC*, Sapporo, Japan, 2010, pp. 962–969.

[10] T. Anzawa, Q. Yu, M. Yamagiwa, T. Shibutani, and M. Shiratori, "Power cycle fatigue reliability evaluation for power device using coupled electrical–thermal–mechanical analysis," in *Proc. ITHERM*, May 2008, pp. 815–821.

[11] T. Brückner and S. Bernet, "Loss balancing in three-level voltage source inverters applying active NPC switches," in *Proc. IEEE Power Electron. Spec. Conf.*, Vancouver, BC, Canada, 2001, pp. 1135–1140.

[12] T. Soeiro and J. W. Kolar, "Novel 3-level hybrid neutral-point-clamped converter," in *Proc. 37th IECON*, 2011.

[13] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[14] B. Kaku, I. Miyashita, and S. Sone, "Switching loss minimized space vector PWM method for IGBT three-level inverter," *Proc. Inst. Elect. Eng.—Elect. Power Appl.*, vol. 144, no. 3, pp. 182–190, May 1997.

[15] P. C. Loh, F. Blaabjerg, and C. P. Wong, "Comparative evaluation of pulsedwidth modulation strategies for z-source neutral-point- clamped inverter," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 1005–1013, May 2007.

[16] T. Brückner, S. Bernet, and P. K. Steimer, "Feedforward loss control of three-level active NPC converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 6, pp. 1588–1596, Nov./Dec. 2007.

[17] T. Friedli and J. W. Kolar, "A semiconductor area based assessment of AC motor drive converter topologies," in *Proc. 24th Annu. IEEE APEC*, Feb. 2009, pp. 336–342.

[18] J. Pereda and J. Dixon, "High-frequency link: A solution for using only one dc source in asymmetric cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3884–3892, Sep. 2011.

[19] D. A. B. Zambra, C. Rech, and J. R. Pinheiro, "Comparison of neutral-point-clamped, symmetrical, and hybrid asymmetrical multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2297–2306, Jul. 2010.

[20] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparison and implementation of a 3-level NPC voltage link back-to-back converter with SiC and Si diodes," in *Proc. 25th Annu. IEEE APEC*, Feb. 2010, pp. 1527–1533.

[21] [Online]. Available: www.digikey.com

[22] S. R. Pulikanti, M. S. A. Dahidah, and V. G. Agelidis, "Voltage balancing control of three-level active NPC converter using SHE-PWM," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 258–267, Jan. 2011.

[23] L. Jun, S. Bhattacharya, and A. Q. Huang, "A new nine-level active NPC (ANPC) converter for grid connection of large wind turbines for distributed generation," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 961–972, Mar. 2011.

[24] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, and R. Teodorescu, "Converter structure-based power loss and static thermal modeling of the press-pack IGBT three-level ANPC VSC applied to multi-MW wind turbines," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2505–2515, Dec. 2011.

[25] C. A. Silva, L. A. Cordova, P. Lezana, and L. Empringham, "Implementation and control of a hybrid multilevel converter with floating DC links for current waveform improvement," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2304–2312, Jun. 2011.

[26] A. Sanchez-Ruiz, M. Mazuela, S. Alvarez, G. Abad, and I. Baraia, "Medium voltage-high power converter topologies comparison procedure, for a 6.6 kV drive application using 4.5 kV IGBT modules," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1462–1476, Mar. 2012.

[27] S. Schroder, P. Tenca, T. Geyer, P. Soldi, L. J. Garces, R. Zhang, T. Toma, and P. Bordignon, "Modular high-power shunt-interleaved drive system: A realization up to 35 MW for oil and gas applications," *IEEE Trans. Ind. Appl.*, vol. 46, no. 2, pp. 821–830, Apr. 2010.

[28] L. Jun, A. Q. Huang, L. Zhigang, and S. Bhattacharya, "Analysis and design of active NPC (ANPC) inverters for fault-tolerant operation of high-power electrical drives," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 519–533, Feb. 2012.

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