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***Abstract*—Modern GaN and SiC power semiconductors require new experimental methods for determining switching losses as the widely accepted double-pulse-test (DPT) fails to accurately capture the dissipated energy during a switching transition because of electrical measurement limitations imposed by the very fast switching of WBG devices. In this paper, a new calorimetric measurement principle which relies on temperature rise monitoring of an aluminum heat sink during continuous operation of the attached power semiconductor is presented. Unlike traditional calorimetric methods, a single measurement can be performed in minutes. Using the proposed measurement principle, a soft-switching performance evaluation of selected $600\,\mathrm{V}$ GaN, SiC and Si power transistors is provided.**

***Index Terms*—WBG Power Semiconductor, Soft-Switching Losses, ZVS Losses, Calorimetric Measurement**

I. Introduction

Targeting maximal power density in kW-scale $400\,\mathrm{V}$ dc/ac converter systems and pushing the switching frequency above $1\,\mathrm{MHz}$, a good knowledge of soft-switching losses is crucial for an optimal design of the power electronic system. Since power semiconductor soft-switching losses are challenging to model mathematically [1] and very much depend on the employed gate-driver and PCB layout, typically empirical loss data obtained from experimental measurements with prototype hardware is used. A well known and widely accepted technique is the double-pulse test (DPT, [2]), where switching losses are calculated from electrical voltage and current measurements of the device during a turn-on and turn-off transient. Unfortunately, for fast switching transients in the ns-range which are typically achieved with WBG devices, the accuracy of the measured soft-switching losses is not satisfying [3]. Instead of measuring individual switching transients, the switching losses can be determined by measuring the average losses provided to the experimental setup during continuous operation without load and then subtract conduction losses and losses in the inductor, where the latter can be calculated [4] or measured calorimetrically [5]. Advantageously, the losses generated in the power semiconductors can also be measured directly as presented in [3], [6], where the temperature excursion of a heat sink attached to the power transistor is monitored. This calorimetric measurement principle is adopted and refined in this paper to characterize soft-switching losses of $600\,\mathrm{V}$ WBG power transistors and to compare them to the latest generation of $600\,\mathrm{V}$ Si superjunction MOSFETs. Since this study is motivated by the optimization of a high power density $400\,\mathrm{V}$ DC/AC converter system, solely power transistors which are available in a very low-inductance and compact surface-mount package were selected and both power transistors of a half-brdige are connected to a common heat sink to achieve a low-inductance layout.

II. Calorimetric Measurement Setup

The experimental setup consists of two power devices under test (DUT, T_1 & T_2) in half-bridge configuration and a LC output filter with filter capacitors connected to negative and positive DC rail as shown in Fig. 1 (a). The half-bridge is operated continuously with $50\,\%$ duty-cycle with symmetrical triangular current in the inductor (cf. Fig. 3 (c)). For given DC-link voltage, the switched current can be varied by means of altering the value of L ($2\,\mu\mathrm{H}$ – $20\,\mu\mathrm{H}$), keeping the switching frequency in the range of $0.8\,\mathrm{MHz}$ – $1.2\,\mathrm{MHz}$) for a high ratio of switching to total semiconductor loss, $P_{\mathrm{sw}}/(P_{\mathrm{sw}}+P_{\mathrm{c}})$. In order to achieve a low-inductance layout of the half-bridge, both power devices are attached to a common aluminum heat sink to extract the losses during continuous operation. Knowing the thermal behavior and parameters of the setup, the total power loss can be determined through monitoring the heat sink temperature. In order to minimize the thermal resistance between the DUT and the aluminum heat sink, the half-bridge is realized with an Insulated Metal Substrate (IMS) board as depicted in Fig. 1 (b). Since the temperature rise of the heat sink characterizes the total impressed losses, it is essential to minimize any transfer of heat to the ambient by means of thermal insulation of the power stage and the aluminum heat sink as illustrated in Fig. 1 (c). Since (i) the gate drive and digital control board are located outside of the insulation box and (ii) power board (IMS) and gate drive PCB are physically separated except for short copper wires connecting the gate contacts (cf. Fig. 1 (b)), the contribution of gate drive and auxiliary power loss to the temperature rise of the heat sink is negligible.

A. Transient Calorimetric Measurement

Although calorimetric approaches offer several advantages over electrical switching loss measurements, often temperature readings at thermal equilibrium are needed. This results in (i) a long total measurement time and (ii) deflects the operating temperature of the DUT over a wide range during the

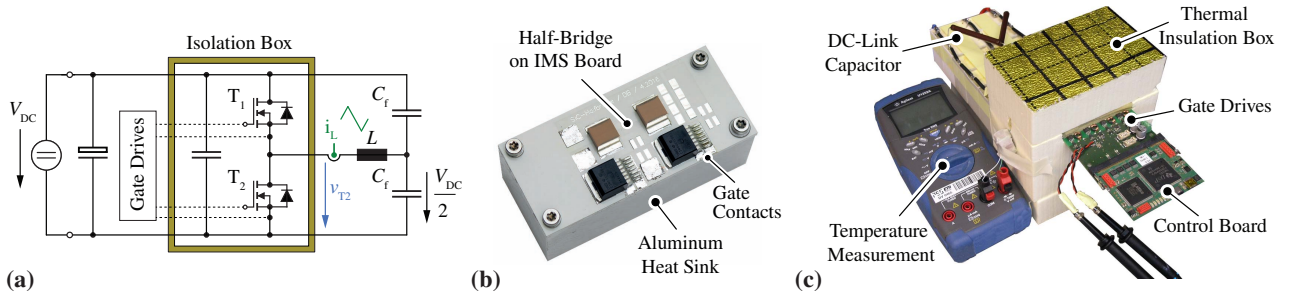

Fig. 1. **(a)** Circuit diagram of the experimental setup with two power devices under test (T_1, T_2) in half-bridge arrangement and connected LC output filter. Both power devices are attached to a common aluminum heat sink to extract the losses. **(b)** The power PCB is realized with a single-layer Insulated Metal Substrate (IMS) board to achieve a low thermal resistance between the DUT and the heat sink. **(c)** The power stage and the attached aluminum block (heat sink) are thermally insulated to the ambient. Gate drive and digital control board are located outside of the insulation box.

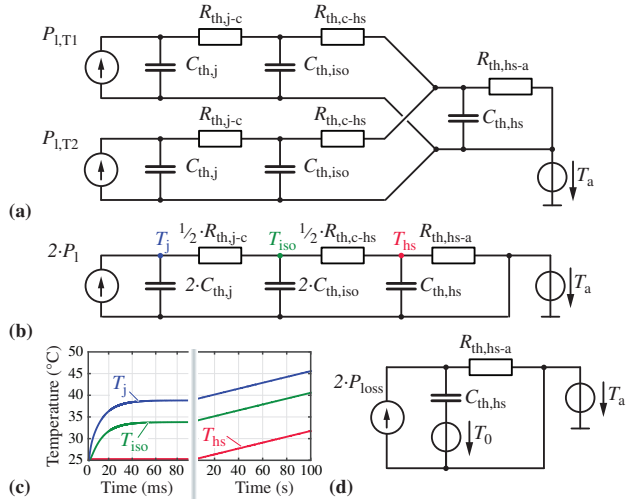

Fig. 2. **(a)** Thermal equivalent circuit (Cauer RC network) of the experimental setup assuming a 1-D heat flux. **(b)** Simplification due to symmetry of the setup. **(c)-(d)** Further simplification of the thermal network by neglecting the RC filter stages with comparably small time constant.

measurements. On the contrary, in the transient calorimetric measurment approach proposed in this paper, the heat sink temperature excursion is always kept between 30 °C to 40 °C and the elapsed time to reach 40 °C differs depending on the impressed power losses. Neglecting lateral heat spreading (1-D heat flow) and assuming uniform heat sink temperature, the circuit shown in Fig. 2 (a) models the thermal behavior of the experimental setup. The thermal properties of the power transistor are approximated with $C_{\mathrm{th,j}}$ and $R_{\mathrm{th,j-c}}$. The prepreg insulation layer of the IMS board between top-side copper layer and aluminum substrate is taken into consideration with $C_{\mathrm{th,iso}}$ and $R_{\mathrm{th,c-hs}}$. The thermal capacitance of the aluminum substrate and the attached large aluminum block are modeled with $C_{\mathrm{th,hs}}$. The thermal resistance to the ambient, kept as large as possible by means of the insulation box, is represented with $R_{\mathrm{th,hs-a}}$. The thermal interface formed by solder and copper layer is neglected, assuming that the temperature of the copper layer and the prepreg layer are identical (T_{iso}). Due to the symmetry of the setup, the thermal circuit can be simplified as shown Fig. 2 (b). The thermal time constants of the first two filter stages (power transistor and prepreg layer) are much smaller compared to the filter stage formed by the aluminum block and thermal resistance to ambient as listed in Tab. II-A. The simulated temperature response as a function of time at the respective thermal interfaces due to a power step of $2 \cdot P_{\mathrm{l}} = 20\,\mathrm{W}$ at $t = 0\,\mathrm{s}$ is illustrated in Fig. 2 (c), showing a settling of T_{j} and T_{iso} already after $t \approx 80\,\mathrm{ms}$, whereas T_{hs} has virtually not changed. Hence, if the continuous operation of the half-bridge is initiated prior to the beginning of the temperature recording such that the fast thermal transients have already settled, then the thermal behavior of the experimental system can be simplified to a first order system as shown in Fig. 2 (d) with initial heat sink temperature $T_{\mathrm{hs}}(t=0) = T_0$. Now, for a stepwise increase of the impressed power, $p(t) = \sigma(t) \cdot P_{\mathrm{l}}$, the heat sink temperature increases according to

$$T_{\mathrm{hs}}(t) = R_{\mathrm{th}} P_{\mathrm{l}} + (T_0 - R_{\mathrm{th}} P_{\mathrm{l}}) \cdot \mathrm{e}^{-\frac{t}{R_{\mathrm{th}} C_{\mathrm{th}}}}. \qquad (1)$$

The thermal parameters of the experimental setup, $C_{\mathrm{th}} = C_{\mathrm{th,hs}}$ and $R_{\mathrm{th}} = R_{\mathrm{th,h-a}}$, are identified by means of a least-mean-square (LMS) regression,

$$\min_{R,C} \sum_{k=1}^{N} \left\| \left(R P_{\mathrm{l,k}} + (T_{0,\mathrm{k}} - R P_{\mathrm{l,k}}) \cdot \mathrm{e}^{-\frac{t}{RC}} \right) - T_{\mathrm{hs,k}} \right\|^2, \qquad (2)$$

with experimental data obtained from N distinct calibration measurements with known power dissipation $P_{\mathrm{l,k}}$ as illustrated in Fig. 3 (a). During a calibration measurement, both power transistors are kept in the on-state and a constant current I_{s} is forced through the transistors (DUT) and the connecting PCB tracks by means of a laboratory power supply operating in constant current mode. Varying I_{s} allows to adjust the dissipated power,

$$p(t) = v_{\mathrm{cal}}(t) I_s = 2 \left(R_{\mathrm{DS,on}}(T_{\mathrm{j}}) + R_{\mathrm{PCB}}(T_{\mathrm{iso}}) \right) I_{\mathrm{S}}^2, \qquad (3)$$

with the instantaneous voltage drop $v_{\mathrm{cal}}(t)$ across the conduction path as indicated in Fig. 3 (b). Since the on-state resistance of the DUT is strongly dependent on the operating temperature, the dissipated power is slightly increasing throughout the calibration measurements although current I_{s} (cf. Fig. 3 (b)) is kept constant. For the LMS regression (2), the average power

TABLE I
TECHNICAL SPECIFICATIONS AND THERMAL PARAMETERS OF THE EXPERIMENTAL SETUP

Aluminum Block (Heat Sink)		IMS Board		Thermal Parameters			
Dimension	$(30 \times 70 \times 50)$ mm^3	Dimension	$(30 \times 70 \times 1.65)$ mm^3	$R_{\mathrm{th,j-c}}$	0.49 K/W [i]	$C_{\mathrm{th,j}}$	0.0035 J/K [i]
Weight	0.28 kg	Alu/Prepreg thk.	1.5/0.1 mm	$R_{\mathrm{th,c-hs}}$	0.88 K/W [ii]	$C_{\mathrm{th,iso}}$	0.01 J/K [ii]
$C_{\mathrm{th,block}}$	262 J/K	$C_{\mathrm{th,core}}$	7.6 J/K	$R_{\mathrm{th,hs-a}}$	18.8 K/W [iii]	$C_{\mathrm{th,hs}}$	292.6 J/K [iii]

[i] Approximation of the thermal properties of power transistor specimen B (cf. Tab. II)
[ii] Considering chip size are of specimen B (10.05 mm × 8.68 mm) and thermal properties of the prepreg layer (FR4, $\lambda = 1.3$ W K/m, $\rho = 1.91$ g/cm^3, $c_{\mathrm{th}} = 0.6$ J K/g)
[iii] Empirically determined by means of LMS regression to measurement data (cf. Fig. 3)

over the course of the k^{th} calibration measurement,

$$P_{\mathrm{l,k}} = \overline{p_{\mathrm{k}}(t)} = \frac{1}{T_{\mathrm{cal,k}}} \int_{t|_{T_{\mathrm{hs,k}}=40\,^{\circ}\mathrm{C}}}^{t|_{T_{\mathrm{hs,k}}=30\,^{\circ}\mathrm{C}}} v_{\mathrm{cal,k}} \cdot I_{\mathrm{s,k}}\, \mathrm{d}t, \quad (4)$$

$$T_{\mathrm{cal,k}} = t|_{T_{\mathrm{hs,k}}=40\,^{\circ}\mathrm{C}} - t|_{T_{\mathrm{hs,k}}=30\,^{\circ}\mathrm{C}}, \quad (5)$$

is considered. Moreover, the average resistance of the conduction path, valid for a heat sink temperature excursion between 30 °C – 40 °C is given by

$$R_{\mathrm{c,tot,k}}(P_{\mathrm{l,k}}) = \frac{P_{\mathrm{l,k}}}{I^2_{\mathrm{S,k}}}, \quad (6)$$

and will be needed to deduct conduction losses as discussed in the section below. Once the thermal system has been identified, the total power dissipation in the half-bridge, i. e. the sum of conduction and switching losses, during regular operation of the setup, can then be obtained by solving the LMS regression,

$$\min_{P} \left\| \left(R_{\mathrm{th}} \cdot P + (T_0 - R_{\mathrm{th}} \cdot P) \cdot \mathrm{e}^{-\frac{t}{R_{\mathrm{th}} C_{\mathrm{th}}}} \right) - T_{\mathrm{hs}} \right\|^2 . \quad (7)$$

B. Switching Loss Extraction

By means of the presented transient temperature measurement approach, the total power loss in the half-bridge i. e. DUT, can be determined with high accuracy. In order to extract the switching losses of the DUT, the conduction losses must be subtracted from the total power loss. In this paper, the conduction losses are calculated numerically according to,

$$P_{\mathrm{l,c}} = R_{\mathrm{c,tot}}(P_{\mathrm{l}}) I^2_{\mathrm{DUT}}. \quad (8)$$

The total resistance of the conduction path as a function of power, $R_{\mathrm{c,tot}}$, is obtained from a polynomial fit to $\{R_{\mathrm{c,tot,1}}, \ldots R_{\mathrm{c,tot,N}}\}$, the result of (4) for the N preceding calibration measurements. The RMS value of the power transistor current, $I_{\mathrm{DUT}} = I_{\mathrm{T,1}} = I_{\mathrm{T,2}}$ due to symmetry, is given by

$$I_{\mathrm{DUT}} = \sqrt{\left(\frac{1}{2} - \frac{t_{\mathrm{d}}}{T_{\mathrm{s}}} \right) \frac{I^2_{\mathrm{sw}}}{3}}, \quad (9)$$

wherein the prevailing current in the inductor at the instant of switching I_{sw}, the adjusted dead-time t_{d} and PWM period T_{s}, illustrated in Fig. 3 (c), are obtained from measurement of i_{L} and the applied gate signals. Depending on the operating point defined by the applied DC-link voltage and the switched current level, the dead-time of the half-bridge t_{d}, is adjusted

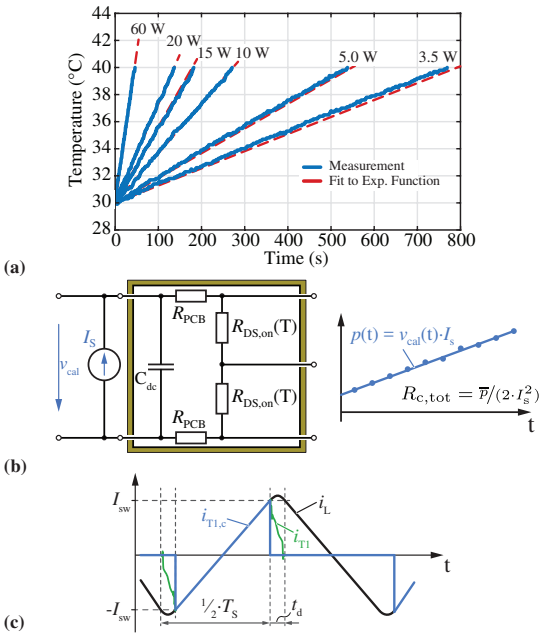

Fig. 3. **(a)** Change of the heat sink temperature over time due to the impressed power loss of the half-bridge i. e. DUT. **(b)** Impressed power during calibration measurements and extraction of the temperature dependent conduction path resistance $R_{\mathrm{c,tot}}$. **(c)** RMS calculation of the transistor current from i_{L} and gate-control timings.

such that the resonant transition for Zero Voltage Switching (ZVS) is completed but the conduction time of the anti-parallel diode is kept at a minimum. Typically, t_{d} is just a small fraction of the PWM period and the conduction losses caused by the copper tracks of the IMS board during the dead-time interval are negligible compared to the switching losses (cf. $i_{\mathrm{T1,c}}$ and i_{T1} in Fig. 3 (c)).

III. SOFT-SWITCHING BENCHMARK

The proposed measurement technique was applied for a soft-switching performance evaluation of selected GaN and SiC power transistors and a comparison of the WBG devices to the latest generation of superjunction Si MOSFETs. As listed in Tab. II, 600 V devices (except for SiC specimen C) with an on-state resistance in the range of 50 mΩ – 65 mΩ were selected for the benchmark. The employed gate drive circuits have been designed according to the specific driving requirements of the individual power devices and technical details are listed in Tab. II. Additional free-wheeling SiC diodes (C3D1P7060Q) were connected in parallel to the selected

TABLE II
SELECTED POWER SEMICONDUCTORS AND TECHNICAL DETAILS

Type / Specimen	$V_{ds,max}$	$R_{ds,on}$	$R_{g,int}$	Q_{tot}	C_{oss} [i]	Package	Gate-Drive IC	V_{gs}	$R_{g,on/off}$
GaN GIT / A	600 V	55 mΩ	5.3 Ω	-	100 pF	ThinPAK 8x8	LM5114	+3.5/-6.5 V	5/0 Ω [ii]
GaN E-HEMT / B	650 V	50 mΩ	1.3 Ω	5.8 nC	65 pF	GaN*PX*^{TM}	LM5114	+5/-5 V	5/5 Ω
SiC MOSFET / C	900 V	65 mΩ	4.7 Ω	30.4 nC	80 pF	7LD2PAK	UCC27531	+15/-5 V	0/0 Ω
Si MOSFET / E	600 V	65 mΩ	0.8 Ω	68.0 nC	54 pF	ThinPAK 8x8	UCC27531	+15/-5 V	2.5/2.5 Ω

[i] According to datasheet at 400 V drain-source voltage [ii] See [5] regarding details of the GaN GIT gate drive

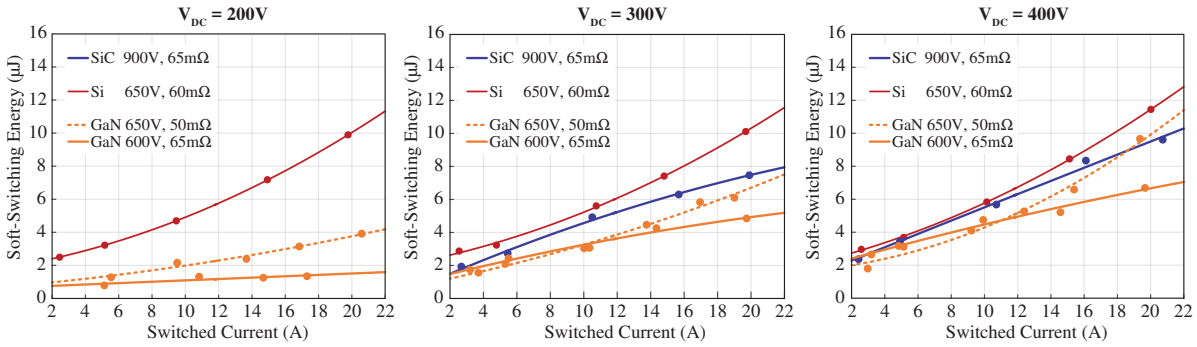

Fig. 4. Soft-switching energy dissipation (µJ) per transistor of selected SiC, GaN and Si power semiconductors in half-bridge arrangement for switched currents in the range of 2 A – 22 A and DC-link voltages of 200 V, 300 V and 400 V. The measurement error is less than ±15 %.

GaN power transistors. The experimental results obtained for the considered power devices in half-bridge arrangement are given in Fig. 4, showing the energy dissipation in µJ per power transistor caused by a soft-switching transition (ZVS) for a device current I_{sw}. The expected measurement error was calculated to be less than ±15 % in a worst case consideration. It can be clearly seen that the selected GaN power devices are leading the benchmark. In particular specimen A features the lowest energy dissipation of 2 µJ – 7 µJ at 400 V DC-link voltage. The 900 V SiC device, specimen C, exhibits a slightly higher energy dissipation close to 10 µJ at the max. switched current. Interestingly, the performance of the tested 600 V, 7th-generation Si MOSFET, specimen E, exhibits a soft-switching performance very similar to the tested WBG devices. In case of the Si MOSFET, the remaining soft-switching losses can be attributed to a distinctive hysteresis in the output capacitance, i. e. a lossy charging of C_{oss}, as described in [7]. However, for the GaN and SiC power transistors further investigations are needed to identify the physical origin of the remaining soft-switching losses.

IV. CONCLUSION

In this paper a new transient calorimetric measurement technique to accurately determine the soft-switching losses of fast switching power semiconductors is presented. The method, based on heat sink temperature rise monitoring, allows to quickly (1 min – 15 min per measurement depending on operating point) and accurately (±15 % error) determine the soft-switching losses of power transistors in half-bridge arrangement. Applying the proposed measurement principle, a soft-switching benchmark of selected 600 V GaN, SiC and superjunction Si devices with low-inductacne SMD packages and similar on-state resistance was performed. The experimental results revealed that at 400 V DC-link voltage and switched currents in the range of 2 A – 20 A, the selected power transistors exhibit an energy dissipation in the range of 2 µJ – 12 µJ, whereby the tested GaN GIT showed the best performance. The tested 600 V Si superjunction MOSFET showed a soft-switching performance comparable to the 900 V SiC MOSFET. It is the topic of ongoing research to identify the origin of this remaining switching losses, as simulation results confirm that they can not be attributed to deficiencies in the gate driving of the power transistors or circuit layout.

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