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***Abstract*—In this paper, a three-phase buck-type unity power factor rectifier is designed for high-power electric vehicle battery charging mains interfaces. The characteristics of the converter, named the SWISS Rectifier (SR), including the principle of operation, modulation strategy, suitable control structure, and dimensioning equations are described in detail. Exemplarily, a 7.5 kW hardware prototype is then designed based on the derived analytical expressions and the feasibility of the SR concept is demonstrated by the means of experimental measurements. Finally, the SR is compared with a conventional six-switch buck-type ac–dc power conversion. According to the results, the SR is the topology of choice for a buck-type PFC.**

***Index Terms*—Active third harmonic current injection, buck-type PFC converter, rectifier systems.**

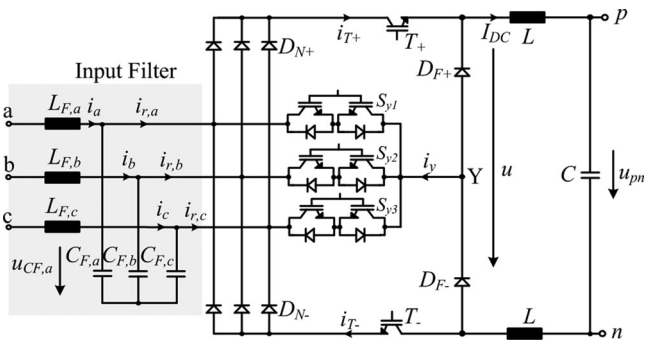

Fig. 1. Circuit topology of the three-phase SR with *LC* input filter.

I. Introduction

CHARGING of electric vehicle (EV) batteries inherently requires conversion of energy from the ac mains into dc quantities. Several charging voltage and power levels have been defined by different standardization organizations (IEC 61851, IEC62196, SAE J1772). Single-phase power factor corrector (PFC) mains interfaces are commonly employed for low-charging power levels (e.g., $P < 5$ kW), whereas for higher power levels, three-phase PFC mains interfaces have to be applied [1]. The EV chargers, typically implemented as two-stage systems, i.e., comprising a PFC rectifier input stage followed by a dc–dc converter, can be either integrated into the car (on-board) or accommodated in specially designed EV charging stations (off-board) [2].

In the particular case of fast charging stations (off-board), the power electronic system should be able to guarantee voltage adaptation to cope with the different specifications of several types of vehicles. Typically, for three-phase 400 or 480 V (line-to-line *rms* voltage) ac mains, EV chargers with a dc-bus voltage in the range of 250 to 450 V are used [1].

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Buck-type three-phase PFC rectifiers are appropriate for high-power EV chargers (>5 kW), as a direct connection to the dc-bus can be used. If isolation of the dc-bus from the PFC rectifier is required for safety reasons, this can be facilitated by an isolated dc–dc converter connected in series, which can additionally be used for voltage regulation. Compared to boost-type topologies, buck-type systems provide a wider output voltage control range, while maintaining PFC capability at the input. Additionally, they enable direct start-up, and allow for dynamic current limitation at the output [3]–[12]. Three-phase boost rectifiers produce an output voltage (typ. 700 to 800 V) that is too high to directly feed the dc-bus of EVs and thus require a step-down dc–dc converter at their output.

This paper presents the design and implementation of a three-phase buck-type PFC rectifier topology, referred to as the SWISS Rectifier (SR) (cf., Fig. 1), appropriate for high-power EV battery charging systems. As it will be shown, this rectifier technology not only has similar operating characteristics as standard buck-type ac–dc converters, but it can also achieve higher efficiency. Other suitable applications include supplies for dc power distribution systems in telecommunication, future more electric aircraft, variable speed ac drives, and high-power lighting systems. The SR was first introduced in [7] and [8], however, only a brief description of the rectifier concept was given. In this paper, after the explanation of the principle of operation of the rectifier topology, employing a three-phase active third harmonic current injection rectifier in Section II, the derivation of the input current space vectors and the calculation of the relative on-times of the active switches guaranteeing PFC operation are presented in Section III. A pulsewidth modulation (PWM)-control method using triangular carriers is proposed in Section IV. The analytical expressions for calculating the

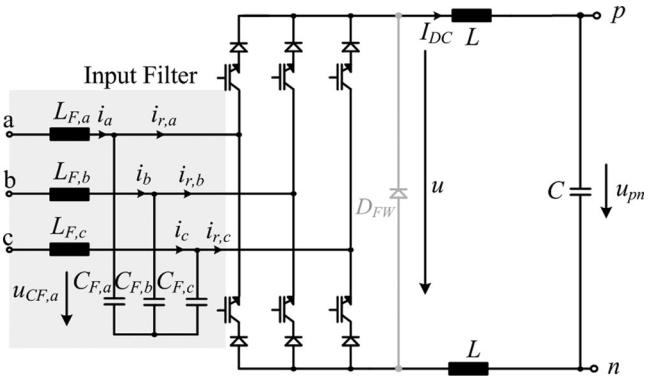

Fig. 2. Circuit topology of a three-phase six-switch buck-type PFC rectifier with *LC* input filter and explicit freewheeling diode D_{FW}.

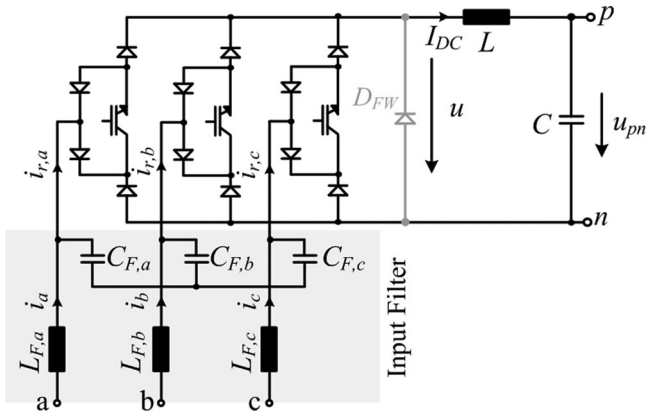

Fig. 3. Basic circuit of the three-phase three-switch buck-type PFC rectifier with input filter $L_{F,a,b,c}$ and $C_{F,a,b,c}$ and explicit freewheeling diode D_{FW}.

stresses of the main semiconductors and passive components in dependency on the input current amplitude and the voltage transfer ratio of the converter are given in Section V. A 7.5 kW SR is designed to attest the feasibility of the proposed rectifier concept. Finally, in Section VI, the SR is systematically compared with a six-switch buck-type PFC rectifier, shown in Fig. 2, which represents the standard three-phase buck-type topology.

II. Three-Phase Buck-Type PFC Rectifier

Agreement with strict guidelines regarding the mains behavior of the three-phase rectifier systems (EN 61000-3-2 and 61000-3-4) and dc output voltage regulation capability can be achieved with the converter structure shown in Fig. 2, which is known as the six-switch buck-type PFC rectifier. By proper modulation of the power transistor in continuous conduction mode, the superimposed output current I_{DC} can be strategically distributed to the three phases in such a manner that after the low-pass filtering the system drains sinusoidal mains currents. Additionally, the line-to-line voltages can be deliberately switched to the output *u* and a cascading low-pass filtering (*L* and *C*) in order to regulate the output voltage u_{pn} [7]. In order to maximize the achievable voltage level, while supplying each mains phase with currents, the two largest line-to-line voltages available during the mains sector can be selected in each pulse period for the formation of the output voltage. Correspondingly, the output voltage can ideally be adjusted to values starting from zero to values

$$u_{pn} < \sqrt{\frac{3}{2}} u_{N,l-l,\mathrm{rms}}. \tag{1}$$

An alternative buck-type PFC rectifier configuration with similar operating characteristics, employing only three power transistors on the ac side of the bridge rectifier, also known as three-switch buck-type PFC rectifier, is presented in Fig. 3. The main drawback of this converter is the high number of semiconductors in the current path, resulting in higher conduction losses than the six-switch version [6]. As for the six-switch buck PFC, the conduction losses in the freewheeling state could be reduced by implementation of an additional freewheeling diode D_{FW} as is shown in Figs. 2 and 3.

A three-phase PFC rectifier solution combining buck dc–dc converters and an active third harmonic current injection circuit, referred to here as the SR, is shown in Fig. 1. Other third harmonic injection topologies are described in [13]–[16], including the dual converter of the SR, a boost-type rectifier.

The SR allows the currents in the positive and negative active switches, i_{T+} and i_{T-}, to be formed proportionally to the two-phase voltages involved in the formation of the output voltage of the diode bridge. If the difference between i_{T+} and i_{T-} is fed back into the mains phase with the currently smallest absolute voltage value via a current injection network, formed with three four-quadrant switches gated at twice the mains frequency, a sinusoidal input current shape can be assured for all mains phases while the dc–dc converters guarantee the output voltage regulation.

A circuit implementation with a single-output inductor is feasible, however, in the proposed circuit, shown in Fig. 1, the total dc inductance is split evenly between the positive and negative output bus in order to provide symmetric attenuation impedances for conducted common mode (CM) noise. The conduction losses in the freewheeling state could be reduced by the implementation of an additional freewheeling diode D_{FW}.

For the SR, the output voltage range is limited by the minimal value of the six-pulse diode bridge output voltage, given by (1) and therefore is identical to the output voltage range for the buck-type PFC rectifiers, shown in Figs. 2 and 3. Contrary to the six-switch buck-type PFC systems, the rectifier diodes of the SR are not commuted with switching frequency. Correspondingly, the conduction losses can be reduced by the use of devices with a low-forward voltage drop (and a higher reverse recovery time). In addition, the mains commutated injection switches could be implemented with an antiparallel connection of RB-insulated gate bipolar transistors (IGBTs) with a low-forward voltage drop.

As shown in Fig. 4 the buck-type dc–dc converter units and the four-quadrant switches of the injection circuit can be replaced by other typical power electronic circuits. Additionally, if converter isolation and/or further voltage level regulation is necessary a transformer can be included in the dc–dc converter units to

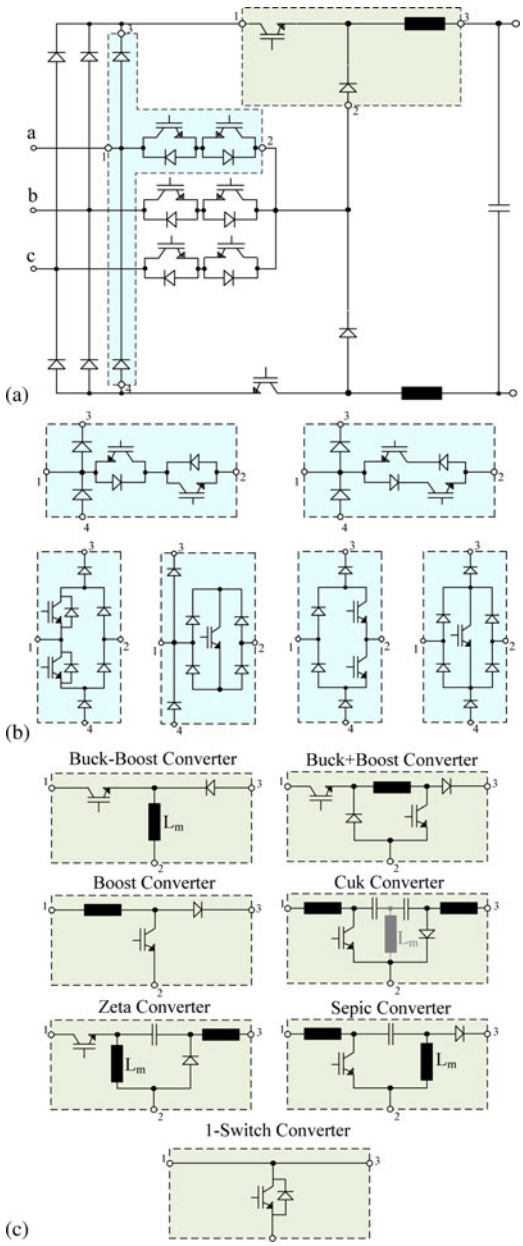

Fig. 4. Alternative implementation of a three-phase PFC rectifier with an active third harmonic injection circuit. (a) Basic circuit of the SR (buck-type PFC rectifier). Alternative (b) four-quadrant switches and (c) dc–dc converters.

replace the inductors L_m shown in Fig. 4(c). A bidirectional version of the SR was proposed in [17].

III. Conduction States, Modulation, and Duty Cycle

For the analysis of the conduction states, the derivation of the current space vectors and the calculation of the relative turn-on times, symmetric mains conditions are assumed. The mains currents $i_{a,b,c}$ are considered to be equal to the fundamental component of the rectifier input currents $i_{r,a,b,c(1)}$. Hence, the reactive currents due to the filter capacitors are also neglected. Moreover, the filter capacitor voltages $u_{CF,a,b,c}$ at the input of the rectifier are considered purely sinusoidally shaped and in phase with the mains voltages $u_{a,b,c}$. The current in the dc

TABLE I
Modulation of the Current Injection Circuit (cf., Fig. 5)

Sector	S_{y1}	S_{y2}	S_{y3}	Sector	S_{y1}	S_{y2}	S_{y3}
0°-30°	0	1	0	180°-210°	0	1	0
30°-60°	0	1	0	210°-240°	0	1	0
60°-90°	1	0	0	240°-270°	1	0	0
90°-120°	1	0	0	270°-300°	1	0	0
120°-150°	0	0	1	300°-330°	0	0	1
150°-180°	0	0	1	330°-360°	0	0	1

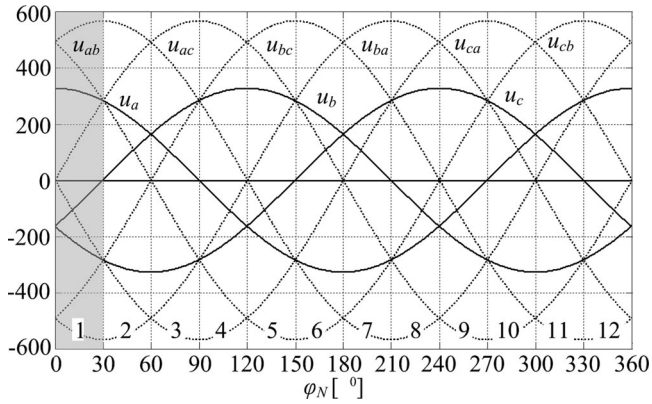

Fig. 5. Mains sectors 1–12 defined by the different relations of the instantaneous values of the mains phase voltages $u_{a,b,c}$.

inductors I_{DC} is assumed to be constant. Finally, all the analyses consider one of the twelve 30°-wide sectors of the mains period, i.e., $0^\circ < \varphi_N < 30^\circ$ with $\varphi_N = \omega_N t$, which is characterized by the mains phase relation $u_a > u_b > u_c$. For the remaining sectors, the calculations can be performed in a similar manner.

The modulation of the current injection circuit is performed at low frequency, following the rectifier input voltages $u_{CF,a,b,c}$ in such a way that the active current injection occurs always into only one mains phase as presented in Table I (cf., Fig. 5). Accordingly, in each of the 30°-wide sectors of the mains period, four different conduction states can be defined by the switches T_+ and T_- within a pulse period T_P, where the dc current I_{DC} impressed by the dc inductors is distributed to two of the input phases or is kept in a freewheeling state. The rectifying discrete converter input current space vector can be calculated by

$$\underline{i}_r = \frac{2}{3}\left(i_{r,a} + e^{j(2\pi/3)} i_{r,b} + e^{j(4\pi/3)} i_{r,c}\right). \tag{2}$$

Fig. 6(a) presents the four conduction states of the SR for the interval $\varphi_N \in [0^\circ, 30^\circ]$. For the switching state j = (ON, ON), where $j = (T_+, T_-)$ indicates a combination of the switching functions of the two fast switches (T_+ and T_-) and ON means that the respective switch is turned ON, while OFF indicates an off-state of the switch, the rectifier input currents are $i_{r,a} = I_{\mathrm{DC}}$, $i_{r,b} = 0$, and $i_{r,c} = -I_{\mathrm{DC}}$. Therefore, the rectifier input current space vector for this switching state results in

$$\underline{i}_{r,(\mathrm{ON,ON})} = \frac{2}{\sqrt{3}} I_{\mathrm{DC}} e^{j(\pi/6)}. \tag{3}$$

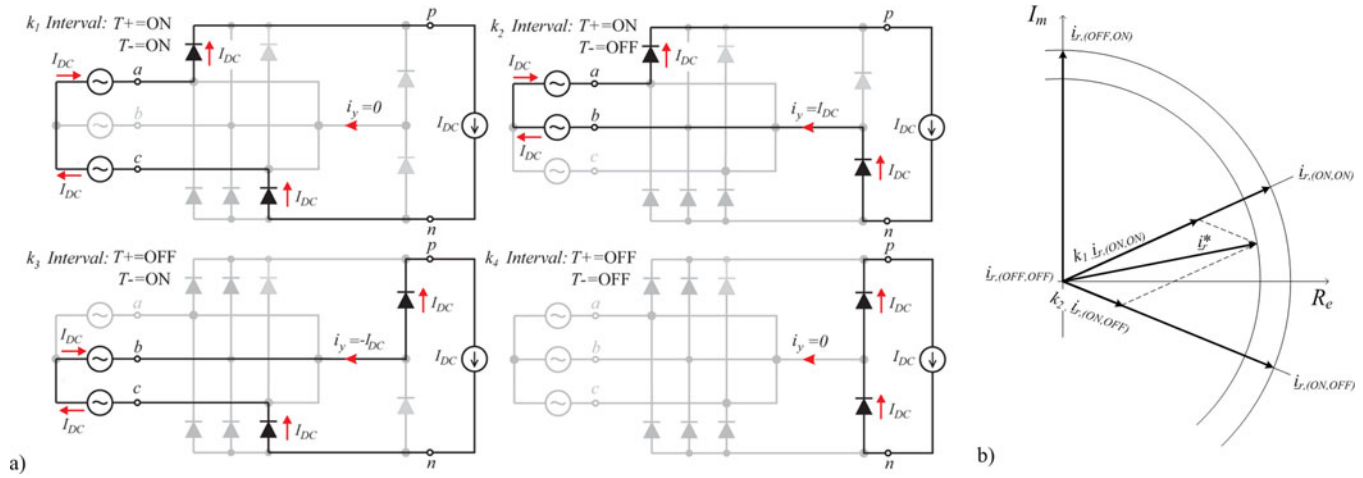

Fig. 6. (a) Conduction states and (b) input current space vector diagram of the SR for $\varphi_N \in [0°, 30°]$.

Analogously, the three remaining space vectors can be calculated as

$$\underline{i}_{r,(\mathrm{ON,OFF})} = \frac{2}{\sqrt{3}} I_{\mathrm{DC}} e^{-j(\pi/6)} \tag{4}$$

$$\underline{i}_{r,(\mathrm{OFF,ON})} = \frac{2}{\sqrt{3}} I_{\mathrm{DC}} e^{j(\pi/2)} \tag{5}$$

$$\underline{i}_{r,(\mathrm{OFF,OFF})} = 0. \tag{6}$$

With these four space vectors, a resulting input current space vector $\underline{i}_r^*$ can be formed [cf., Fig. 6(b)] so that it is in phase with the mains voltage vector $\underline{u}_r^*$ and has the required amplitude according to the actual power demand.

Proper selection of the switching state sequences allows control over the current ripple Δi_{DC} of the dc inductor current I_{DC} and Δi_y of the phase injection current i_y. Accordingly, the converter can be modulated in order to minimize the current ripple of i_y or that of the inductor current I_{DC}.

For the first mains sector $(0° < \varphi_N < 30°)$, the SR can operate with minimal injection current ripple Δi_y and consequently lower ripple values of the input capacitor voltages $u_{CF,a,b,c}$ if a vector modulation with the switching sequence (ON, ON)–(ON, OFF)–(OFF, OFF)–(ON, OFF)–(ON, ON), arranged symmetrically around the middle of the pulse interval, is applied [cf., Fig. 7(a)]. As can be seen in Fig. 7(a), the input phase currents are formed by segments of the dc current I_{DC} defined by the relative on-times k_i of the current vectors

$$i_{r,a} = I_{\mathrm{DC}}(k_1 + k_2); \quad i_{r,b} = -I_{\mathrm{DC}} k_2; \quad i_{r,c} = -I_{\mathrm{DC}} k_1. \tag{7}$$

The output voltage u_{pn} is formed by the line-to-line voltages u_{ab} and u_{ac} rated by the relative on-time of the respective current vectors

$$u_{pn} = k_1 u_{ac} + k_2 u_{ab}. \tag{8}$$

Note that u_{pn} is limited by the minimal value of the six-pulse diode bridge output voltage as given in (1).

Finally, PFC operation in the first mains sector can be achieved with relative on-times k_i, reliant on the modulation

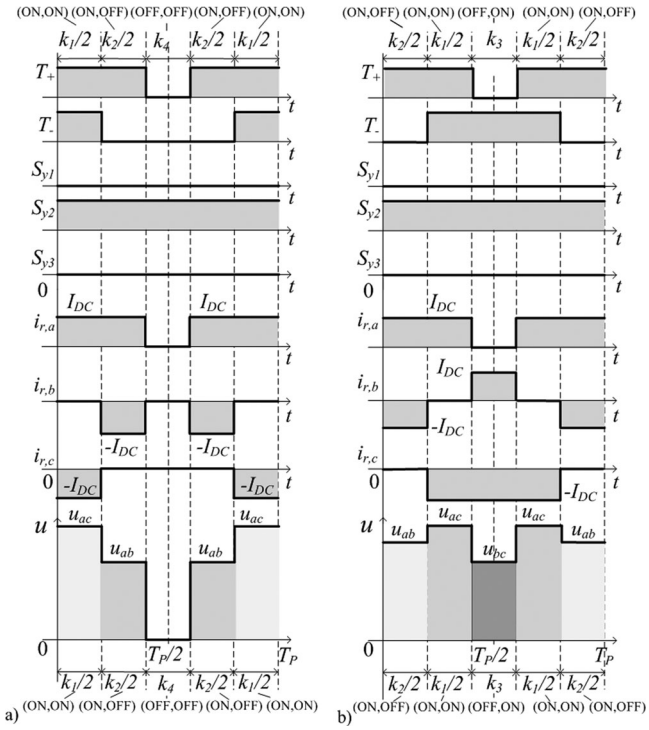

Fig. 7. Modulation scheme for (a) minimal injection current ripple Δi_y or (b) minimal dc current ripple Δi_{DC} for $\varphi_N \in [0°, 30°]$.

index M, the instantaneous values of $u_{a,b,c}$, and the amplitude of the mains phase voltages $\hat{U}_N$ given by

$$M = \frac{2}{3} \frac{u_{pn}}{\hat{U}_N} \tag{9}$$

$$k_1 = -M \frac{u_c}{\hat{U}_N}, \quad k_2 = -M \frac{u_b}{\hat{U}_N}, \quad k_4 = 1 - M \frac{u_a}{\hat{U}_N}. \tag{10}$$

Note that the switch duty cycles a_+ (for T_+) and a_- (for T_-) for symmetric mains $(u_a + u_b + u_c = 0)$ are defined according to

$$\alpha_+ = \frac{2}{3} \frac{u_{pn}}{\hat{U}_N^2} u_a = \frac{2}{3} \frac{u_{pn}}{\hat{U}_N^2} (-u_b - u_c) = k_1 + k_2 \tag{11}$$

$$\alpha_- = -\frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}u_c = k_1. \tag{12}$$

Alternatively, for the first mains sector ($0° < \varphi_N < 30°$), the SR can operate with minimized dc inductor current ripple Δi_{DC} and consequently reduced ripple values of the output low-pass filtering if a vector modulation with the switching sequence (ON,OFF)–(ON,ON)–(OFF,ON)–(ON,ON)–(ON,OFF), arranged symmetrically around the middle of the pulse interval, is applied [cf., Fig. 7(b)]. As can be seen in Fig. 7(b), the (local average) input phase currents are defined by the dc current I_{DC} and the relative on-times k_i

$$\begin{aligned} i_{r,a} &= I_{\mathrm{DC}}\,(k_1 + k_2)\,; \quad i_{r,b} = I_{\mathrm{DC}}\,(k_3 - k_2)\,; \\ i_{r,c} &= -I_{\mathrm{DC}}\,(k_1 + k_3)\,. \end{aligned} \tag{13}$$

The output voltage u_{pn} is formed by the line-to-line voltages u_{ab}, u_{bc}, and u_{ac}, weighted by the relative on-times of the respective current vectors

$$u_{pn} = k_1 u_{ac} + k_2 u_{ab} + k_3 u_{bc}. \tag{14}$$

Finally, PFC operation in the first mains sector can be achieved with relative on-times k_i, dependent on the modulation index M, instantaneous input voltage values $u_{a,b,c}$, and the amplitude of the mains phase voltages $\hat{U}_N$ given by

$$k_2 = 1 + M\frac{u_c}{\hat{U}_N}, \quad k_3 = 1 - M\frac{u_a}{\hat{U}_N},$$

$$k_1 = 1 - k_2 - k_3 = M\frac{u_a - u_c}{\hat{U}_N} - 1, \quad k_4 = 0 \tag{15}$$

$$\alpha_+ = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}u_a = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}\,(-u_b - u_c) = k_1 + k_2 \tag{16}$$

$$\alpha_- = -\frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}u_c = k_1 + k_3. \tag{17}$$

Note that the (15)–(17) are valid for $M \geq \hat{U}_N/u_{\mathrm{rect}}$, where $u_{\mathrm{rect}} = \{\max(u_a, u_b, u_c) - \min(u_a, u_b, u_c)\}$. For $M < \hat{U}_N/u_{\mathrm{rect}}$, the following equations are valid:

$$k_2 = M\frac{u_a}{\hat{U}_N}, \quad k_3 = -M\frac{u_c}{\hat{U}_N},$$

$$k_4 = 1 - k_2 - k_3 = 1 - M\frac{u_a - u_c}{\hat{U}_N}, \quad k_1 = 0 \tag{18}$$

$$\alpha_+ = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}u_a = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}\,(-u_b - u_c) = k_2 \tag{19}$$

$$\alpha_- = -\frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}u_c = k_3. \tag{20}$$

Finally, for all the remaining current space vectors the duty cycles of T_+ and T_- can be determined as

$$\alpha_+ = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}\max\,(u_a, u_b, u_c) \tag{21}$$

$$\alpha_- = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}\,|\min\,(u_a, u_b, u_c)|\,. \tag{22}$$

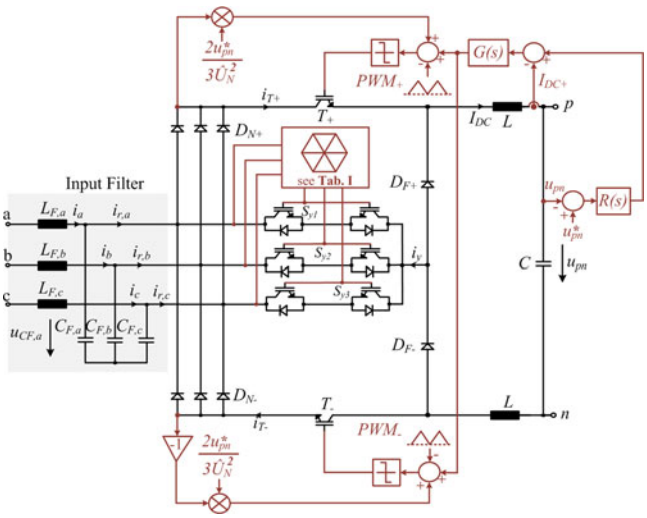

Fig. 8. PWM control structure for the SR.

IV. PWM Control Scheme

A possible implementation of a control scheme for the SR is shown in Fig. 8. This feedback PWM control comprises a superimposed output voltage controller $R(s)$ and a subordinate output current controller $G(s)$. Finally, a feed-forward loop adds the normalized modulation functions defined by the positive and negative diode bridge output voltage and the system output voltage reference value u_{pn}^* to the dc current controllers in order to directly generate the input current forming voltage u.

In the proposed control structure, setting the PWM modulator for T_+ and T_- to operate with in-phase carriers allows the system to work similarly to if it were controlled with the vector modulation described in Fig. 7(a), where the current ripple Δi_y is minimized while Δi_{DC} is maximized. On the other hand, operation using carriers with a phase difference of 180° (interleaved carriers) permits the system to work similarly to if it were controlled with the vector modulation depicted in Fig. 7(b), where the dc current ripple Δi_{DC} is minimized.

Simulation results, depicting the principle of operation of the SR, are shown in Fig. 9. The converter specifications, given in Table II, are considered in the simulation where operation with in-phase or interleaved PWM carriers and a load step (from 3.75 to 7.5 kW) are presented. As can be observed, the results demonstrate that the line currents $i_{a,b,c}$ can effectively follow the sinusoidal input phase voltages $u_{a,b,c}$ even in case of load steps, attesting the feasibility of the proposed rectifier and PWM control.

V. SR System Design

In this section, in order to provide a clear and general guideline for the components selection for the SR design, the stresses of the active and passive components of the converter are calculated analytically with dependence on the operating parameters of the rectifier. In addition, the power losses across the main components of the rectifier are derived such that during the initial design stage of the converter the total loss and efficiency

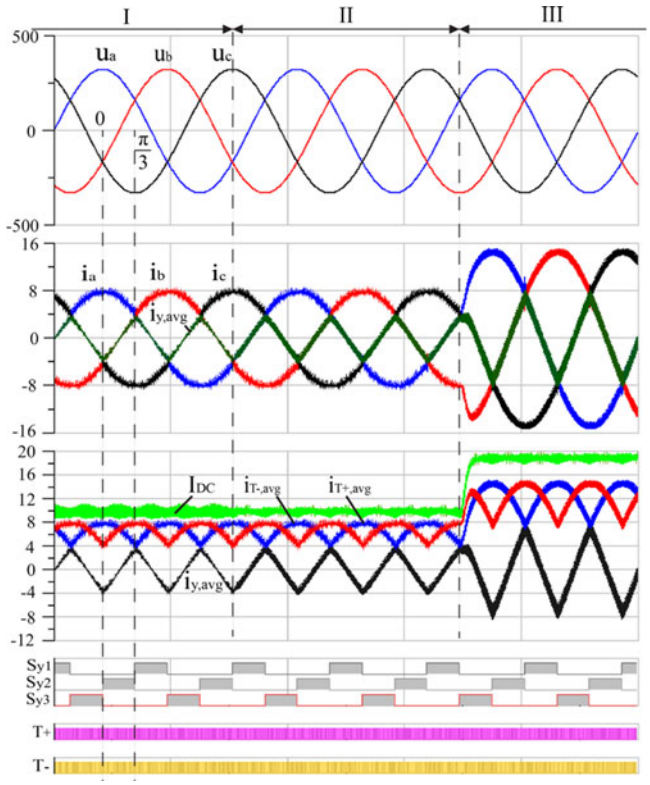

Fig. 9. Simulation results of the SR operating with (I) in-phase or (II) interleaved PWM carriers; (III) load step from 50% to 100% of the rated output power (3.75–7.5 kW).

TABLE II
SR PROTOTYPE SPECIFICATIONS

Input phase voltage $u_{a,b,c}$	230 V *rms* ±10%
Mains frequency f_N	50 Hz
Switching frequency f_P	36 kHz
Rated output power P_0	7.5 kW
Output capacitor C	470 µF
DC inductor L	305 µH

can be anticipated. Finally, the DM and CM noise models of the SR are presented. As an application case, a 7.5 kW unity power factor rectifier system shall be dimensioned that should provide a constant output voltage of $u_{pn} = 400\,\mathrm{V}$ for operation at a mains with 230 $\mathrm{V_{rms}}$ phase voltage ($u_{a,\mathrm{rms}} = 230\,\mathrm{V} \pm 10\%$) and a switching frequency of $f_P = 36\,\mathrm{kHz}$.

A. Semiconductor Voltage and Current Stresses

The maximum voltage stress on the line diodes, D_{N+} and D_{N-}, is defined by the line-to-line voltage $u_{N,l-l,\max}$

$$u_{DN,\max} = u_{N,l-l,\max} = \sqrt{2}\sqrt{3}u_{a,\mathrm{rms}}\,(1+10\%) = 620\,\mathrm{V}. \tag{23}$$

All the remaining semiconductors (T_+, T_-, D_{F+}, D_{F-}, and S_y) have to block a maximum voltage that corresponds to the 60° sinusoidal progression of the maximum line-to-line input voltage $u_{N,l-l,\max}$

$$u_{DF,\max} = u_{T,\max} = u_{Sy,\max} = \frac{\sqrt{3}}{2}u_{N,l-l,\max} = 537\,\mathrm{V}. \tag{24}$$

Note that the selections of the blocking voltage capability of the power transistors and diodes have to consider a additional safety margin δ for undesirable oscillations of the rectifier input voltage in case of low-passive damping of the input filter. Therefore, 1200 V power diodes and IGBTs ($55\% > \delta > 48\%$) or 900 V MOSFETs ($\delta \approx 40\%$) are suitable for the full silicon implementation of the SR. For the design at hand, the latest generation Trench and Fieldstop IGBTs as active switches are considered further.

In order to determine the on-state losses of the semiconductors, the current *rms* and average values have to be calculated and therefore, simple analytical approximations are derived. For the following calculations, it is assumed that the rectifier has:

1) a purely sinusoidal phase current shape;
2) ohmic fundamental mains behavior;
3) a constant dc current I_{DC};
4) no low-frequency voltage drop across the input filter inductors, therefore $u_{C,a,b,c} = u_{a,b,c}$;
5) a switching frequency that is much higher than the mains frequency f_N ($f_P \gg f_N$).

1) Current Stress of the Bidirectional Switches S_y and D_y: With a defined modulation index M [cf., (9)], the average and *rms* currents of the two transistors and diodes forming a bidirectional switch finally result in

$$I_{Sy/Dy,\mathrm{avg}} = I_{\mathrm{DC}}M\frac{2-\sqrt{3}}{2\pi} \quad \text{and}$$
$$I_{Sy/Dy,\mathrm{rms}} = I_{\mathrm{DC}}M\sqrt{-\frac{\sqrt{3}}{2\pi}+\frac{1}{3}}. \tag{25}$$

The total power loss of the low-frequency commanded IGBTs S_y and diodes D_y, P_{Sy}, and P_{Dy}, are mainly defined by their conduction losses, and can be approximated by

$$P_{Sy/Dy} = I^2_{Sy/Dy,\mathrm{rms}}R_{Sy} + I_{Sy/Dy,\mathrm{avg}}V_{Sy} \tag{26}$$

where R_{Sy} is the on-resistance and V_{Sy} is the forward voltage of the selected commercial power devices (IGBT/diode).

2) Current Stress of the Rectifier Diodes D_{N+} and D_{N-}: The average and *rms* currents of the rectifier diodes can be calculated as

$$I_{DN,\mathrm{avg}} = I_{\mathrm{DC}}M\frac{\sqrt{3}}{2\pi} \quad \text{and} \quad I_{DN,\mathrm{rms}} = I_{\mathrm{DC}}\sqrt{\frac{\sqrt{3}M}{2\pi}}. \tag{27}$$

The rectifier diodes D_N dissipate essentially conduction losses, thereby the total power losses across this device is defined by

$$P_{DN} = I^2_{DN,\mathrm{rms}}R_{DN} + I_{DN,\mathrm{avg}}V_{DN} \tag{28}$$

where R_{DN} is the on-resistance and V_{DN} is the forward voltage of the selected commercial power diode.

3) Current Stress of the Fast Diodes D_{F+} and D_{F-}: The average and *rms* currents of the fast freewheeling diodes can be determined as

$$I_{DF,\mathrm{avg}} = I_{\mathrm{DC}}\left(1 - \frac{3\sqrt{3}}{2\pi}M\right) \quad \text{and}$$

$$I_{DF,\mathrm{rms}} = I_{\mathrm{DC}}\sqrt{1 - \frac{3\sqrt{3}}{2\pi}M}. \tag{29}$$

The conduction loss of the fast diodes $P_{DF,c}$ can be estimated by

$$P_{DF,c} = I^2_{DF,\mathrm{rms}}R_{DF} + I_{DF,\mathrm{avg}}V_{DF} \tag{30}$$

where R_{DF} is the on-resistance and V_{DF} is the forward voltage drop of the selected commercial power diode.

The reverse recovery losses of the fast diodes $P_{DF,s}$ can be calculated by

$$P_{DF,s} = \frac{3\sqrt{3}\hat{U}_N f_P E_{\mathrm{rr},DF}(I_{\mathrm{DC}}, U_B)}{2\pi U_B} \tag{31}$$

where $E_{\mathrm{rr},DF}(I_{\mathrm{DC}}, U_B)$, which can be obtained directly from the manufacturers datasheet, is the reverse recovery energy modeled as a function of the forward current of the diode and the applied reverse voltage U_B utilized during the switching loss measurements, assuming a constant current fall time.

Finally, the total averaged power loss P_{DF} can be determined using

$$P_{DF} = P_{DF,c} + P_{DF,s}. \tag{32}$$

4) Current Stress of the Power Transistors T_+ and T_-: The average and *rms* currents of the PWM-modulated power transistors are determined by

$$I_{T,\mathrm{avg}} = I_{\mathrm{DC}}M\frac{3\sqrt{3}}{2\pi} \quad \text{and} \quad I_{T,\mathrm{rms}} = I_{\mathrm{DC}}\sqrt{\frac{3\sqrt{3}M}{2\pi}}. \tag{33}$$

The conduction loss of the fast IGBTs, $P_{T,c}$, can be estimated by

$$P_{T,c} = I^2_{T,\mathrm{rms}}R_T + I_{T,\mathrm{avg}}V_T \tag{34}$$

where R_T is the on-resistance and V_T is the forward voltage drop of the selected IGBT.

The switching losses of the fast IGBTs, $P_{T,s}$, can be calculated by

$$P_{T,s} = \frac{3\sqrt{3}\hat{U}_N f_P \left(E_{T,\mathrm{ON}}(I_{\mathrm{DC}}, U_B) + E_{T,\mathrm{OFF}}(I_{\mathrm{DC}}, U_B)\right)}{2\pi U_B} \tag{35}$$

where $E_{T,\mathrm{ON}}(I_{\mathrm{DC}}, U_B)$ and $E_{T,\mathrm{OFF}}(I_{\mathrm{DC}}, U_B)$, which can be obtained directly from the manufacturers datasheet, are the turn-on and turn-off energy modeled as a function of the forward current and the applied reverse voltage U_B.

Finally, the total averaged power loss P_T can be determined using

$$P_T = P_{T,c} + P_{T,s}. \tag{36}$$

B. Passive Components: Voltage and Current Stresses

1) DC Inductor L: The voltage across each of the dc inductors *L* is equivalent to half of the value of the maximum allowed line-to-line input voltage $u_{N,l-l,\max}$

$$u_{L+} + u_{L-} = u_{N,l-l,\max} \quad \therefore u_{L+} = \frac{u_{N,l-l,\max}}{2} = 310\,\mathrm{V}. \tag{37}$$

The current flowing through *L* is defined by the full dc (load) current I_{DC} and a current ripple $\Delta i_{L,\mathrm{pp,max}}$, which is limited to a given value, i.e., 25% of I_{DC}. The current ripple peak-to-peak value and the *rms* value of the dc inductor current, $\Delta i_{L,\mathrm{pp}}$ and $i_{L,\mathrm{rms}}$, can be determined as follows:

$$I_{\mathrm{DC}} = \frac{P_0}{u_{pn}} \tag{38}$$

$$\Delta i_{L,\mathrm{pp,max}} = \frac{u_{pn}}{2Lf_P}\left(1 - \frac{\sqrt{3}}{2}M\right) \tag{39}$$

$$i_{L,\mathrm{rms}} = \sqrt{I^2_{\mathrm{DC}} + \frac{\Delta i^2_{L,\mathrm{pp,max}}}{12}}. \tag{40}$$

The inductance value of the dc inductor can then be selected according to

$$L \geq \frac{u_{pn}}{2\Delta i_{L,\mathrm{pp,max}} f_P}\left(1 - \frac{\sqrt{3}}{2}M\right). \tag{41}$$

The losses for the output inductors *L* can be dived into: core losses, dc winding resistance losses, and high-frequency copper losses due to skin and proximity effect. The core losses can be calculated using the modified Steinmetz equation for triangular current (current ripple) [18] as follows:

$$P_{\mathrm{core}} = k f_P \left(\frac{2}{\pi^2}4f_P\right)^{\alpha-1}\hat{B}^{\beta}V_{\mathrm{core}} \tag{42}$$

where *k*, α, and β are the Steinmetz parameters obtained from the core material, $\hat{B}$ is the peak magnetic flux density [cf., (43)] and V_{core} is the total core volume

$$\hat{B} = \frac{L\Delta i_{L,\mathrm{pp}}}{2NA_e} \tag{43}$$

where A_e is the inductor core cross-sectional area. The dc resistance $R_{L,\mathrm{DC}}$ of an inductor assembled with E-cores wound with solid rectangular wire can be determined with

$$R_{L,\mathrm{DC}} = \frac{\rho N l_T}{A_\omega} \tag{44}$$

where ρ is the wire resistivity, *N* is the number of turns, l_T is the average length of a turn, and A_ω is the wire cross-sectional area. The modeling of the ac winding resistance $R_{L,ac,nn}$ resulting from the *n*th harmonic of the current ripple Δi_L can be determined using the Ferreira method [19]

$$R_{L,ac,n} = R_{L,\mathrm{DC}}\frac{\xi(\eta)}{2}e\frac{\sinh\xi(\eta) + \sin\xi(\eta)}{\cosh\xi(\eta) - \cos\xi(\eta)} + \\ + \sum_{m=1}^{m_{\mathrm{tot}}}\frac{R_{L,\mathrm{DC}}}{m_{\mathrm{tot}}}\frac{\xi(\eta)}{2}\eta^2(2m-1)\frac{\sinh\xi(\eta) - \sin\xi(\eta)}{\cosh\xi(\eta) + \cos\xi(\eta)}. \tag{45}$$

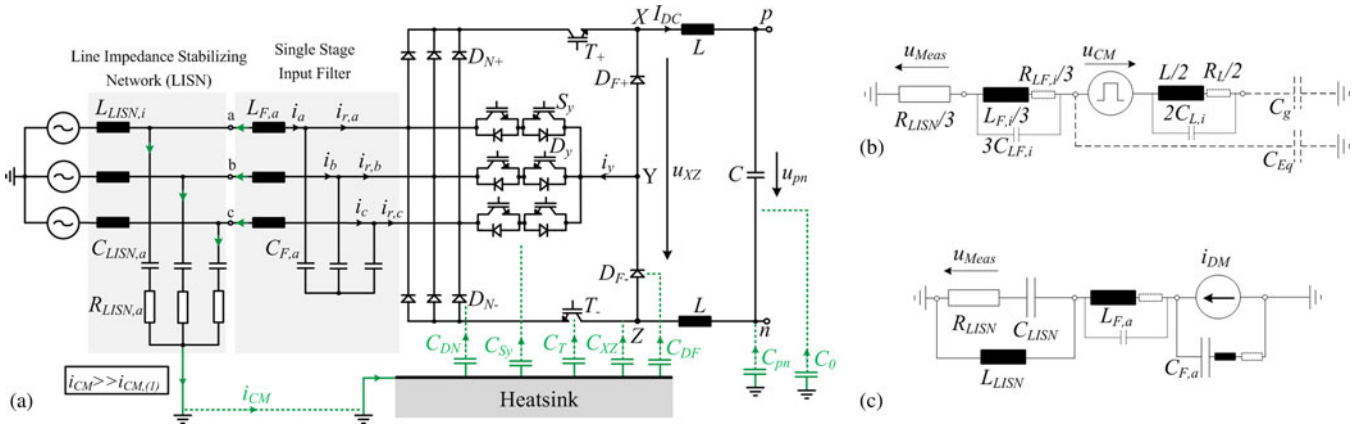

Fig. 10. (a) Model for the propagation of the CM currents in the SR used for deriving the CM noise model. Simplified high-frequency model for (b) CM and (c) DM emissions, including the high-frequency equivalent circuit of the LISN and a single stage DM input filter with parasitics of inductive and capacitive elements shown.

For an inductor with $m_{\rm tot}$ layers of windings with porosity factor η and skin depth related term $\xi(\eta)$

$$\eta = \frac{aN_m}{b} \quad \text{and} \quad \xi(\eta) = \sqrt{A_\omega \pi \mu_0 \sigma n f_P \eta} \tag{46}$$

where a is the side length of the square conductor, b is the width of a layer, N_m is the number of turns in a layer, and σ is the conductivity of the wire. Finally, the total inductor loss P_L can be calculated as follows:

$$P_L = P_{\rm core} + R_{L,\rm DC} I_{\rm DC}^2 + \sum_{n=1}^{n_{\rm tot}} R_{L,ac,n} \frac{\Delta i_{L,n}^2}{3} \tag{47}$$

where $\Delta i_{L,n}$ is the amplitude of the nth harmonic of inductor current ripple.

2) Output Capacitor C: When selecting the output capacitor C, the value of the controlled output voltage u_{pn} and an additional overshoot margin to enable safe operation during load transients (around 10% of u_{pn}), must be taken into consideration

$$u_C > 1.1 u_{pn} = 440\,\text{V}. \tag{48}$$

The *rms* value of the output capacitor current ripple $\Delta i_{C,\rm rms}$ and the peak-to-peak value of the output voltage ripple $\Delta u_{C,\rm pp}$ are given by

$$\Delta i_{C,\rm rms} = \sqrt{\frac{\Delta i_{L,\rm pp,max}^2}{12}} \quad \text{and} \quad \Delta u_{C,\rm pp} = \frac{u_{pn}}{L}\left(\frac{1-M}{8 f_P^2 C}\right). \tag{49}$$

The capacitance value of the dc output capacitor can then be determined according to

$$C \geq \frac{u_{pn}}{L}\left(\frac{1-M}{8 f_P^2 \Delta u_{C,\rm pp,max}}\right). \tag{50}$$

The power loss in the dc-link capacitor C is caused by the equivalent series resistance (ESR) and by leakage current $I_{\rm leak}$ [5]. The ESR, which is often given in the capacitor datasheets, can be calculated using the loss factor $\tan(\delta)$ given in the datasheets as follows:

$$\text{ESR} = \frac{\tan(\delta)}{2\pi f_P C}. \tag{51}$$

The leakage current $I_{\rm leak}$ can be determined using characteristic equations given in the datasheets. Finally, the total output capacitor losses P_C can be determined using

$$P_C = \Delta i_{C,\rm rms}^2 \text{ESR} + I_{\rm leak} u_{pn}. \tag{52}$$

C. Simple DM and CM Noise Models of the SR

The semiconductors of a power electronics converter are typically mounted onto a common heat sink that is usually connected to ground (PE). Therefore, parasitic capacitances to ground exist, leading to propagation of CM noise currents in the circuit (cf., Fig. 10).

Due to the discontinuous input current of the SR, at least a single-stage differential mode (DM) input filter, i.e., $L_{F,i}$ and $C_{F,i}$, is necessary. However, for full compliance to electromagnetic compatibility (EMC) standards, the conducted DM and CM noise emissions propagating to the mains have to be attenuated sufficiently. In order to design a proper EMI filter, the CM and DM noise levels of the SR need to be determined. Accordingly, the modeling approach given in [20] and [21] is extended to this three-phase converter.

The DM noise is generated by the pulsating input currents $i_{r,a,b,c}$ at switching frequency and is attenuated by the input filter capacitors $C_{F,a,b,c}$ and the ac side filter inductors $L_{F,a,b,c}$. The CM noise is caused within each pulse period T_P by the switched line-to-line voltages during the formation of the output voltage and for the distribution of the dc current to the mains phases. For the SR, this pulsed voltage $u_{\rm CM}$ has a maximum high-frequency peak-to-peak amplitude $U_{\rm CM,pp,max}$ of approximately

$$U_{\rm CM,pp,max} \approx \frac{3}{\sqrt{8}} u_{a,\rm rms}. \tag{53}$$

Fig. 10 defines the simplified circuits to evaluate CM and DM noise sources for the SR. There, the CM voltage $u_{\rm CM}$, the DM current $i_{\rm DM}$, and the stray capacitances, C_g and $C_{\rm Eq}$, model the

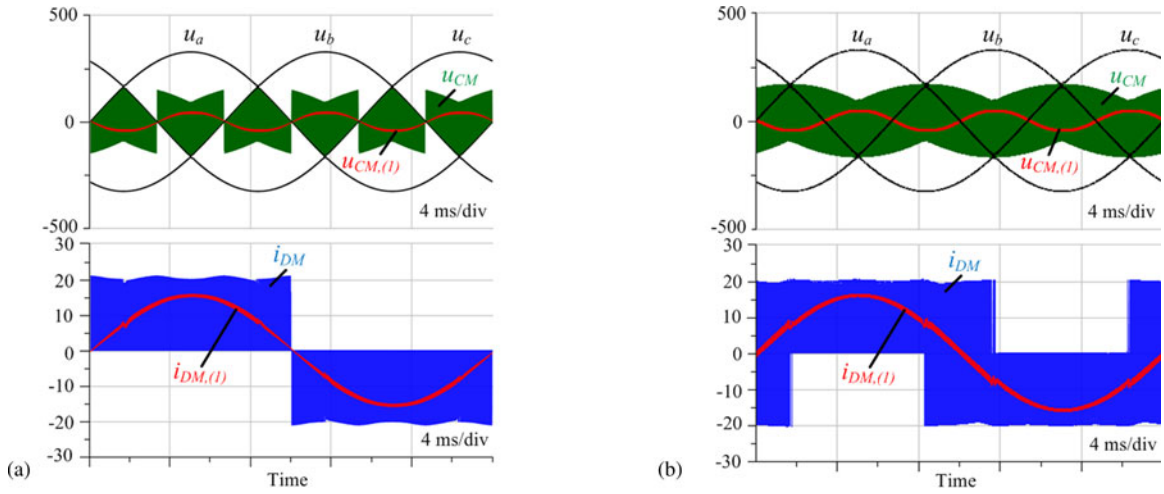

Fig. 11. Time behavior of the CM voltage $u_{\rm CM}$ and DM current $i_{\rm DM}$ noise sources of the SR operating with modulation (a) for minimal injection current ripple Δi_y [cf., Fig. 7(a)] and (b) for minimal dc inductor current ripple $\Delta i_{\rm DC}$ [cf., Fig. 7(b)].

power converter CM and DM noise circuits. The capacitances C_g and $C_{\rm Eq}$ are lumped representations of all relevant stray capacitances included in the CM propagation path. C_g represents mainly the capacitances of the positive and negative output voltage bus to ground C_{pn}, and from the load to earth C_0, while $C_{\rm Eq}$ models the stray capacitances from the semiconductors to the heatsink (C_{DN}, C_{Sy}, C_T, and C_{DF}) and the power connection terminals to earth, C_{XZ}.

A simplified time domain simulation of the system is sufficient to obtain the DM current and CM voltage sources, $i_{\rm DM}$ and $u_{\rm CM}$. The CM voltage can be calculated by measuring the voltages $u_{X,\rm PE}$ and $u_{Z,\rm PE}$

$$u_{\rm CM} = \frac{u_{X,\rm PE} + u_{Z,\rm PE}}{2} \tag{54}$$

and the DM currents are computed directly from the input currents as long as no CM paths exist in the simulation circuit. For simplicity, the current measured in phase a is used so that

$$i_{\rm DM} = i_{r,a}. \tag{55}$$

A simulation of the SR in GeckoCIRCUITs [22] is used for determining the CM and DM noise sources. The converter specifications listed in Table II are used to perform the simulation. The time behavior of the CM voltage $u_{\rm CM}$ and DM current $i_{\rm DM}$ for both space vector modulations described in Section III are presented in Fig. 11, where it can be seen that the CM voltage is formed with combinations of the input voltages, while the DM current is formed by the switched dc current $I_{\rm DC}$. Finally, the low-frequency component $i_{\rm DM,(1)}$ shows a nearly ideal sinusoidal behavior, thus PFC at the input of the converter is obtained.

It can be observed that the different modulation strategies result in different CM and DM waveforms that would finally lead to different EMI filter requirements. As an example, by comparing the calculated DM noise emissions for both modulations to the CISPR 22 Class B limit at $f = 180\,\rm kHz$ (first multiple of the switching frequency ($f_P = 36\,\rm kHz$) within the EMC measurement band), the required suppression for the EMI filter can be determined. As a result, with quasi-peak measurement, the necessary attenuation of noise for the modulation, which minimizes the ripple Δi_y, is $\rm Att_{req} = 75\,dB$, while for the modulation, which minimizes the ripple $\Delta i_{\rm DC}$, the necessary noise suppression is slightly higher, i.e., $\rm Att_{req} = 78\,dB$.

Due to the high required filter attenuations a second filter stage is recommended. For control stability reasons, the attenuation of the first stage filter, $L_{F,a,b,c}$ and $C_{F,a,b,c}$, has to be higher than for the second stage. As a design criteria, the suppression of the first DM filter stage will be considered as follows [21]:

$$\rm Att_{LF,CF}[dB] = (0.7, \ldots, 0.8)\, Att_{req}[dB]. \tag{56}$$

Additionally, the selection of $C_{F,i}$ needs to limit the voltage ripple peak-to-peak value at the input of the converter to about 5–10% in order to ensure correct detection of the input line-to-line voltages that is required for the system modulation [21]. On the other hand, high values of $C_{F,i}$ lead to a low-power factor at low-load operation, therefore, as a compromise the value of $C_{F,i}$ is defined in the range

$$C_{F,i}\,;\ \frac{I_{\rm DC} M\,(1-M)}{\Delta u_{CF,\rm pp} f_P}\,;\ 2.2\,\mu\rm F, \ldots, 5\,\mu F. \tag{57}$$

Finally, the range of the inductance value of the filter inductors can be determined for $\rm Att_{req}[dB] = 78\,dB$

$$L_{F,i} = \frac{10^{\rm Att_{LF,CF}[dB]/20}}{4\pi^2 C_{F,i}\,(f = 180\,\rm kHz)^2} = (66\,\mu\rm H, \ldots, 460\,\mu H). \tag{58}$$

In this paper, only the modeling of conducted differential and CM emissions for the SR is shown. A preliminary design of the EMI filter could be accomplished using computer simulation incorporating the derived equivalent circuits with the modeled CM and DM noise sources by following the strategy proposed by [21] such that the generated emissions measured by the modeled EMC test receiver $u_{\rm Meas}$ does not exceed the limits defined by

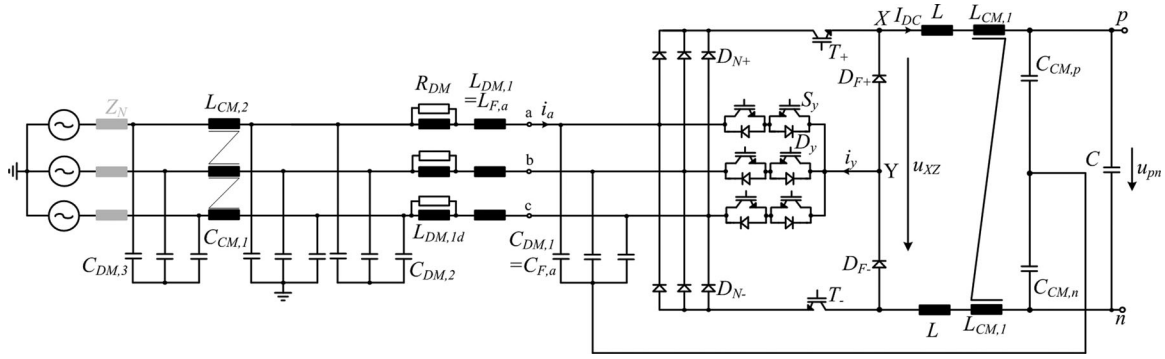

Fig. 12. Example of the EMI filter structure of the SR. Note that an additional filter stage is formed by the inner mains impedance Z_N.

TABLE III
SR: COMPARISON OF ACTIVE AND PASSIVE COMPONENT STRESSES DETERMINED BY ANALYTICAL CALCULATIONS AND DIGITAL SIMULATIONS

	Analytical Calculations	Simulation	Deviation [%]
$I_{Sy,avg}$	0.65	0.65	0.0
$I_{Sy,rms}$	3.69	3.57	+3.36
$I_{DN,avg}$	4.24	4.25	-0.23
$I_{DN,rms}$	8.92	8.95	-0.35
$I_{T,avg}$	12.72	12.75	-0.23
$I_{T,rms}$	15.45	15.5	-0.32
$I_{DF,avg}$	6.02	6.00	+0.33
$I_{DF,rms}$	10.63	10.62	+0.01
$i_{L,rms}$	18.81	18.79	+0.1
$\Delta i_{L,pp,max}$	5.27	5.17	+1.93

an EMC standard, i.e., CISPR22 class B. An example of the EMI structure suitable for the SR is shown in Fig. 12.

D. SR Model Accuracy

In order to verify the accuracy of the derived equations modeling the voltage and current stresses of the SR, an appropriate switching frequency and the values of the passive components according to (41), (50), (57), and (58) have been selected. A switching frequency of $f_P = 36\,\text{kHz}$ is designated as it constitutes a good compromise between high efficiency, high-power density, and high-control bandwidth. Advantageously, the fourth switching frequency harmonic is found near, but still below the beginning of the considered EMC measurement range at 150 kHz. With $f_P = 36\,\text{kHz}$, the values for the output filter $L = 305\,\mu\text{H}$ and $C = 470\,\mu\text{F}$ are selected. The component values of the first input filter stage is $L_{F,i} = 85\,\mu\text{H}$ and $C_{F,i} = 4.4\,\mu\text{F}$.

In Table III, the values of the average and *rms* component stresses calculated with the respective expressions are compared to the results obtained with a simulation performed in GeckoCIRCUITs [22] and show very good accuracy.

E. 7.5 kW Hardware Demonstrator

A laboratory prototype of the SR according to the specifications given in Table II has been built. The implemented prototype is shown in Fig. 13. A list of the employed semiconductor devices and passive components is given in Table IV along with the key design parameters. The overall dimensions of the system

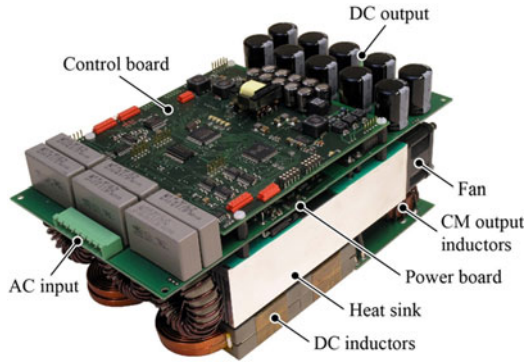

Fig. 13. Implemented 7.5 kW SR hardware prototype, using 1200 V Trench and Fieldstop IGBTs and 1200 V SiC MPS freewheeling diodes. Mechanical dimensions: 210 mm × 132 mm × 92 mm; power density: 2.94 kW/dm^3 = 48 W/in^3, switching frequency: $f_P = 36\,\text{kHz}$.

TABLE IV
SELECTED MAIN COMPONENTS OF THE SR HARDWARE PROTOTYPE (CF., FIG. 13)

Component	Device Description
S_y / D_y	Si T&FS IGBTs, 1200 V / 25 A, IKW25N120, Infineon
T_+ / T_-	Si HighSpeed T&FS IGBTs, IGW40N120H3, Infineon
D_{N+} / D_{N-}	Si fast recovery diode, DSEP060-12AR, IXYS
D_{F+} / D_{F-}	SiC Schottky diodes, 1200 V / 20 A, C2D20120A, CREE
L	305 µH, 2 x E64-50-10 cores, 3C91 ferrite, Ferrox Cube N_L = 16 turns, Cu wire cross section $A_{w,L}$ = 8.5 mm^2
C	10 x 47 µF / 450 V, electrolytic capacitors, EPCOS
$L_{F,abc}$	85 µH, High Flux 58254 powder core, Magnetics N_{Lf} = 22 turns, Cu wire cross section $A_{w,Lf}$ = 3.1 mm^2
$C_{F,abc}$	2 x 2.2 µF, 305 V X2, MKP foil, Arcotronics
$L_{CM,1}$	3 x series connected VAC500F cores with 2 8-turns winding (A_w = 4.9 mm^2)

are 210 mm × 132 mm × 92 mm, hence leading to a power density of 2.94 kW/dm^3.

Note that for the selection of the 7.5 kW SR components, the analytical (23)–(58) were utilized, considering the worst case operating condition for each specific component. For instance, the semiconductors have to cope with the highest current stress that occurs at the maximum modulation index ($M \approx 0.91$). According to (23) and (24), IGBTs and diodes with a blocking voltage capability of 1200 V have been chosen.

With respect to the operating principle of the converter, the injection switches $S_{y,i}$ are implemented with the latest generation Trench and Fieldstop IGBTs (1200 V/25 A, IKW25N120,

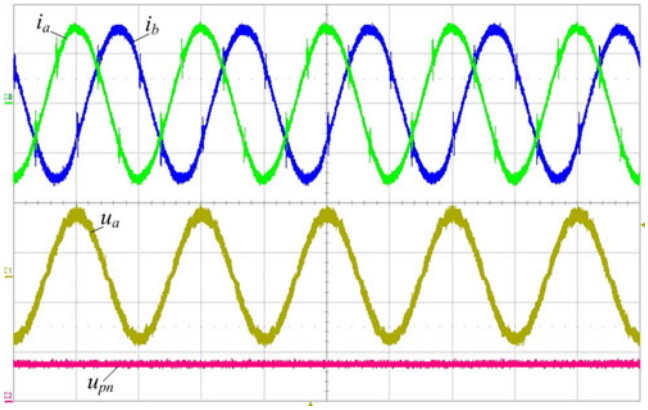

Fig. 14. Experimental waveforms (i_a and i_b: 10 A/div; u_a: 250 V/div; and u_{pn}: 500 V/div).

Infineon) with an antiparallel freewheeling diode that are optimized for low-conduction losses as they are switched with only twice the mains frequency. For the transistors T_+ and T_-, high-speed T&FS IGBTs (1200 V/40 A, IGW40N120 H3, Infineon) are used in combination with SiC MPS diodes (1200 V/20 A, C2D20120A, CREE) for D_{F+} and D_F to enable low-switching losses at the selected switching frequency of $f_P = 36$ kHz.

By combining the analytical equations for the losses of passive and active components (23)–(52) with the respective selected device (cf., Table IV) the total losses of the converter can be calculated depending on the operating parameters. A breakdown of the total losses of the designed system for nominal operation ($P_o = 7.5\,\text{kW}$, $u_{pn} = 400\,\text{V}$, $u_{a,b,c} = 230\,\text{Vrms}$ and $f_P = 36\,\text{kHz}$) is depicted in Fig. 16. Additionally, other loss sources are considered, such as for the auxiliary power supply that powers a TI DSP and a lattice field-programmable gate array used for the control, the gate drivers and the air cooling system. Losses in the PCB, connectors, and cables are also included.

The input currents of the rectifier i_a and i_b (10 A/div), the phase *a* mains voltage u_a (250 V/div) and the output voltage u_{pn} (500 V/div) are given in Fig. 14 for an output power of 7.5 kW, where an input current total harmonic distortion of 4% and a power factor of $\lambda = 0.99$ have been measured. The prototype efficiency has been measured with a Yokogawa WT3000 precision power analyzer (basic power accuracy of 0.02%). Fig. 15 shows the measured/calculated efficiency and losses over the output power for different output voltages ($u_{pn} = 400\,\text{V}$ and 440 V). It can be seen that the loss results obtained by calculations correspond very well with those obtained by measurement. The deviation can be explained by the approximately linear models of the conduction/switching losses and by the prediction of the other circuit losses.

VI. Buck-Type Rectifier Comparative Evaluation

In this section, the SR is compared to a standard buck-type ac–dc converter technology, i.e., the six-switch buck-type PFC (cf., Fig. 2). Thus, a suitable modulation scheme and the main design expressions of this PFC rectifier are given.

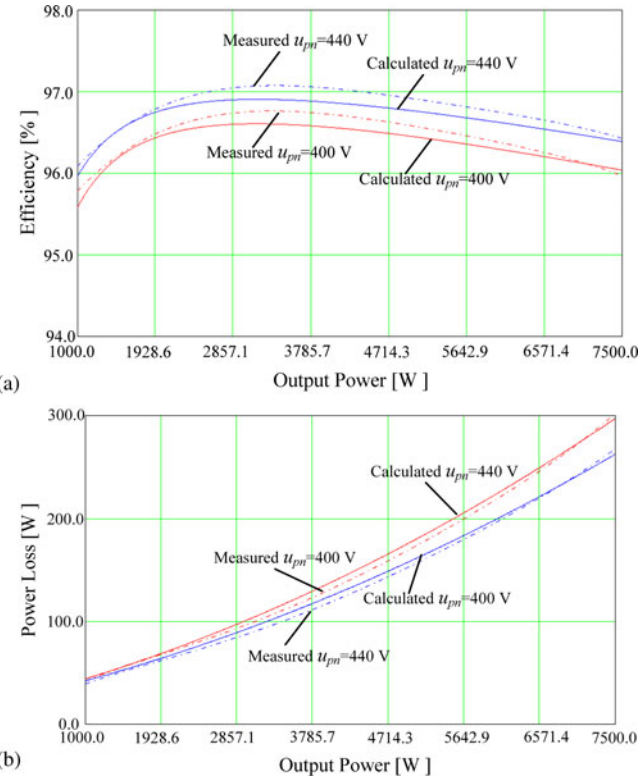

Fig. 15. Measured and calculated (a) efficiency and (b) power losses with the implemented 7.5 kW SR prototype.

Initially, the calculated total losses for the active and passive components for each analyzed rectifier specified according to Table II are used for the assessment. The power devices listed in Table IV are used for the calculation. Finally, the loss calculation is extended to a variable chip area to allow a fair comparison between the studied systems. This approach not only provides a distinct figure-of-merit for comparison, but can also be used to determine the semiconductor costs of the different topologies.

A. Six-Switch Buck-Type PFC: Modulation Scheme and Design

In this paper, the modulation scheme developed in [23]–[25] that guarantees minimum switching losses as well as minimum input filter capacitor voltage ripple is considered. This incorporates a short interval t_d during which switch on-times overlap guaranteeing the required freewheeling state of the inductor *L*, where the duty ratios $\delta_{a,b,c}$ for the three bridge legs are set according to

$$\delta_i = \frac{u_{pn,\text{ref}}}{\sum_{j=a,b,c} u_{CF,j}^2} |u_{CF,i}| \tag{59}$$

where $u_{pn,\text{ref}}$ is the required rectifier output voltage and $i = \{a, b, c\}$. In this modulation the IGBTs corresponding to the same phase are switched at the same time, with duty cycles corresponding to the values presented in Table V. Accordingly, the half of the leg and diode that conducts is determined by the input voltages.

As for the SR, the stresses of the active and passive components can be calculated analytically with dependency on the

TABLE V
APPLIED DUTY CYCLE BY INPUT VOLTAGE SECTOR FOR THE SIX-SWITCH BUCK-TYPE PFC RECTIFIER (CF., FIG. 5)

Sector	$\delta_{eff,a}$	$\delta_{eff,b}$	$\delta_{eff,c}$
1, 7	δ_a	$1-\delta_c+t_d$	δ_c
2, 8	δ_a	$1-\delta_a+t_d$	δ_c
3, 9	$1-\delta_b+t_d$	δ_b	δ_c
4, 10	$1-\delta_c+t_d$	δ_b	δ_c
5, 11	δ_a	δ_b	$1-\delta_a+t_d$
6, 12	δ_a	δ_b	$1-\delta_b+t_d$

operating parameters of the converter. For instance, the *rms* and average values of the fast diodes $D_{F+/-}$ and IGBTs $T_{+/-}$ can be calculated by

$$I_{T/DF,\mathrm{avg}} = \frac{I_{\mathrm{DC}}}{3} \quad \text{and} \quad I_{T/DF,\mathrm{rms}} = \frac{I_{\mathrm{DC}}}{\sqrt{3}}. \tag{60}$$

The conduction loss of the diodes/IGBTs, $P_{T/DF,c}$, can be estimated by

$$P_{T/DF,c} = I^2_{T/DF,\mathrm{rms}} R_{T/DF} + I_{T/DF,\mathrm{avg}} V_{T/DF} \tag{61}$$

where $R_{T/DF}$ is the on-resistance and $V_{T/DF}$ is the forward voltage drop of the selected diode or IGBT.

The switching losses of the diodes and IGBTs $P_{T/DF,s}$ can be calculated by (62) and (63), respectively

$$P_{T,s} = \frac{3\sqrt{3}\hat{U}_N f_P \left(E_{T,\mathrm{ON}}(I_{\mathrm{DC}},U_B) + E_{T,\mathrm{OFF}}(I_{\mathrm{DC}},U_B)\right)}{4\pi U_B} \tag{62}$$

$$P_{DF,s} = \frac{\sqrt{3}\hat{U}_N f_P E_{\mathrm{rr},DF}(I_{\mathrm{DC}},U_B)}{4\pi U_B} \tag{63}$$

where $E_{T,\mathrm{ON}}(I_{\mathrm{DC}},U_B)$, $E_{T,\mathrm{OFF}}(I_{\mathrm{DC}},U_B)$, and $E_{\mathrm{rr},DF}(I_{\mathrm{DC}},U_B)$, which can be obtained directly from the manufacturers datasheet are the turn-on, turn-off, and reverse recovery energy modeled as function of the forward current and the reverse voltage U_B.

The total averaged power loss of the diodes and IGBTs, $P_{T/DF}$, can be determined using

$$P_{T/DF} = P_{T/DF,c} + P_{T/DF,s}. \tag{64}$$

Finally, as for the SR, the power losses and stresses across the passive components of the six-switch buck-type PFC rectifier can be determined by (37)–(58).

B. Efficiency and Chip Area Comparison

Fig. 16 presents the breakdown of the total losses for the SR and the six-switch buck-type PFC rectifier, both specified according to Tables II and IV. As can be observed the SR can achieve the highest efficiency, justifying its implementation for the project at hand.

Although the efficiency comparison gives a good overview regarding the expected performance of the analyzed topologies, it can be considered not completely fair. This is particularly true because the selected IGBT and diode devices for each topology are not individually optimized. Therefore, some devices can be found overdimensioned while others can be brought to operate

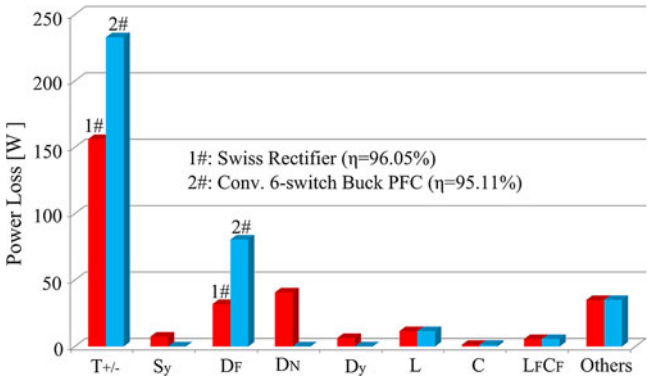

Fig. 16. Comparative evaluation: Breakdown of the total losses for operation at $P_o = 7.5\,\mathrm{kW}$, $u_{pn} = 400\,\mathrm{V}$, $u_{a,b,c} = 230\,\mathrm{V_{rms}}$ and $f_P = 36\,\mathrm{kHz}$.

at their limits. For a fair comparison, the semiconductor chip sizes of each rectifier could be adapted for a given operating point such that the maximum or average IGBT and diode junction temperatures, $T_{J,T/D}$, are equal to or less than a predefined maximum value, i.e., $T_{J,\max} = 125\,^{\circ}\mathrm{C}$. This strategy not only guarantees optimal chip area partitioning and semiconductor material usage, but also provides a common basis for comparisons [26] and [27].

Due to their good documentation and data availability, the Infineon Trench and Field Stop 1200 V IGBT4 and 600 V IGBT3 series have been chosen as the data basis. With a statistical analysis of many commercial devices, datasheets and manufacturer data, the power losses and thermal characteristics of these semiconductor series can be modeled with a chip die size, $A_{S,T/D}$. A thorough description of the employed chip area optimization, including the resulting expressions for the power loss of the IGBTs and diodes and thermal characteristics modeled with a nominal chip area, are given in [27].

In this paper, using the derived chip area mathematical expressions, the optimization algorithm calculates the losses of each topology and chip sizes until the average junction temperature of each semiconductor chip reaches $T_J = 125\,^{\circ}\mathrm{C}$, assuming a heat sink temperature of $T_{\mathrm{Sink}} = 80\,^{\circ}\mathrm{C}$. By summing up all optimized chip sizes, the total chip area, the semiconductor costs, and the total efficiency for a topology and corresponding operation point can be found. Therein, the chip area of each element is limited to a minimum of $A_{S\min} = 2\,\mathrm{mm}^2$. This is due to unconsidered side effects becoming dominant for small chip sizes and the limits in bonding technology.

Fig. 17 shows the chip area optimization results for the specified 7.5 kW SR and the six-switch buck-type PFC system (cf., Table II). Therein, the total chip area is calculated depending on the switching frequency. As can be noticed, the results confirm the initial efficiency calculations (cf., Fig. 16), as the SR is the solution that requires the lowest semiconductor chip area. The part count and the count for external circuitry such as isolated gate drivers is increased, but the total cost of the semiconductors can be expressively lower, especially for high-switching frequencies. Accordingly, the SR is the topology of choice for the specified buck-type PFC rectifier.

The main advantage of the SR is not only seen in the higher achievable efficiency but also that the system can be controlled

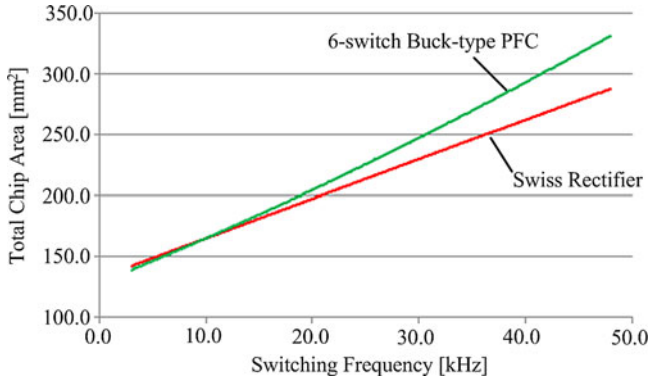

Fig. 17. Comparative of the total semiconductor chip area as function of the operating switching frequency.

similar to a dc–dc converter. Accordingly, basic knowledge of the function of a buck-type dc–dc converter and a three-phase passive diode rectifier is sufficient to implement a three-phase PFC rectifier with sinusoidal input currents and a controlled output voltage.

VII. Conclusion

This paper deals with a three-phase unity power factor buck-type PFC rectifier, named the SR, appropriate not only for high-power EV battery charging systems, but also for power supplies for telecommunication, future more electric aircraft, variable speed ac drives, and high-power lighting systems.

The complete design procedure of this system is based on analytical expressions of the current stresses of the active and passive power components, including a simplified EMI DM/CM modeling for conducted emission and filter design, as well as the control analysis, has been described. Additionally, a 7.5 kW SR hardware prototype has been implemented and its feasibility has been verified. Finally, the new rectifier concept has been compared with a conventional six-switch buck-type PFC rectifier. According to the results, the SR is a very suitable topology for the implementation of a buck-type PFC mains interface for an EV battery charger.

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