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Weight and Efficiency Analysis of Switched Circuit Topologies for Modular Power Electronics in MEA

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***Abstract*—This paper details weight and efficiency analysis of a bidirectional $\pm 270\,\mathrm{V}$ dc to 3-phase $115\,\mathrm{V}$ ac power electronic interface as part of an integrated modular power electronics cabinet, which supplies various loads, such as motors and ac buses from a HVDC bus in more electric aircraft. Through a case study the analysis shows that a significant reduction of filter component weight is achieved with a 3-level instead of a 2-level topology. The interactions and trade offs between the power electronic switched circuits and the EMI filter are analyzed and quantified. The potential benefits through the use of SiC-MOSFET's instead of Si-IGBTs and the implications for the circuit topologies are detailed. Recommendations for the choice of the optimal switched circuit topology, dependent on the importances of efficiency, weight, and reliability, are proposed. Furthermore, recommendations for the focus of future research enabling the competitiveness of the MEA concept is given.**

I. Introduction

The more electric aircraft (MEA) concept aims to reduce operating costs, fuel consumption, and the environmental impact of future air travel, through the replacement of pneumatic and/or hydraulic systems with electrical systems [1]. The replacement of the bleed air systems with electrical systems, for example, can save roughly $35\,\%$ of power from the engine [2]. Although great benefits of the MEA concept have been identified, it also links great challenges related to the requirements for power electronic systems, i.e. high power densities (weight and volume), efficiency, reliability, availability, and reduced cost [1]–[8]. In 2009 Prissé suggests to address these challenges through modular interconnections of power converters and loads [9]. The approach by Prissé takes the power requirements during the different flight phases and the limited reliability of power electronic components into account. Through redundancy and load sharing/shifting the weight of the sum of all power converters can be decreased while simultaneously the system availability is increased. This approach led to numerous publications aimed at the optimization of the complete MEA electrical system [10]–[13]. Predominately the tradeoff between semiconductor cooling and filtering efforts are analyzed. In [14] Bourdon outlines that the emergence of wide band gap (WBG) semiconductor devices and their associated packaging/integration and cooling solutions are key enabling technologies for the MEA concept. However, the rapid developments in power electronics created a gap between the state of the art in aircraft systems and other industries, e.g. automotive industry and university level research, due to higher safety and reliability requirements and the associated certification process of aircraft systems. Within the scope of the EU research and innovation program Horizon2020, the I^{2}MPECT project [16], coordinated by SIEMENS in association with industry partners and academia, aims to bridge this gap and create synergies for the aircraft industry with other industries. The goals of the I^{2}MPECT project are the following:

- Increase efficiency, power density and power to weight ratio of power electronic conversion systems through the use of wide bad gap (WBG) devices.
- Demonstrate increased reliability and efficiency by use of advanced packaging and thermal management solutions.
- Enable reduced maintenance cost and increase availability by employing health monitoring techniques.
- Reduce qualification and certification cost through the availability of modularized power electronic modules.

The I^{2}MPECT project aims to demonstrate these achievements with a $45\,\mathrm{kW}$ 3-phase bidirectional dc-ac power converter featuring a power to weight ratio of $15\,\mathrm{kW/kg}$ ($6.8\,\mathrm{kW/lb}$) at an efficiency of $99\,\%$ for the power electronics core component, which consists of the semiconductor switches including gate drives, measurement equipment, and the dc-side filter components (excluding the ac side filter components). The power converter will be part of a mock-up system as described in [9].

This paper analyzes the influence of the selection of the switched circuit topology and it's components on the power conversion system with emphasis on the total system weight, efficiency and reliability. The system level benefits provided by the use of WBG devices are outlined. As a case study the interactions and trade offs between the power electronic switched circuit and the EMI filter of a $\pm 270\,\mathrm{V}$ dc to $115\,\mathrm{V}$ three-phase ac interface are analyzed.

Section II describes the influence of semiconductor technologies and circuit topologies on the system efficiency and the sizing of the cooling system. In Section III electro magnetic interference (EMI) issues and the need for electro magnetic compatibility (EMC) standards are addressed. EMI filter structures suitable for a lightweight implementation are proposed. Optimization algorithms, which yield low weight

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filter implementations, are detailed, important dependencies are outlined, and optimization results are presented. Section IV presents a discussion on the obtained results and gives a recommendation on the focus of further research. Finally Section V concludes.

II. Switched Circuits

In this section power electronic switched circuit topologies suitable for bidirectional dc-ac conversion are compared in terms of reliability, EMI emissions, and losses. The differences in conduction and switching losses of Si-IGBTs and SiC-MOSFETs are summarized. Finally, the scaling of the cooling system, which is the greatest contribution to the weight of the switched circuit, i.e. excluding filter components, is outlined.

A. Topologies

Three switched circuit topologies are considered to be relevant, where each 3-phase inverter system features 3 identical bridge legs: standard 2-level half bridge (HB), 3-level T-Type and 3-level NPC inverters [15]. Each circuit has advantages and disadvantages. The HB has the minimal component count and is most favorable in order to maximize reliability, but it also features the highest switching losses and EMI noise emissions, which increase filter component size and losses as well as EMI issues. Compared to the HB inverter the T-Type inverter reduces the switching losses and EMI noise emissions, because the switched voltage is devided by a factor of two. If the T-Type inverter is built with IGBTs it would inherently feature higher conduction losses, because of the bidirectional switch. However, if it is built with MOSFETs only a greater semiconductor area/cost is required to achieve the same conduction losses as the HB would generate. The use of a greater semiconductor area, for a given amount of total losses, also reduces the thermal stress of the semiconductor devices, and furthermore the heat spreading requirements of the cooling system are reduced. On the other hand additional gate drives and supplies are required, which increases the system complexity and has an adverse effect on system reliability and cost. Compared to the T-Type the NPC increases the component count and complexity even further, but enables the use of semiconductors with reduced blocking voltage capability. Because semiconductors with sufficient voltage blocking capabilities for this work are available, the NPC would be the least suitable solution in terms of reliability.

B. Power Semiconductors

Before the emergence of high voltage wide band gap (WBG) semiconductor devices, e.g. 1.2 kV SiC-MOSFETs, Si-IGBTs were the most feasible devices for high power inverters. Si-MOSFETs aren't suitable to be used in a power hard switched HB configuration, because of their parasitic body diode's large reverse recovery charge. A comparison of conduction and switching loss characteristics of 1.2 kV Si–IGBTs (IKW40N120H3) and SiC-MOSFETs (C2M0025120D) in a HB configuration is summarized in Fig. 1. It shows that the reduction of conduction losses through paralleling of single

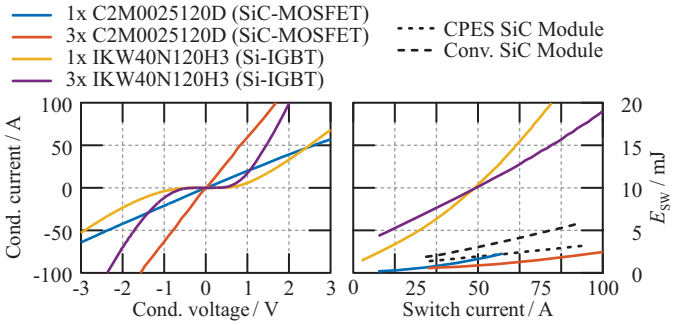

Fig. 1. Comparison of conduction (at 175 °C) and switching loss data ($E_{sw} = E_{on} + E_{off}$ at $V_{dc} = 600$ V) from the manufacturer's data sheets of the Si-IGBT IKW40N120H3 and the SiC–MOSFET C2M0025120D. And switching loss measurement data of 1200 V / 120 A SiC-modules ($V_{dc} = 540$ V) provided in [17].

devices is limited for IGBTs. The IGBT (and diode) require a significant forward voltage drop in order to conduct current, whereas SiC-MOSFETs do not have such a limitation. Fig. 1 also clearly shows that switching losses of SiC-MOSFETs are significantly smaller. However, the available switching loss data shows a large variance, because MOSFET switching losses show a high dependency on parasitic capacitances and inductances of the commutation and gate loop, as well as the employed gate drive circuitry. Hence the data is only meaningful for each specific combination of device, layout, and gate drive circuit. Due to the reduced conduction and switching losses WBG devices are more suitable for high efficiency and high power density inverters, however, limited data on reliability is available.

C. Cooling

Semiconductor cooling essentially deals with two thermodynamic problems: Heat dissipation and heat spreading.

Heat dissipation, e.g. [4], describes how the heat is delivered to the environment, e.g. the air outside the aircraft, and typically deals with heat and mass transfer of gases. Given the project specific boundary conditions, e.g. available mass flow and static pressure drop, the I^{2}MPECT project partners estimate a heat sink mass requirement of ≈ 500 g to dissipate ≈ 500 W of losses to the ambient. The heat sinks often feature a far greater interface area as the heat generating devices themselves, i.e. a large temperature difference between the heat sink and the device junction temperature may result, in which case heat spreading effects must be carefully considered.

Heat spreading, e.g. [18], describes how large the temperature difference between the hot spots, e.g. the semiconductor dies, and the heat dissipation device is, i.e. it requires the size and location of both: the heat sources (semiconductor dies) and the heat dissipating device (heat sink). If the difference in size between source and sink is large special heat spreading techniques, such as water cooling or the use of heat pipes, may be required.

In general it can be summarized that the weight requirement of the heat sink scales with the total losses to be dissipated and, depending on the ratio between size of the heat source

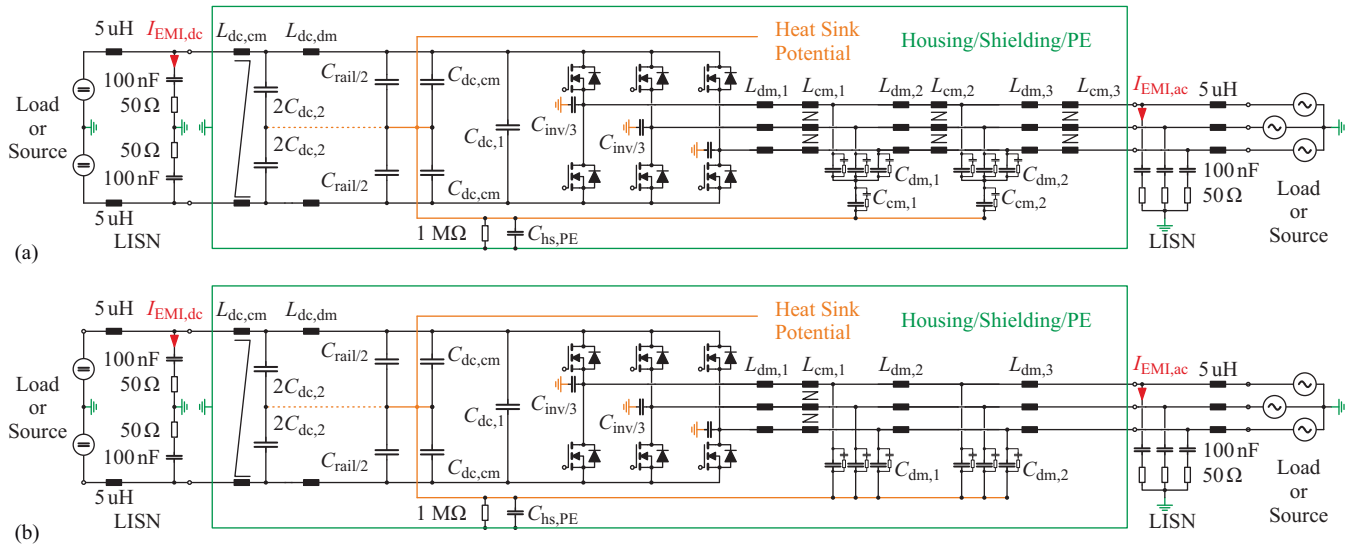

Fig. 2. Proposed EMI filter structure for 3–phase inverters (a) with and (b) without low frequency 3rd harmonic voltage injection modulation schemes. The source and load connections via line impedance stabilization networks (LISN) as described in the RTCA/DO-160 standard are indicated. For the derivation of the CM equivalent circuit, the protective earth (PE) connection scheme has to be defined as well.

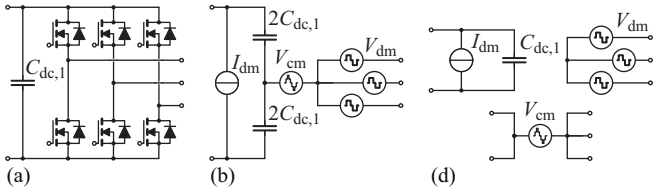

Fig. 3. Separation of DM and CM noise sources: (a) switched circuit (b) equivalent circuit generating the same voltage and current waveforms at the input/output terminals and (c) separation of DM and CM circuits through superposition.

and sink, special heat spreading techniques may be required, where an a priori prediction of the weight required for heat spreading is difficult.

III. EMI Filters

In this section electro magnetic interference (EMI) issues and the need for electro magnetic compatibility (EMC) standards are addressed. EMI filter structures suitable for a lightweight implementation are proposed. Optimization algorithms, which yield low weight filter implementations, are detailed, while important dependencies are outlined. Finally optimization results are presented.

A. EMI and EMC Standards

It is important to make a distinction between complying with EMC standards, such as RTCA/DO-160 or CISPR, and dealing with EMI issues. While a converter may function just fine without complying with an EMC standard, the effects of EMI issues range from reduced performance to failure or even inoperability of the converter in the first place. The most common issues are:

1) Measurement and signal distortion due to voltages induced by changing currents, e.g. a gate signal next to a power track is distorted because the $\mathrm{d}i/\mathrm{d}t$ in the power track creates a changing magnetic field $\mathrm{d}H/\mathrm{d}t$, which in turn induces voltages in the signal circuitry.
2) Measurement and signal distortion as well as insulation degradation due to CM currents, e.g. the gate drive of a HB's high side switch has a parasitic coupling C_{inv} to ground, which is charged/discharged by a current $i_{\mathrm{inv}} = \mathrm{d}v/\mathrm{d}t \cdot C_{\mathrm{inv}}$ during the switching transients. Depending on the amplitude of i_{inv} and path it flows through,

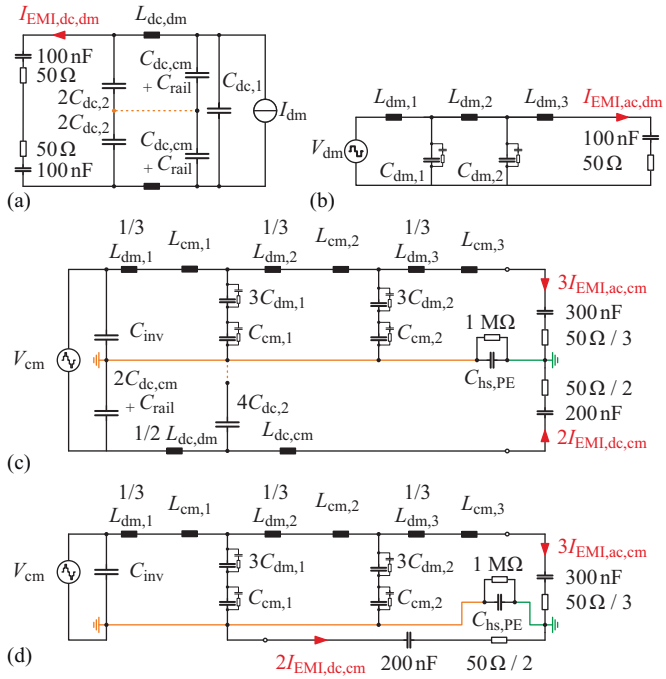

Fig. 4. Derived (a) dc-side DM, (b) ac-side DM, (c) CM equivalent circuits of the proposed EMI filter structure for 3–phase inverters with low frequency 3rd harmonic voltage injection modulation schemes, and (d) simplified CM equivalent circuit for $C_{\mathrm{inv}} \ll C_{\mathrm{dc,cm}}$.

the signal electronics may fail.

EMI issues are usually dealt with during the commissioning of the converter, while EMC standards apply where systems are interfaced with each other to ensure that they do not adversely affect each other, i.e. the converter in this work needs to comply with the RTCA/DO-160 standard at the dc-side and ac-side interfaces.

B. EMI Filter Structure

Fig. 2 (a) depicts the proposed EMI filter structure for 3–phase inverters with low frequency 3rd harmonic voltage injection modulation schemes. The filter structure is a slight modification of the one proposed in [19]. Without 3rd harmonic voltage injection the CM filter elements $L_{\text{cm,2}}$, $L_{\text{cm,3}}$, $C_{\text{cm,1}}$, and $C_{\text{cm,2}}$ can be omitted, as will be described in Section III-B3, which yields the filter structure shown in Fig. 2 (b). Further Fig. 2 shows the source and load connections via line impedance stabilization networks (LISN) as described in the RTCA/DO-160 standard. For the derivation of the CM equivalent circuit, the protective earth (PE) connection scheme has to be defined as well. All circuit elements in Fig. 2 represent physical components, except for the parasitic (capacitive) couplings between the heat sink and: the drain of the low side switches C_{inv}, the positive and negative rails C_{rail}, and PE $C_{\text{hs,PE}}$. Substitution of an equivalent circuit describing the behavior of the switched circuit, as described in [20] and shown in Fig. 3, enables the derivation of separate DM and CM equivalent circuits shown in Fig. 4. The choice and design of each component of the equivalent circuits is detailed in the following subsections.

The worst case EMI noise emissions as well as worst case component stresses need to be determined before the filter elements can be designed. The noise spectra of the current and voltage sources I_{dm}, V_{dm} and V_{cm} are obtained through fourier transformation of the current and voltage waveforms of the switched circuit, cf. Fig. 3. Both, the noise spectra and component stresses, are dependent on the modulation strategy, the operating point, the switched circuits topology, the switching frequency f_{sw}, and finally the current ripple in the first filter stage, i.e. the combination of the inductance value $L_{\text{dm,1}}$ and f_{sw}.

In this work a sinusoidal modulation strategy is chosen, since the $15\,\%$ additional output voltage amplitude gained by a low frequency 3rd harmonic voltage injection isn't required. Other modulation strategies are not considered, however the impact on the filter design is detailed. The ranges of operating points span: $\pm 45\,\text{kW}$ active and $\pm 2\,\text{kVA}$ reactive ac-line power, $200\,\text{Hz}$ to $2\,\text{kHz}$ fundamental frequency, $115\,\text{V} \pm 10\,\%$ rms ac-line, and $540\,\text{V} \pm 10\,\%$ dc-link voltage. Values for $L_{\text{dm,1}}$ between $1\,\mu\text{H}$ and $52\,\mu\text{H}$ with switching frequencies between $20\,\text{kHz}$ and $200\,\text{kHz}$ are considered. The design algorithms for the different filter circuits are detailed in the following subsections.

1) DC Side DM Filter: The design algorithm is visualized in Fig. 5. It ensures that the maximum voltage ripple is less

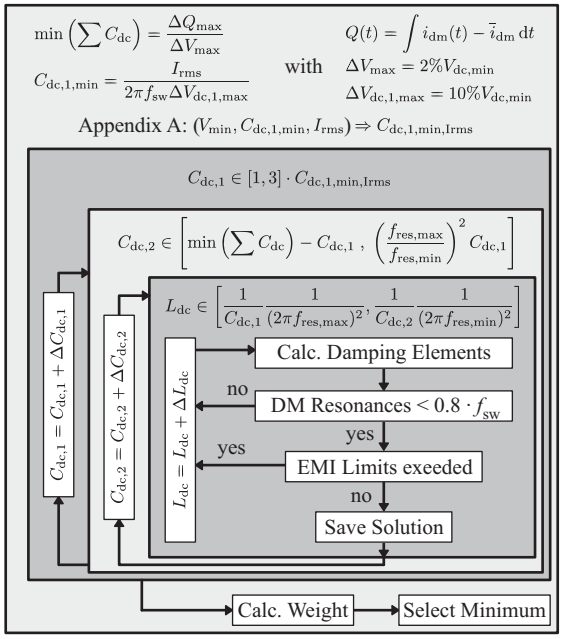

Fig. 5. Optimization algorithm flow chart and equations, which determine the low weight implementation of the dc-side EMI filter, while satisfying RTCA/DO-160 conducted EMI limits and resonance criteria.

than $2\,\%$ of the minimum dc-bus voltage for all frequencies and that the RTCA/DO-160 (category "L,M & H") conducted EMI limits aren't exceeded. Furthermore it ensures that none of the operating points excite any filter circuit resonances, which would ultimately lead to high damping losses and stresses of the filter components during steady state operation.

First the minimum total sum of the filter capacitances $\min\left(\sum C_{\text{dc}}\right) = C_{\text{dc,1}} + C_{\text{dc,2}}$ is calculated from the worst case charge $Q(t)$ injected by the switched circuit. Secondly the lightest combination of foil capacitors from the MKP1848, MKP1848C, and MKP1848s series is selected according to Appendix A, which features sufficient capacitance $C_{\text{dc,1,min}}$, current rating I_{rms}, and a minimum rated voltage V_{min}. V_{min} is chosen to be 1.5 times the maximum dc-link voltage. This yields a minimum feasible capacitance $C_{\text{dc,1,min,Irms}}$ for $C_{\text{dc,1}}$. The algorithm in Fig. 5 then determines the minimum inductance L_{dc}, which satisfies conducted EMI limits and resonance criteria for each of the swept combinations of $C_{\text{dc,1}}$ and $C_{\text{dc,2}}$. The resonance frequency of the filter is kept within $f_{\text{res,max}} = 0.8 \cdot f_{\text{sw}}$ and $f_{\text{res,min}} = 1.2 \cdot \max(f_{\text{fund}})$, where f_{fund} is the fundamental frequency of the output voltage. Furthermore the inductance L_{dc} is damped by a parallel damping resistor with high-frequency series blocking inductor according to [21] (with a value of $n = 10$). High reliability electrolytic capacitor series 095 PLL-4TSI, 152 RMH, 159 PUL-SI , and 198 PHR-SI are considered for $C_{\text{dc,2}}$.

The final step calculates the weight of all components according to Appendix A and selects the design featuring minimal total weight.

2) AC Side DM Filter: The design algorithm is visualized in Fig. 6. It ensures that the maximum voltage ripple after

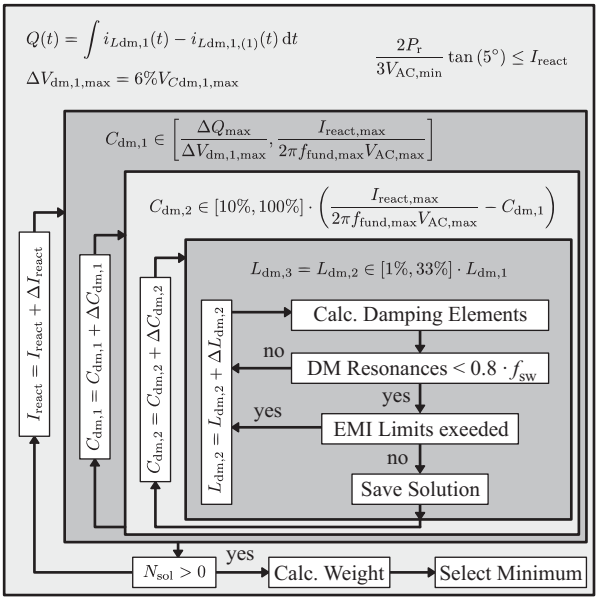

Fig. 6. Optimization algorithm flow chart and equations, which determine the low weight implementation of the ac-side DM EMI filter, while satisfying RTCA/DO-160 conducted EMI limits and resonance criteria.

the first filter stage, $\Delta V_{\text{dm,1,max}}$ is less than $6\,\%$ and that the RTCA/DO-160 (category "L,M & H") conducted EMI limits aren't exceeded. Furthermore it ensures that none of the operating points excite any filter circuit resonances.

A minimal reactive power consumption of the DM EMI filter which is equivalent to a $5\,^\circ$ phase shift between the fundamental voltage and current is assumed and considered with the corresponding current I_{react}. The maximum voltage ripple criterion $\Delta V_{\text{dm,1,max}}$ defines the lower boundary for $C_{\text{dm,1}}$ and I_{react} defines the upper boundary for the sum $C_{\text{dm,1}} + C_{\text{dm,2}}$. The algorithm in Fig. 6 then determines the minimum inductance values (with $L_{\text{dm,2}} = L_{\text{dm,3}}$) which satisfy the conducted EMI limits. With this, the two outer loops of the algorithm ensure that the filter's resonance frequencies are less than $f_{\text{res,max}} = 0.8\, f_{\text{sw}}$ [22]. Furthermore the resonances are damped at the capacitors $C_{\text{dm,1}}$ and $C_{\text{dm,2}}$ by shunt R-C_{d} damping networks according to [21] (with a value of $n = 0.05$). The ac-filtering film capacitor series MKP1847 is considered. If no solution can be found the algorithm repeats with an increased maximum reactive current consumption I_{react} of the EMI filter.

The final step calculates the weight of all components according to Appendix A and selects the design featuring minimal total weight.

3) CM Filter: The CM filter design can theoretically not be separated into a dc-side and ac-side analysis, cf. Fig. 4 (c), but it can be significantly simplified if the parasitic coupling between the positive and negative rail and the heat sink potential C_{rail} is artificially increased by low inductive CM capacitors $C_{\text{dc,cm}}$. Usually the parasitic couplings C_{inv} and C_{rail} define the distribution between the CM voltage noise amplitudes applied to the ac- and dc-side EMI filters, but with

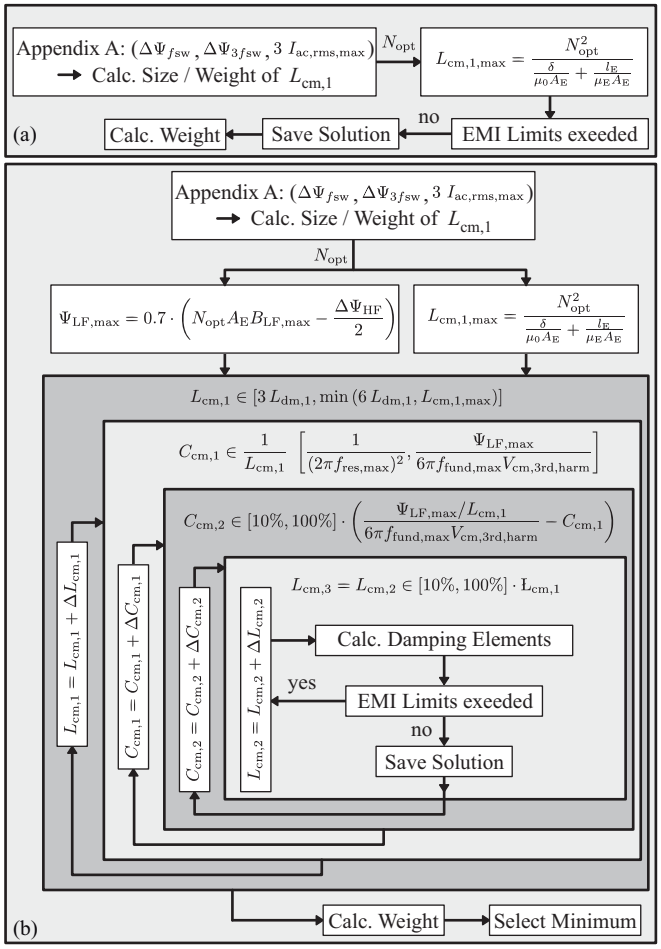

Fig. 7. Optimization algorithm flow chart and equations, which determine the low weight implementations of the ac-side CM EMI filters, while satisfying RTCA/DO-160 conducted EMI limits; (a) for sinusoidal modulation strategies and (b) for modulation strategies with low frequency CM voltage injection, e.g. 3rd harmonic injection.

$C_{\text{dc,cm}} \approx 500\, C_{\text{inv}}$ the dc-side is already virtually shielded from the CM voltage emissions. Furthermore, $C_{\text{dc,cm}}$ could easily be implemented to simultaneously function as a commutation loop bypass capacitor inside a power module. The DM filter stage $L_{\text{dc,dm}}$ - $C_{\text{dc,2}}$ should theoretically provide sufficient CM attenuation, but because electrolytic capacitors often feature an inductive behavior at frequencies well above $150\,\text{kHz}$, a small additional CM inductor $L_{\text{dc,cm}}$ will probably be required. Taking these considerations into account the equivalent circuit Fig. 4 (c) can be simplified to Fig. 4 (d), i.e. only the ac-side CM filter remains to be designed.

The ac-side CM filter design algorithms are visualized in Fig. 7 (a) for a sinusoidal modulation strategy and in Fig. 7 (b) for modulation strategies with low frequency voltage injection, e.g. 3rd harmonic, flat top, etc..

The size and weight of the CM inductor $L_{\text{cm,1}}$ will predominately be defined through thermal and efficiency considerations, while the value of $L_{\text{cm,1}}$ is preferably chosen to be as large as possible for a given minimal loss CM inductor design. This is because the linked flux in the CM inductor is (similar to a transformer) independent of the load current,

i.e. $\Psi_{\text{cm}} = i_{\text{cm}} L_{\text{cm,1}} = \int v_{\text{cm}}(t)\,\mathrm{d}t$. This implies that for a sinusoidal modulation strategy the CM filter design is reduced to the design of the CM mode inductor. The DM capacitances $C_{\text{dm,1}}$ and $C_{\text{dm,2}}$ are then directly connected to the feed back path, i.e. connected to the heat sink potential bypassing $C_{\text{cm,1}}$ and $C_{\text{cm,2}}$. In that case the CM inductance $L_{\text{cm,2}}$ and $L_{\text{cm,3}}$ can be omitted, since the CM attenuation of the first CM filter stage with $L_{\text{cm,1}}$ and $C_{\text{dm,1}}$ is very large. Furthermore the attenuation of the second DM filter stage with $L_{\text{dm,2}}$ and $C_{\text{dm,2}}$ provides the same attenuation for DM and CM voltages, if $C_{\text{cm,2}}$ is bypassed. Therefore the algorithm only estimates the size and weight of $L_{\text{cm,1}}$ according to Appendix A and verifies that the EMI limits are not exceeded.

For F3CC cut cores a minimal equivalent air gap of $\delta \approx 75\,\mu\text{m}$ has been determined experimentally. Because the determination of the maximum possible CM inductance for the given minimal loss inductor design made from cut cores requires the minimum possible air gap size δ, i.e. the cores and the number of windings are already selected due to the minimal loss inductor design. The analysis has shown that, for the specifications in this work, this approach always provides sufficient CM voltage attenuation.

For modulation strategies with low frequency CM voltage injection the same thermal and efficiency considerations apply, however, the peak value of the CM current i_{cm} needs to be limited in order to avoid saturation of $L_{\text{cm,1}}$. Since, by design, the filter capacitors $C_{\text{cm,1}}$ and $C_{\text{cm,2}}$ need to follow the low frequency component of the CM voltage $v_{\text{cm,LF}}$. The worst case low frequency CM current amplitude for 3rd harmonic voltage injection will be

$$\begin{aligned}\hat{i}_{\text{cm,LF}} &\approx \left(\sum C_{\text{cm,eq}}\right) \frac{\mathrm{d}v_{\text{cm,LF}}}{\mathrm{d}t} \\ &\approx \left(\sum C_{\text{cm,eq}}\right) \frac{\sqrt{2}}{6} V_{\text{ac,max}} \cdot 3 \cdot 2\pi f_{\text{fund,max}} \\ &\approx \left(\sum C_{\text{cm,eq}}\right) 1.124\,\frac{\text{A}}{\mu\text{F}}.\end{aligned} \tag{1}$$

Therefore the sum of the equivalent CM capacitances $\sum C_{\text{cm,eq}}$ should be kept small, which is achieved by series connection of $C_{\text{cm,1}}$ and $C_{\text{cm,2}}$ to $C_{\text{dm,1}}$ and $C_{\text{dm,2}}$, i.e. if a low frequency CM voltage injection is employed the value of $L_{\text{cm,1}}$ is limited by size of $\sum C_{\text{cm,eq}}$. Furthermore the series connection of $C_{\text{cm,1}}$ and $C_{\text{cm,2}}$ to $C_{\text{dm,1}}$ and $C_{\text{dm,2}}$ significantly reduces the CM voltage attenuation of the first and second DM filter stages and yields the necessity of the additional CM inductors $L_{\text{cm,2}}$ and $L_{\text{cm,3}}$. The optimization algorithm in Fig. 7 (b) selects the minimum weight CM filter implementation, which satisfies RTCA/DO-160 EMI emission limits and doesn't saturate $L_{\text{cm,1}}$.

C. Results

Fig. 8 shows the estimated weight of the EMI filter designs versus switching frequency. For each switching frequency the inductor $L_{\text{dm,1}}$ which yields minimum total filter weight is selected. The weight of the dc-side DM filter, $\approx 400\,\text{g}$, is almost independent of the switching frequency, because the size and weight of $C_{\text{dc,1}}$ is defined by it's current rating.

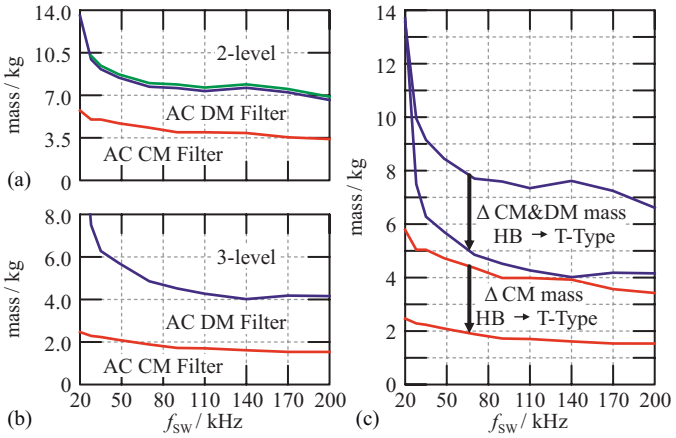

Fig. 8. Optimization results for the required EMI filter mass of (a) 2-level voltage waveform and (b) 3-level voltage waveform. (c) shows the potential EMI filter weight reduction from a HB to a T-Type topology, which predominantely originates from the reduced CM filter losses.

Both the weights of the ac-side DM and CM filter monotonically decrease up to a switching frequency of about 100 kHz. The most significant result however is highlighted in Fig. 8 (c) and shows that the difference between the EMI filter weights of 2-level and 3-level voltage waveforms is $\approx 3\,\text{kg}$, which is the target weight of the power electronics stage including the cooling system, dc-side filter stage, housing, as well as auxiliary and control functions. Furthermore, Fig. 8 (c) shows that the difference in weight largely stems from the difference in mass of the CM inductor $L_{\text{cm,1}}$, whose size is predominately a function of it's losses and cooling, i.e. it can be translated into an approximate difference in losses of $\approx 70\,\text{W}$.

IV. Discussion

This paper summarizes the design challenges of power electronics for aerospace applications and quantifies the approximate weight of the EMI filter for a typical $\pm 270\,\text{V}$ dc to $115\,\text{V}$ three-phase ac grid interface. In order to perform a full system weight and efficiency optimization the characteristic of weight and efficiency versus switching frequency of the semiconductor power stage is also required. There the losses of the semiconductors and the weight of the cooling system will monotonically increase with the switching frequency. The switched circuit's conduction losses will define the offset of its loss versus switching frequency characteristic and the switching losses will define the slope. The conduction losses can be reduced by using multiple MOSFETs in parallel, but the switching losses should (from a device physics point of view) increase with a greater chip area, i.e. optimal combinations of: switching frequency, number of parallel MOSFET dies, and EMI filter designs do exist.

However, the great discrepancies between switching loss data provided in the manufacturer's data sheets (or lack of data), as well as published measurement results, cf. Fig. 1, shows that SiC-MOSFET switching losses are not dominated

by the semiconductor device physics, but the combination of package parasitics and employed gate drive circuit. Therefore the I²MPECT project strives to develop a power electronic module, which features a layout and gate drive combination that is optimized for minimal switching losses independent of the employed switched circuit topology. Furthermore it has been shown that a high frequency capacitive current feed back path as an interface for either the EMI filter or potentially only a $^{\mathrm{d}v}/_{\mathrm{d}t}$ filter in case of a motor load needs to be provided. It should be mentioned that a CM filter may also be required for a motor load.

V. Conclusion

This paper summarizes the design challenges of power electronics for aerospace applications and quantifies the approximate weight of the EMI filter for a typical $\pm 270\,\mathrm{V}$ dc to $115\,\mathrm{V}$ three-phase ac grid interface for 2-level and 3-level inverters. The choice of the optimal topology depends on the weighting of importance between reliability, efficiency, weight and acquisition or life cycle cost. If reliability is absolutely most important the choice will be the standard 2-level inverter due to minimal component count and complexity. If overall system weight and efficiency are of higher importance a 3-level topology will be the obvious choice, since it will reduce the weight and losses of components with magnetic circuits, such as filters and motors [15]. For example, if the I²MPECT project's $45\,\mathrm{kW}$ 3-phase bidirectional dc-ac power converter demonstrator achieves the power to weight ratio of $\gamma \approx 15\,\mathrm{kW/kg}$ ($6.8\,\mathrm{kW/lb}$) and efficiency of $\eta \approx 99\,\%$ at a switching frequency of $48\,\mathrm{kHz}$, the corresponding EMI filter for a 2-level circuit topology features $\gamma \approx 5.3\,\mathrm{kW/kg}$ ($2.4\,\mathrm{kW/lb}$) and $\eta \approx 99.2\,\%$. This yields an over all performance of $\gamma \approx 3.9\,\mathrm{kW/kg}$ ($1.77\,\mathrm{kW/lb}$) and $\eta \approx 98.2\,\%$. Whereas the corresponding EMI filter for a 3-level circuit topology features $\gamma \approx 7.9\,\mathrm{kW/kg}$ ($3.58\,\mathrm{kW/lb}$) and $\eta \approx 99.5\,\%$ and yields an over all performance of $\gamma \approx 5.2\,\mathrm{kW/kg}$ ($2.36\,\mathrm{kW/lb}$) and $\eta \approx 98.5\,\%$, i.e. choosing a 3-level instead of a 2-level topology can reduce the over all system weight by $\approx 33\,\%$ while increasing the system efficiency.

Finally, if cost is the deciding factor a complete life cycle cost analysis becomes necessary. This would then requires a great deal of additional information, such as: the price of fuel, the additional fuel required per additional kg of weight, the fuel required per additional kWh of electric energy, the converters load profile and expected life cycle, as well as acquisition, qualification and certification costs.

Appendix A
Component Weight Models

This Section details the capacitor and inductor weight models required for the EMI filter optimization algorithms.

A. Capacitors

The aim of the capacitor weight model is to select a capacitor, which simultaneously fulfills a minimum capacitance requirement C_{min}, current capability I_{min}, and rated operating voltage V_{min}. To that end, lists containing the capacitance C, current capability I, rated voltage V, and associated mass m_{cap} are created based on the information provided in the data sheets from the manufacturers. For each capacitor in the list the minimum number of parallel capacitors to achieve the capacitance and current rating is determined

$$N_{C,\mathrm{min}} = \left\lfloor \frac{C_{\mathrm{min}}}{C} \right\rfloor \quad \text{and} \quad N_{I,\mathrm{min}} = \left\lfloor \frac{I_{\mathrm{min}}}{I} \right\rfloor . \tag{2}$$

Consequently the required number of capacitors in parallel and associated mass in order to satisfy both constraints is

$$N_{\mathrm{min}} = \max\left(N_{C,\mathrm{min}}, N_{I,\mathrm{min}}\right) \quad \text{and} \quad m_{\mathrm{tot}} = N_{\mathrm{min}} \cdot m_{\mathrm{cap}}. \tag{3}$$

Finally the capacitor, which has the minimum weight m_{tot} is selected.

B. DM & CM Inductors

The aim of the magnetic component weight model is to estimate the minimum required weight, with which the magnetic component can be realised. The total losses, P_{loss}, composed of conduction and core losses, need to be less than the maximum heat, which can be dissipated

$$P_{\mathrm{loss}} = \underbrace{V_{\mathrm{w}} k_{\mathrm{w}} \rho_{\sigma,\mathrm{w}} S_{\mathrm{rms}}^2}_{P_{\mathrm{loss,winding}}} + \underbrace{V_{\mathrm{c}} k_{\mathrm{c}} f^{\alpha} B_f^{\beta}}_{P_{\mathrm{loss,core}}} \leq O h \Delta T. \tag{4}$$

Where V_{w}, k_{w}, $\rho_{\sigma,\mathrm{w}}$ are the total winding volume, packing factor and conductivity, S_{rms} the average conductor current density, V_{c} the core volume, k_{c}, α, β the Steinmetz Parameters, B_f and f are the (sinusoidal) magnetic field amplitude and frequency, O the surface of the magnetic component, and $h\Delta T$ the product of average heat transfer coefficient and difference between the ambient and the component temperature. The parameter $h\Delta T$ is dependent on the thermal connection to the surrounding environment. In this work $h\Delta T = 2000\,{}^{W}/_{\mathrm{m}^2}$ is chosen, i.e. some sort of forced cooling is assumed. The size of the magnetic core must be large enough, such that

$$\Psi_f I_{\mathrm{rms}} \leq \underbrace{B_f A_{\mathrm{e}}}_{\Psi_{f/N}} \underbrace{S_{\mathrm{rms}} k_{\mathrm{w}} A_{\mathrm{w,eff}}}_{N I_{\mathrm{rms}}} \tag{5}$$

holds true, where Ψ_f is the required flux linkage amplitude, I_{rms} the required rms value of the inductor current, A_{e} the core cross sectional area, and $A_{\mathrm{w,eff}}$ the effective winding cross sectional area (excluding the space required for the bobbin). The requirements Ψ_f, I_{rms} and linked flux frequency, f, can be extracted from the circuit simulations, i.e. as a first order approximation from the waveforms spectral decompositions. All remaining parameters except for the allowed flux amplitude B_f and current density S_{rms} can be extracted from material data sheets, available core geometries, and winding geometry considerations.

B_f will either be constrained by the core material saturation flux density, B_{sat}, or the permissible losses

$$B_f = \min\left(B_{\mathrm{sat}}, \left[\frac{P_{\mathrm{loss}} - V_{\mathrm{w}} k_{\mathrm{w}} \rho_{\sigma,\mathrm{w}} S_{\mathrm{rms}}^2}{V_{\mathrm{c}} k_{\mathrm{c}}}\right]^{\frac{1}{\beta}} \cdot f^{-\frac{\alpha}{\beta}}\right). \tag{6}$$

TABLE I
MATERIAL PROPERTIES/PARAMETERS FOR THE INDUCTOR DESIGN

material	Core Material Parameters B_{sat} T	β	k_{c}	α W/m^3	ρ_{c} kg/m^3
AMCC	1.2	1.740	1.3773	1.5100	7180
F3CC	1.0	2.117	0.0239	1.7281	7300
N87(25°C)	0.33	2.385	10.5505	1.2930	4850
N87(100°C)	0.33	2.747	1.5179	1.4701	4850

material	Winding Parameters $\rho_{\sigma,\text{cu}}$ Ωm	ρ_{w} kg/m^3	k_{w}	bobbin margin mm
Rect. copper	2.07E^{-8}	8920	0.7	2

Substituting B_{sat} for B_f in (4) yields the allowed current density for magnetic saturation limited designs

$$S_{\text{rms,sat}} = \sqrt{\frac{P_{\text{loss}} - V_{\text{c}} k_{\text{c}} f^{\alpha} B_{\text{sat}}^{\beta}}{V_{\text{w}} k_{\text{w}} \rho_{\sigma,\text{w}}}}, \tag{7}$$

and substituting (6) into (5) yields the optimal current density in case of core loss limited designs:

$$\frac{\partial(\Psi_f I_{\text{rms}})}{\partial S_{\text{rms}}} = 0 \;\Rightarrow\; S_{\text{rms,opt}} = \sqrt{\frac{P_{\text{loss}}}{V_{\text{w}} k_{\text{w}} \rho_{\sigma,\text{w}}} \frac{\beta}{2+\beta}}. \tag{8}$$

This approach yields a mapping between the electrical requirement $\Psi_f, I_{\text{rms}}, f$ and the magnetic component weight, m_{mag} (neglecting skin and proximity effects). Since for any given core geometry in combination with the employed winding technology (which defines k_{w} and $\rho_{\sigma,\text{w}}$) the maximum possible $\Psi_f I_{\text{rms}}$ product can be expressed as a function of the linked flux frequency, f,

$$\Psi_f I_{\text{rms}} \leq A_{\text{e}} A_{\text{w,eff}} k_{\text{w}} S_{\text{rms,opt}} \left[\frac{P_{\text{loss}} - V_{\text{w}} k_{\text{w}} \rho_{\sigma,\text{w}} S_{\text{rms,opt}}^2}{V_{\text{c}} k_{\text{c}}} \right]^{\frac{1}{\beta}} f^{-\frac{\alpha}{\beta}} \tag{9}$$

in case of core loss limited designs and

$$\Psi_f I_{\text{rms}} \leq A_{\text{e}} A_{\text{w,eff}} k_{\text{w}} \sqrt{\frac{P_{\text{loss}} - V_{\text{c}} k_{\text{c}} f^{\alpha} B_{\text{sat}}^{\beta}}{V_{\text{w}} k_{\text{w}} \rho_{\sigma,\text{w}}}}\; B_{\text{sat}} \tag{10}$$

in case of saturation limited designs.

Finally the minimum weight magnetic component, which satisfies (9) and (10) is selected.

The designs consider amorphous and nanocrystalline cores from Hitachi Metals and various N87 ferrites from TDK. The material properties and parameters are summarized in Table I.

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