Three-Phase Sinusoidal Output Buck-Boost GaN Y-Inverter for Advanced Variable Speed AC Drives

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Three-Phase Sinusoidal Output Buck-Boost GaN Y-Inverter for Advanced Variable Speed AC Drives

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Abstract—Motor drive systems supplied by a fuel-cell/battery are especially demanding when it comes to the design of the inverter. Besides a high performance (high efficiency $\eta$ and power density $\rho$), the inverter has to cope with the wide DC voltage variation of the fuel-cell/battery that supplies the motor drive. A promising three-phase inverter topology, denoted as Y-VSI, is presented in this paper. The Y-VSI is a modular three-phase inverter, and comprises three identical phase-modules connected to a common star “$Y$” point. Each phase-module is equivalent to a buck-boost DC/DC converter, which allows the AC output voltages to be higher or lower than the DC input voltage. Thereby, the Y-VSI effectively copes with the wide variation of the fuel-cell/battery voltage. Each phase-module can be operated in a similar fashion to a conventional DC/DC converter, independently of the remaining two phases. Accordingly, a straightforward and simple operation/control of the Y-VSI is possible. In addition, the Y-VSI features an integrated output filter. This allows for continuous/sinusoidal motor voltage waveforms, eliminating the need of an additional filter between the inverter and the motor. This paper details the operating principle of the Y-VSI, and comparatively evaluates two modulation strategies. In order to validate the proposed concepts, a Y-VSI hardware prototype is drawn, while the fuel-cell voltage is decreasing as the drawn current increases [6]. The inverter has to always guarantee the full speed range of the motor. That is, the inverter must be able to generate the nominal motor voltage, which is proportional to the motor speed, independent of the input voltage fluctuation. It is noted, that similar consideration apply

I. INTRODUCTION

The electrification of vehicles has created new application opportunities for the power electronics industry [1]–[3]. One such application example is shown in Fig. 1(a). There, a 10 kW fuel-cell is depicted, which is part of a fuel-cell vehicle powertrain. An auxiliary drive system controls a high-speed 1 kW electric compressor, which in return provides the required oxygen for the fuel-cell unit operation [4]. This compressor drive system is directly supplied by the fuel-cell DC voltage $U_i = 60$ V...120 V and uses 10% of the fuel-cell power. The employed high-speed 280 krpm electric compressor [5] has a nominal phase voltage amplitude of $\hat{U}_o = 40$ V. The system specifications are summarized in Tab. I.

In general, motor drives placed on board of vehicles, demand efficient inverter systems in a small form factor. Besides the high performance, the new generation of inverter systems is expected to offer additional functionalities: (i) Buck-boost operation. The inverter system must cope with the wide voltage variation of a fuel-cell. The fuel-cell voltage is highly dependent on the operating point, as depicted in Fig. 1(b). The fuel-cell voltage is high when no current is drawn, while the fuel-cell voltage is decreasing as the drawn current increases [6]. The inverter has to always guarantee the full speed range of the motor. That is, the inverter must be able to generate the nominal motor voltage, which is proportional to the motor speed, independent of the input voltage fluctuation. It is noted, that similar consideration apply

Fig. 1: Motor drive application. (a) An electric compressor provides oxygen to the fuel-cell, while a motor drive, directly supplied by the same fuel-cell, controls the electric compressor. (b) Fuel-cell voltage-current characteristics.

TABLE I: Specifications of Fig. 1 motor drive. The nominal operating condition is highlighted in bold.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fuel-cell voltage</td>
<td>$U_i = 60$ V...120 V</td>
</tr>
<tr>
<td>Fuel-cell power</td>
<td>$P = 0$ W...10 kW</td>
</tr>
<tr>
<td>Inverter output freq.</td>
<td>$f_m = 0$ Hz...5 kHz</td>
</tr>
<tr>
<td>Inverter power</td>
<td>$P = 0$ W...1.1 kW</td>
</tr>
<tr>
<td>Motor speed</td>
<td>$n = 0$ rpm...280 krpm</td>
</tr>
<tr>
<td>Motor voltage</td>
<td>$\hat{U}_m = 0$ V...40 V (phase, PK)</td>
</tr>
<tr>
<td>Motor power</td>
<td>$P = 0$ W...1 kW</td>
</tr>
</tbody>
</table>
for inverters supplied by a battery. In this case, the DC input voltage can significantly fluctuate, depending on the charging status and the operating temperature of the battery.

(ii) High quality motor voltage. High-speed motors are an essential component of power dense motor drives, thanks to their small volume/weight. However, such motors are sensitive to poor current quality, which induces high rotor losses [7], [8]. Therefore, the inverter must guarantee high quality, sinusoidal motor voltages/currents. In addition, the fast switching speeds of the latest generation of wide-bandgap (WBG) semiconductor devices cause high $\frac{du}{dt} > 30$ kV/µs [9], [10], which poses a great concern for the motor reliability. The most common problem is premature bearing failure due to high common-mode (CM) $\frac{du}{dt}$ [11]–[13]. For the above reasons, a DM/CM sine-wave output filter must be placed between the inverter and the motor.

There has been extensive research in literature, towards inverter topologies with a wide input-to-output voltage ratio. A conventional voltage source inverter (VSI), only features buck-type functionality, hence cannot be directly used in the examined application. However, by exchanging the DC link capacitor of a VSI, with an $LC$ DC link impedance network, then the $Z$-source inverter (ZSI) is derived [14], [15]. The ZSI utilizes shoot-through zero states [16], [17], and its unique DC link impedance network, in order to achieve buck-boost capability, i.e. generates AC output voltages which are higher or lower than the input voltage. However, the ZSI suffers from increased voltage/current stress under boost operation, a fact that effectively limits its usability [18]–[20].

Buck-boost inverters with two energy conversion stages, as shown in Fig. 2, have found broad acceptance. In order to enable boost functionality, a boost-type DC/DC converter is placed before a VSI. The dedicated boost-type DC/DC converter (DC/DC stage) adapts the fluctuating input voltage $U_i$ to a higher DC link voltage $U_{DC}$, when necessary. The DC link voltage supplies the VSI, which generates the AC motor voltages ($DC/AC$ stage). A DM/CM filter is placed after the VSI in order to ensure high quality voltage for the motor. This popular inverter solution is denoted as boost-VSI (B-VSI). A two-stage inverter [21]–[24] processes the transmitted power twice, first in the DC/DC stage and then in the DC/AC stage, thus the overall performance is compromised. The increased number of inductive components and semiconductor losses originating from the DC/DC stage result in a low efficiency and a relatively large volume.

A current source inverter (CSI) based solution can be used instead of the B-VSI [25], [26]. The CSI is inherently a boost-type inverter [27]–[29], i.e. it generates AC output voltages which are strictly greater than the input voltage. In order to enable buck functionality, in addition to the inherent boost functionality of the CSI, a buck-type DC/DC converter must precede the CSI. Therefore, a two-stage inverter topology results, denoted as buck-CSI (B-CSI) [30], [31]. The switches of the CSI have to be realized with two anti-series connected devices (two anti-series MOSFETs or a MOSFET anti-series connected with a diode) [32], a fact that potentially leads to higher complexity, reliability concerns and higher conduction losses. This is a drawback of the B-CSI which limits its practical use.

In response to the shortcomings of the state-of-the-art inverter solutions, the Y-VSI inverter topology [33], [34] of Fig. 3, is proposed in this paper. The Y-VSI is based on the well established idea of modular three-phase inverters [35]–[41], where three identical DC/DC converters are connected to a common star “Y” point. In the case of the Y-VSI, each phase-module is equivalent to a non-isolated buck-boost DC/DC converter, while the three phase-modules are connected to the negative DC rail $n$ (star point). The modular concept employed by the Y-VSI is highlighted in Fig. 4. The Y-VSI benefits from four key features:

(i) Buck-boost capability. Thanks to the inherent buck-boost characteristics of each phase-module, the AC output voltage can be higher or lower than the DC input voltage.

(ii) High efficiency. The Y-VSI processes the transmitted power $P$ in a unique way. In the typical case, only three out of the six half-bridges are switched, at any given point in time. As a result, low switching losses are generated and a high inverter efficiency is achieved.

(iii) High quality motor voltage. The Y-VSI features an integrated $L_o - C_o$ output filter, hence generates continuous/sinusoidal motor voltages. Therefore, no additional filter is required, between the inverter and the motor.

(iv) Simple control strategy. Each phase-module can be controlled independently of the remaining two phases and employs a simple control configuration, similar to conventional DC/DC converters.

In a first step, the operating principle of the Y-VSI is explained in Sec. II. In particular, two modulation strategies are proposed, while the uncomplicated control of the Y-VSI is highlighted. In Sec. III, the voltage/current stresses on the different inverter components are analytically derived, and are followed by a comprehensive design guideline. The proposed concept is experimentally validated in Sec. IV. A Y-VSI hardware prototype and a conventional B-VSI hardware prototype are purposely assembled and compared for the specifications of Tab. I. The experimental results validate the performance benefits derived from the Y-VSI technology. Finally, the conclusions are drawn in Sec. V.

II. OPERATION PRINCIPLE

A three-phase inverter system can be constructed in a modular way [36]–[41] as is visualised in Fig. 4. Three identical phase-modules, each comprising a non-isolated DC/DC converter, are connected to a common star “Y” point. Following this modular inverter concept, the Y-VSI of Fig. 3 consists of three buck-boost DC/DC converters [42] connected to the negative DC rail $n$ (star point). The phase $a$ module comprises two half-bridges, the buck half-bridge $a_1$ and the boost half-bridge $a_2$, connected to the opposite terminals of an inductor $L_o$. When the inverter output voltage is lower than the input voltage $u_{in} \leq U_i$, the Y-VSI operates in buck regime of Fig. 5(a), where only the buck half-bridge $a_1$ is switched.
For the sake of simplicity, the motor voltage is considered to be in phase with the motor current, i.e. unity power factor $\cos(\phi) = 1 \leftrightarrow \phi = 0$. The modulation index that relates the motor phase voltage amplitude $U_m$ to the fuel-cell voltage $U_i$ is defined

$$M = \frac{U_m}{\pi U_i}. \tag{3}$$

The modulation index $M$ can exceed the value of $2/\sqrt{3}$, which is the limit of a conventional VSI, thanks to the inherent buck-boost capability of the Y-VSI. Each phase-module is independent of the remaining two phases, thus the analysis is from now focused on phase $a$, when possible.

A. Sinusoidal Modulation (SPWM)

The sinusoidal motor voltage $u_{ao}$ cannot be directly generated by phase-module $a$. The motor phase voltage $u_{ao}$ assumes negative values, during the negative half-cycle ($\pi/2 < \varphi < 3\pi/2$), while the output voltage of the phase $a$ module (DC/AC converter) must be strictly positive $u_{an} \geq 0$. Instead of sinusoidal voltages, the phase-modules $\{a, b, c\}$ generate sinusoidal voltages with an offset $u_{off}$

$$u_{an}(t) = \tilde{U}_m \cos(\omega_m t) + u_{off}, \tag{4}$$

$$u_{bm}(t) = \tilde{U}_m \cos(\omega_m t - \pi/3) + u_{off},$$

$$u_{cn}(t) = \tilde{U}_m \cos(\omega_m t + \pi/3) + u_{off},$$

such that the output voltages remains always positive e.g. $u_{an}(t) \geq 0$. In a first step, a constant offset voltage is selected

$$u_{off} = \tilde{U}_m. \tag{5}$$

Therefore, three sinusoidal voltages with the same constant offset voltage are generated with respect to the Y-VSI star point $n$. The phase $a$ output voltage is

$$u_{ao}(\varphi) = \tilde{U}_m(\cos(\varphi) + 1). \tag{6}$$

The Y-VSI output voltages in this case are visualized in Fig. 6(a). Even though the inverter output voltages are offsetted sinusoids, the line-to-line voltages $u_{ab}$, $u_{bc}$ and $u_{ca}$ are sinusoidal. Accordingly, sinusoidal motor phase currents/voltages appear. Since the inverter output voltages have an offsetted...
sinusoidal shape, the current modulation strategy is denoted as sinusoidal pulse width modulation (SPWM). It is noted that, the offset voltage \( u_{off} = U_m \) is common to all three phases and hence constitutes by definition a common-mode (CM) voltage component. A CM voltage component cannot drive any current in a three-phase motor with a floating neutral point \( o \) (or grid neutral point, in the case of grid connected inverter).

The characteristic waveforms of a Y-VSI employing SPWM are analysed in the following. Depending on the instantaneous motor voltage \( u_{an}(t) \) value, the output inverter voltage \( u_{an}(t) \) can be higher or lower than the input voltage \( U_i \). Accordingly, phase-module \( a \) operates in buck or boost regime as highlighted in Fig. 6(a)

\[
\begin{align*}
\text{buck regime:} & \quad m_a(\varphi) \leq 1, \quad +\varphi_o < \varphi < 2\pi - \varphi_o \\
\text{boost regime:} & \quad m_a(\varphi) > 1, \quad -\varphi_o < \varphi < +\varphi_o,
\end{align*}
\]

(7)

where \( m_a \) is the modulation factor, showing the instantaneous ratio between the inverter output voltage and the input voltage

\[
m_a(\varphi) = \frac{u_{an}(\varphi)}{U_i}.
\]

(8)

The transition angle from boost to buck regime is

\[
\varphi_o = \cos^{-1}\left( \frac{U_i - U_m}{U_m} \right) \equiv \cos^{-1}\left( \frac{2}{M} - 1 \right).
\]

(9)

During buck regime in Fig. 6(c), the half-bridge \( \bar{a}_1 \) (devices \( T_{a1} - T_{a2} \)) is operated with the switching frequency \( f_s \), while the high-side switch \( T_{a3} \) of the half-bridge \( \bar{a}_2 \) is continuously turned-on (clamped). In this case, phase-module \( a \) reduces to a simple buck converter as is highlighted in Fig. 5(a). During boost regime in Fig. 6(c), the half-bridge \( \bar{a}_2 \) (devices \( T_{a3} - T_{a4} \)) is operated with the switching frequency \( f_s \), while the high-side switch \( T_{a1} \) of the half-bridge \( \bar{a}_1 \) is continuously turned-on (clamped). In this case, phase-module \( a \) reduces to a simple boost converter as is highlighted in Fig. 5(b). Depending on the instantaneous output voltage reference \( u_{an}(t) \), the inverter transitions seamlessly between buck and boost regime.

The two half-bridges \( \bar{a}_1 \) and \( \bar{a}_2 \) are operated in a mutually exclusive fashion. That is, only one half-bridge is in switching operation, while the high-side switch of the other half-bridge is continuously turned on. In total, only three half-bridges are switched, at any given point in time. As a result, low switching losses are generated and high inverter efficiency is achieved. Note that a simple VSI employing SWPM results in continuous switching of three half-bridges, which is the same as the Y-VSI. A VSI is a single-stage inverter from a power conversion perspective. Accordingly, a Y-VSI can also be considered as a single-stage inverter topology, based on the number of switched half-bridges.

The characteristic waveforms of phase \( a \), which are illustrated in Fig. 6, are half period symmetric. Therefore, the analytic expressions of those waveforms are calculated for only half of the fundamental period, i.e. in the interval \( 0 < \varphi = \omega_m t < \pi \). The duty cycles \( d_{a1} \) and \( d_{a2} \) which control the high-side switches of the half-bridges \( \bar{a}_1 \) and \( \bar{a}_2 \), respectively, are now calculated. Each point in time \( t \) of the offsetted sinusoidal output voltage \( u_{an}(t) \), can be considered as a quasi-static operating point of the DC/DC converter phase-module. This is true because the switching frequency is much higher compared to the motor fundamental frequency \( f_s \gg f_m \). Thereby, the duty cycles \( d_{a1} \) and \( d_{a2} \) can be derived

\[
d_{a1}(\varphi) = \min\left[ 1, m_a(\varphi) \right] = \begin{cases} 1, & 0 < \varphi \leq \varphi_o \\ m_a(\varphi), & \varphi_o < \varphi \leq \pi \end{cases},
\]

(10)

\[
d_{a2}(\varphi) = \min\left[ 1, \frac{1}{m_a(\varphi)} \right] = \begin{cases} \frac{1}{m_a(\varphi)}, & 0 < \varphi \leq \varphi_o \\ 1, & \varphi_o < \varphi \leq \pi \end{cases}.
\]

(11)

The resulting duty cycles for the SPWM modulation are visualized in Fig. 6(b) and are calculated based on (6) as

\[
d_{a1}(\varphi) = \begin{cases} 1, & 0 < \varphi \leq \varphi_o \\ M(1 + \cos(\varphi))/2, & \varphi_o < \varphi \leq \pi \end{cases}.
\]

(12)
Fig. 6: Sinusoidal modulation strategy (SPWM) characteristic waveforms. (a) Inverter output voltages (offset sinusoidal shape). (b) Phase α duty cycles followed by (c) gate signals. (d) Phase α filter inductor current and motor current, (e) filter inductor current ripple and (f) motor voltages.

TABLE II: Y-VSI characteristic waveforms, for sinusoidal modulation (SPWM) and discontinuous modulation (DPWM).

<table>
<thead>
<tr>
<th>SPWM (M ≥ 1)</th>
<th>DPWM (M ≥ 4/3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>uαm(φ) = U_m</td>
<td>[ -\min{u_{ao}(\varphi), u_{am}(\varphi), u_{co}(\varphi)} ]</td>
</tr>
<tr>
<td>uαm(φ) = U_m(\cos(\varphi) + 1)</td>
<td>[ \begin{aligned} &amp;U_m(\cos(\varphi) - \cos(\varphi + \frac{2\pi}{3})), \ &amp;0 &lt; \varphi &lt; 2\pi/3 \ &amp;0 &lt; \varphi &lt; \pi \end{aligned} ]</td>
</tr>
<tr>
<td>( \varphi_0 )</td>
<td>[ \begin{aligned} &amp;\cos^{-1}\left(\frac{3}{M} - 1\right), \ &amp;0 &lt; \varphi \leq \varphi_0 \ &amp;\frac{M(1+\cos(\varphi))}{2}, \ &amp;\varphi_0 &lt; \varphi \leq \pi \end{aligned} ]</td>
</tr>
<tr>
<td>( \varphi_0 )</td>
<td>[ \begin{aligned} &amp;\cos^{-1}\left(\frac{2}{\sqrt{3}}\right) + \frac{\pi}{3}, \ &amp;0 &lt; \varphi \leq \varphi_0 \ &amp;\frac{M(\cos(\varphi) - \cos(\varphi + \frac{2\pi}{3}))}{2}, \ &amp;0, \ &amp;\frac{2}{M(\cos(\varphi) - \cos(\varphi + \frac{2\pi}{3}))}, \ &amp;\varphi_0 &lt; \varphi \leq \pi \end{aligned} ]</td>
</tr>
<tr>
<td>( d_{a1}(\varphi) )</td>
<td>[ \begin{aligned} &amp;1, \ &amp;M(1+\cos(\varphi)), \ &amp;0 &lt; \varphi \leq \varphi_0 \end{aligned} ]</td>
</tr>
<tr>
<td>( d_{a2}(\varphi) )</td>
<td>[ \begin{aligned} &amp;1, \ &amp;\frac{2}{M(1+\cos(\varphi))}, \ &amp;0 &lt; \varphi \leq \varphi_0 \end{aligned} ]</td>
</tr>
<tr>
<td>( i_{L,a}(\varphi) )</td>
<td>[ \begin{aligned} &amp;I_m \cos(\varphi) \frac{M}{2}(\cos(\varphi) + 1), \ &amp;I_m \cos(\varphi), \ &amp;0 &lt; \varphi \leq \varphi_0 \end{aligned} ]</td>
</tr>
<tr>
<td>( i_{L,a}(\varphi) )</td>
<td>[ \begin{aligned} &amp;I_m \cos(\varphi) \frac{M}{2}(\cos(\varphi) - \cos(\varphi + \frac{2\pi}{3})), \ &amp;I_m \cos(\varphi), \ &amp;0 &lt; \varphi \leq \varphi_0 \end{aligned} ]</td>
</tr>
</tbody>
</table>
Each phase-module features an integrated output filter ($L_{o} - C_{o}$) which allows for the continuous output voltages of Fig. 6(a). The filter inductor characteristics are now analysed. The modulation index range, the Y-VSI transitions between buck and boost regime (cf. Fig. 5 and 6). For a lower modulation index $M = 0...1$ the Y-VSI operates exclusively in buck regime, over the whole fundamental period, hence is equivalent to a simple VSI. The properties of the Y-VSI in the modulation range $M = 0...1$ are discussed in Appx. A.

B. Discontinuous Modulation (DPWM)

The offset voltage $u_{off}$ of (4), was selected to be constant for the sinusoidal modulation (SPWM), in (5). However, this is not necessary: The offset voltage $u_{off}$ is a degree of freedom that can be utilized in order to further improve the inverter performance. By selecting a time-varying offset voltage $u_{off}(t)$ significant performance advantages can be achieved.

In the case of a two-level VSI, this degree of freedom has been extensively detailed in literature. By employing a time-varying offset voltages and/or common-mode voltage injection [45], [46], different modulation strategies are derived: For example, in the case of third harmonic injection [47], a sinusoidal offset voltage (third harmonic) is injected, while in the case of triangular voltage insertion [48], a triangular offset voltage is used. These modulation strategies allow for an optimal utilization of the VSI DC link voltage. In the case of discontinuous modulation (DPWM) [49], it is possible to generate a three-phase voltage system for the motor by switching only two out of the three phases of the VSI. Accordingly, the switching losses of the VSI are significantly reduced. There are many variants of DPWM [50], but in all cases a discontinuous offset voltage is injected.

The DPWM modulation concept is now extended for the Y-VSI. In particular, the time-varying offset voltage is

$$u_{off}(t) = -\min[u_{an}(t), u_{bo}(t), u_{co}(t)].$$

(21)

The Y-VSI output voltages are equal to the sum of the respective motor voltages and the offset voltage, according to (4). The three-phase output voltages are illustrated in Fig. 7(a), while the output voltage of phase $a$ in particular is

$$u_{an}(\varphi) = \begin{cases} u_{an} - u_{bo}, & -\frac{2\pi}{3} < \varphi < 0 \\ u_{an} - u_{co}, & 0 < \varphi < \frac{2\pi}{3} \\ u_{an} - u_{ao}, & \frac{2\pi}{3} < \varphi < \frac{4\pi}{3} \\ \hat{U}_{m} \left[ \cos(\varphi) - \cos(\varphi - \frac{2\pi}{3}) \right], & -\frac{2\pi}{3} < \varphi < 0 \\ \hat{U}_{m} \left[ \cos(\varphi) - \cos(\varphi + \frac{2\pi}{3}) \right], & 0 < \varphi < \frac{2\pi}{3} \\ 0, & \frac{2\pi}{3} < \varphi < \frac{4\pi}{3} \end{cases}$$

(22)

According to DPWM, the phase with the most negative motor voltage is clamped to the negative DC rail $n$, for one third of the fundamental period $T_{m}/3$. Phase $a$ in particular is clamped for the interval $\frac{2\pi}{3} < \varphi < \frac{4\pi}{3}$ in Fig. 7(c). The output voltages of Fig. 7(a) have a non-sinusoidal shape, however the line-to-line motor voltages are sinusoidal. Therefore it
is possible by means of DPWM to generate a sinusoidal three-phase motor voltage system with non-sinusoidal inverter output voltages. The DPWM modulation benefits from two key advantages compared to SPWM: (i) Reduction of the total Y-VSI switching transitions by 33% [21]. During one third of the fundamental motor period $T_m/3$ (i.e. the interval $\frac{2\pi}{3} < \phi < \frac{4\pi}{3}$), the phase-module $a$ is clamped, thus no switching losses are generated from this phase-module. (ii) Reduction of the voltage stress on the boost half-bridges $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ by 13%. The phase $a$ boost half-bridge $a_2$ processes switches the output voltage $u_{an}$. The DPWM can generate the same motor phase voltage amplitude $U_{an}$ as SWPM, but with the non-sinusoidal output voltages of Fig. 7(a). The maximum value of those output voltages is $U_{an,PK} = \sqrt{3}U_m$ which is 13% lower compared to the respective value for SPWM $U_{an,PK} = 2U_m$.

The characteristic waveforms of a Y-VSI employing DPWM are analysed in the following. Depending on the instantaneous motor voltage $u_{an}(t)$ value, the output inverter voltage $u_{an}(t)$ can be higher or lower than the input voltage $U_i$. Accordingly, the phase-module $a$ operates in boost regime (cf. Fig. 5(b)) or buck regime (cf. Fig. 5(a)). The two operation regimes are highlighted on Fig. 7(a) and are analytically expressed in (7). The angle $\phi_o$, where the transition from boost to buck regime occurs, is

$$\phi_o = \cos^{-1} \left( \frac{U_i}{\sqrt{3}U_m} \right) + \frac{\pi}{6} \equiv \cos^{-1} \left( \frac{2}{\sqrt{3}M} \right) + \frac{\pi}{6}, \quad (24)$$

The duty cycles $d_{a_1}$ and $d_{a_2}$, that control the half-bridges $\bar{a}_1$ and $\bar{a}_2$, are illustrated in Fig. 7(b) and are calculated based on (10) and (11) as

$$d_{a_1}(\phi) = \begin{cases} 1, & 0 < \phi \leq \phi_o \\ \frac{M \cos(\phi) - \cos(\phi + \frac{2\pi}{3})}{2}, & \phi_o < \phi \leq \frac{2\pi}{3} \\ 0, & \frac{2\pi}{3} < \phi \leq \pi \end{cases},$$

$$d_{a_2}(\phi) = \begin{cases} 2, & 0 < \phi \leq \phi_o \\ \frac{M \cos(\phi) - \cos(\phi + \frac{2\pi}{3})}{1}, & \phi_o < \phi \leq \pi \end{cases}. \quad (25)$$

The integrated output filter is finally analysed, starting from the filter inductor $L_o$. In the case of DPWM, the inductor current is depicted in Fig. 7(d) and is calculated base on (2), (14) and (26) as

$$i_{l_{an}}(\phi) = \begin{cases} \hat{i}_m \cos(\phi) \frac{M}{2} \left( \cos(\phi) - \cos(\phi + \frac{2\pi}{3}) \right), & 0 < \phi \leq \phi_o \\ \hat{i}_m \cos(\phi), & \phi_o < \phi \leq \pi \end{cases}. \quad (27)$$

The inductor current waveform is non-sinusoidal, and is approximated by a simpler waveform

$$i_{l_{an}}(\phi) \approx \hat{i}_m \left( \frac{M \sqrt{3} + 2}{4} \cos(\phi) + \frac{M \sqrt{3} - 2}{4} \right). \quad (28)$$

The maximum inductor current is greater than the motor current amplitude $I_m$ and occurs during boost regime

$$\hat{i}_{l_{an}} = \hat{i}_m \frac{\sqrt{3}}{2} M, \quad (29)$$

while the RMS current of the filter inductor is

$$\hat{i}_{l_{an,RMS}} = \frac{\hat{i}_m}{\sqrt{2}} \frac{\sqrt{9M^2 + 4\sqrt{3} + 12}}{4}. \quad (30)$$

A current ripple is superimposed to the inductor current due to the PWM operation of the Y-VSI (cf. Fig. 7(d)). The current ripple of the inductor $\Delta i_{l_{an}}$ is isolated in Fig. 6(e), while the maximum occurring current ripple value (single-side amplitude) is

$$\Delta i_{l_{an}} = \max \left[ \frac{\pi}{2} \frac{\sqrt{3}}{M} - 1 \right], \quad \frac{U_i}{8L_o f_s}. \quad (31)$$

Finally, the output capacitor $C_o$ is analysed. A voltage ripple is superimposed to the continuous output voltages of Fig. 7(a), due to the PWM operation of the Y-VSI. The maximum occurring voltage ripple value across the filter capacitor $C_o$ (single-side amplitude) is

$$\Delta U_{o_{an}} = \Delta U_{an} = \max \left[ \frac{U_i}{64L_o C_o f_s^2}, \frac{\sqrt{3} M \hat{i}_m}{8C_o f_s} \right]. \quad (32)$$

A voltage ripple of $\Delta U_{an} < 2$ V should be achieved, in order to avoid parasitic bearing currents.

The characteristic waveforms, corresponding to DPWM modulation strategy, are summarized in Tab. II and are valid for a modulation index $M \geq 4/3$. For this modulation index range, the Y-VSI alternates between buck and boost regime (cf. Fig. 5 and 7). For a low modulation index $M = 0...2/\sqrt{3}$ the Y-VSI operates exclusively in buck regime, over the whole fundamental period, hence is equivalent to a simple VSI. The properties of the Y-VSI in the modulation range $M = 0...2/\sqrt{3}$ are discussed in Appx. A. Finally for a modulation index $M = 2/\sqrt{3}...4/3$, the Y-VSI alternates several times between buck and boost regime during the fundamental period. The analytic formulas of Tab. II can be used as an approximation in the modulation range $M = 2/\sqrt{3}...4/3$.

C. Control System

A complete control system is now conceptualized for the Y-VSI and is illustrated in Fig. 8. The goal of the control system is to maintain the desired motor speed set-point $\omega = \omega^*$. To this end, a standard cascaded speed-torque controller, referenced to the dq-axis frame, is used for the motor. The motor controller receives the speed $\omega$, the position angle $\epsilon$, and the terminal currents $[i_{m,a}, i_{m,b}, i_{m,c}]$ as input. In return, the motor controller outputs the motor terminal voltage references $[u_{m,a}^*, u_{m,b}^*, u_{m,c}^*]$. The Y-VSI ensures that the motor voltages $[u_{m,a}, u_{m,b}, u_{m,c}]$ follow the respective sinusoidal references $[u_{m,a}^*, u_{m,b}^*, u_{m,c}^*]$. Each phase-module of the Y-VSI is operated independently, hence the control block diagram is visualized for only phase $a$.
cell voltage is $U_i = 60$ V, while the motor voltage ranges within $\hat{U}_m = 0$ V...40 V (phase amplitude). The nominal motor voltage/power operation ($\hat{U}_m = 40$ V, $P = 1$ kW), that corresponds to a modulation index of $M = 4/3$, yields the highest component stresses. For the sake of simplicity, a resistive load $R = 3\frac{U_i^2}{P_{max}}/2P_{max} = 2.4\Omega$ is assumed, which corresponds to a unity power factor, $\cos(\phi) = 1$. Thereby, the transferred power $P$, fuel-cell current $I_i$ and motor fundamental phase current amplitude $I_m$ can be derived as a function of the modulation index

$$P = M^2\frac{3U_i^2}{8R}, \quad I_i = M^2\frac{3U_i}{8R}, \quad \dot{I}_m = M\frac{U_i}{2R}.$$  \hspace{1cm} (33)

In order to further simplify the analysis, the current ripple of the filter inductor $L_o$ is neglected, unless stated otherwise. Furthermore, the two half-bridges comprising each phase-module (e.g. half-bridges $\bar{a}_1$ and $\bar{a}_2$ for phase-module $a$) are assumed to be identical.

A. Sinusoidal Modulation (SPWM)

The component stresses are analytically derived for a modulation index range $M = 1...2$. For this modulation range the Y-VSI generates motor voltages amplitudes $\hat{U}_m$ greater than the input voltage $U_i$ (buck and boost regime). For a low modulation index $M = 0...1$, the Y-VSI is equivalent to a simple two-level VSI (buck regime) as shown in Fig. 5(a). The component stresses for a low modulation index case are derived in Appx. A.

1) Semiconductor Voltage Stress: The semiconductors of the buck half-bridges ($\bar{a}_1$, $\bar{b}_1$, $\bar{c}_1$) are blocking/switching the DC input voltage $U_i$ independent of the employed modulation strategy

$$U_{T1} = U_{T2} = U_i.$$  \hspace{1cm} (34)

In contrast, the boost half-bridges ($\bar{a}_2$, $\bar{b}_2$, $\bar{c}_2$) are blocking the time-varying inverter output voltages (e.g. voltage $u_{in}(\phi)$ for half-bridge $\bar{a}_2$), which depend on the employed modulation strategy. Therefore, the maximum inverter output voltage value from Fig. 6(a) defines the voltage stress on the boost half-bridge semiconductor devices

$$U_{T3} = U_{T4} = 2\hat{U}_m.$$  \hspace{1cm} (35)

2) Semiconductor Current Stress: The RMS current stress of the semiconductor devices is plotted in Fig. 9 and is analytically approximated by

$$I_{T1,\text{RMS}} = I_{L_o,\text{RMS}}\sqrt{\frac{\sqrt{3}}{\pi^2}M^2 + (1 - \frac{\sqrt{3}}{\pi^2})M + 1 - \frac{2}{\sqrt{3}}}.$$  \hspace{1cm} (36)

$$I_{T2,\text{RMS}} = I_{L_o,\text{RMS}}\sqrt{\frac{2}{\sqrt{3}^2}M^2 - (1 - \frac{\sqrt{3}}{\pi^2})M + \frac{2}{\sqrt{3}}}.$$  \hspace{1cm} (37)

$$I_{T3,\text{RMS}} = I_{L_o,\text{RMS}}\sqrt{\frac{1}{2\pi^2}M^2 - \frac{8}{15}M + \frac{3}{2}}.$$  \hspace{1cm} (38)

$$I_{T4,\text{RMS}} = I_{L_o,\text{RMS}}\sqrt{-\frac{1}{2\pi^2}M^2 + \frac{8}{15}M - \frac{1}{2}}.$$  \hspace{1cm} (39)
where the RMS current of the inductor $I_{L,RMS}$ is given by (18).

As shown in Fig. 9, the current stress on the semiconductor devices is asymmetric and depends on the modulation index $M$. In the most extreme case example, for the modulation index range $M = 0...1$, the high-side switch $T_3$ conducts the total motor current, while the low-side switch $T_4$ conducts no current. Therefore, the current rating of the semiconductor devices must be carefully selected in order to account for this asymmetric current stress.

3) Semiconductor Conduction Losses: The conduction losses of the Y-VSI semiconductor devices are

$$P_{cd} = 6I_{L,RMS}^2R_{T, on},$$

where $R_{T, on}$ is the on-state resistance of each (unipolar) power semiconductor device and $I_{L,RMS}$ is the RMS current of the filter inductor $L_o$. It is reminded that, the current ripple is neglected, for the inductor RMS current calculation. Therefore, the conduction losses are calculated for SPWM based on (18) and (40)

$$P_{cd} = 6I_{L,RMS}^2\frac{M^2 - 2M + 3}{4}R_{T, on}.$$  

4) Semiconductor Switching Losses: In a half-bridge, the switching energy dissipation $E_{sw}$, associated with a hard switching transition, is approximated as a linear function of the commutation current $I_{sw}$ as

$$E_{sw}(I_{sw}) = k_0 + k_1I_{sw}.$$  

Accordingly, the switching power dissipation for a switching frequency $f_s$ is

$$P_{sw}(I_{sw}) = f_sE_{sw} = f_s(k_0 + k_1I_{sw}).$$  

The parameters $k_0$ and $k_1$ depend on the commutation (switched) voltage $U_{sw}$. Namely, the parameter $k_0$ represents the constant part of the switching losses and is calculated in literature [51] (assuming unipolar power semiconductors) as

$$k_0(U_{sw}) = Q_{oss}(U_{sw}) \cdot U_{sw},$$

where $Q_{oss}$ is the electric charge stored in the non-linear output parasitic capacitance $C_{oss}$ of the MOSFET

$$P_{sw,1} = \frac{3f_s}{\pi} \int_{\phi_0}^\pi [k_0 + k_1I_{L}(\phi)]d\phi.$$  

Besides the commutation voltage $U_{sw}$, the parameter $k_1$ depends on the semiconductor technology and the gate driver configuration [52], [53].

The switching losses of the Y-VSI are now derived, starting from the buck half-bridges. The buck half-bridge $a_1$ is switched only during the buck regime of Fig. 6, i.e. when $u_{an}(\phi) \leq U_i$. The commutation voltage of the buck half-bridge $a_1$ is constant and equal to the input voltage $U_{sw,1} = U_i$. The commutation current is equal to the inductor current and hence varies over time $i_{sw,1}(\phi) = i_{L,a}(\phi)$. An integration of the local (instantaneous) switching losses of (43) must be performed over the fundamental period $T_m$ in order to derive the total switching losses caused by the buck half-bridges

$$P_{sw,1} = \frac{3f_s}{\pi} \left[ k_0 - \frac{\phi_0}{\pi} \right] + k_1 \frac{2}{\pi} \int_{0}^{\phi_0} (1 - \frac{1}{2} \sin(\phi)) \right],$$

where the sin of the transition angle $\phi_0$ is

$$\sin(\phi_0) = \frac{2}{M} \sqrt{M - 1}.$$  

Furthermore, the switching parameters $k_0$ and $k_1$ of (47) are calculated for the constant commutation voltage of the buck half-bridges $U_{sw,1} = U_i$.

The boost half-bridge $a_2$ is switched only during the boost regime of Fig. 6, i.e. when $u_{an}(\phi) > U_i$. The commutation voltage of the boost half-bridge $a_2$ is equal to the inverter output voltage and hence varies over time $u_{sw,2}(\phi) = u_{an}(\phi)$. The commutation current is equal to the inductor current $i_{sw,2}(\phi) = i_{L,a}(\phi)$ and is also time-varying. An integration of the local switching losses of (43) must be performed over the fundamental period $T_m$ in order to derive the total switching losses caused by the boost half-bridges

$$P_{sw,2} = \frac{3f_s}{\pi} \int_{\phi_0}^\pi [k_0(\phi) + k_1(\phi)i_{L,a}(\phi)]d\phi,$$

where the switching parameters $k_0(\phi)$ and $k_1(\phi)$ are varying over time and depend on the instantaneous commutation voltage $u_{sw,2}(\phi)$. The resulting sum of switching losses for
the three boost half-bridges, when SPWM modulation is used, is approximated by

$$P_{sw,2} = 3f_s (k_0 + k_1 M \hat{I}_m) \frac{\sin(\hat{\phi}o)}{\pi},$$  \hspace{1cm} (50)$$

where \(\sin(\hat{\phi}o)\) is given in (48). The switching parameters \(k_0\) and \(k_1\) of (50) are calculated for the highest commutation voltage of the boost half-bridges \(U_{sw,2} = u_m(0) = 2U_m\). The total switching losses of the Y-VSI are the sum of the local (instantaneous) RMS current ripple of the inductor

$$P_{sw} = P_{sw,1} + P_{sw,2}.$$  \hspace{1cm} (51)$$

5) Passive Components Selection: The integrated output filter \((L_o - C_o)\) of the Y-VSI is now analysed in detail, starting from the filter inductors \(L_o\). The current of the filter inductor is non-sinusoidal, as is described by (15) and shown in Fig. 6(d). The maximum current stress on the inductor depends on the modulation index \(M\), as given in (16) and plotted in Fig. 11(a). The peak current ripple of the filter inductor is given by (19). Accordingly, in order to limit this current ripple to a maximum value of \(\Delta I_{L_o}\), the inductance value must be selected as

$$L_o \geq \max \left[ 1, \frac{4M - 1}{M} \right] \cdot \frac{U_i}{8\Delta I_{L_o}f_s},$$  \hspace{1cm} (52)$$

where \(M = M_{max}\) is the highest possible modulation index within the inverter operating range. In general, there is a direct relation between the inductor losses and the RMS inductor current ripple \(\Delta I_{L_o,RMS}\), as a high RMS current ripple results in high frequency RMS flux density and hence substantial core losses [54]. In addition, a high RMS current ripple causes high-frequency winding losses due to skin and proximity effect. Therefore, the RMS inductor current ripple \(\Delta I_{L_o,RMS}\) is a reasonable performance indicator for the design of the inductive components and is calculated in the following. The local (instantaneous) RMS current ripple of the filter inductor

$$\Delta I_{L_o,RMS}(\phi) = \left\{ \begin{array}{ll}
4m_a (1 - m_a) & \frac{U_i}{8\sqrt{3}L_o f_s}, \quad 0 < \phi \leq \hat{\phi}o \\
4m_a - 1 & \frac{U_i}{8\sqrt{3}L_o f_s}, \quad \hat{\phi}o < \phi \leq \pi 
\end{array} \right.$$  \hspace{1cm} (53)$$

where \(m_a(\phi)\) is the modulation factor and is given in (8). The relation between the local RMS current ripple of the inductor \(\Delta I_{L_o,RMS}\) and the modulation factor \(m_a\) is visualized in Fig. 10. In order to calculate the global (total) RMS current ripple, an integration of the local RMS current ripple (53) over the fundamental period \(T_m\) is performed. The global RMS current ripple is calculated numerically and is plotted in Fig. 11(b). Finally, the filter capacitors \(C_o\) are selected. The peak voltage ripple across the filter capacitor is given in (20). Accordingly, in order to limit this voltage ripple to a maximum value of \(\Delta U_{C_o}\), the capacitance value must be selected as

$$C_o \geq \max \left[ \frac{U_i}{64L_o \Delta U_{C_o} f_s^2}, \frac{M \hat{I}_m}{8\Delta U_{C_o} f_s} \right].$$  \hspace{1cm} (54)$$

A voltage ripple of \(\Delta U_{C_o} < \Delta u_m < 2V\) should be selected, for a safe motor operation. Finally, an RC damping circuit is placed in parallel to the filter capacitor \(C_o\), in order to avoid unwanted resonances of the output filter [38].

B. Discontinuous Modulation (DPWM)

The component stresses are analytically derived for a modulation index range \(M = 4/3...2\). For this modulation range the Y-VSI generates motor voltage amplitudes \(U_m\) greater than the input voltage \(U_i\) (buck and boost regime). For a low

50
100
150
200
0
0.0 0.5 1.0 1.5 2.0
Modulation Factor \(M\)

50
100
150
200
0
Local (instantaneous) RMS current of the filter inductor \(L_o\), normalized with respect to \(\frac{U_i}{8\sqrt{3}L_o f_s}\). The local RMS current ripple depends on the modulation factor \(m_a(\phi) = u_m(\phi)/U_i\) of (8).

Fig. 10: Local (instantaneous) RMS current of the filter inductor \(L_o\), normalized with respect to \(\frac{U_i}{8\sqrt{3}L_o f_s}\). The local RMS current ripple depends on the modulation factor \(m_a(\phi) = u_m(\phi)/U_i\) of (8).

Fig. 11: Filter inductor \(L_o\) current stress, calculated for SPWM and DPWM modulation strategies. (a) Maximum inductor current, normalized with respect to the motor current amplitude \(I_m\) and (b) inductor RMS current ripple, normalized with respect to the value \(\frac{U_i}{8\sqrt{3}L_o f_s}\).
modulation index $M = 0 \ldots 2/\sqrt{3}$, the Y-VSI is equivalent to a simple two-level VSI (buck regime) as shown in Fig. 5(a). The component stresses for a low modulation index case are derived in Appx. A.

1) Semiconductor Voltage Stress: The semiconductors of the buck half-bridges $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ are blocking/switching the DC input voltage $U_i$ independent of the employed modulation strategy

$$U_{T1} = U_{T2} = U_i.$$  (55)

In contrast, the boost half-bridges $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ are blocking the time-varying inverter output voltages (e.g. $U_{\text{m}}(\phi)$ for half-bridge $\bar{a}_2$), which depend on the employed modulation strategy. Therefore the maximum inverter output voltage value from Fig. 7(a) defines the voltage stress on the boost half-bridge semiconductor devices

$$U_{T3} = U_{T4} = \sqrt{3}U_{\text{m}}.$$  (56)

2) Semiconductor Current Stress: The RMS current stress on the semiconductor devices is plotted in Fig. 9 and is analytically approximated by

$$I_{T1,\text{RMS}} = \frac{I_{L,\text{RMS}}}{\sqrt{\frac{\sqrt{3}}{4\pi} M^2 + \frac{5}{7} M - \frac{1}{6}},}$$  (57)

$$I_{T2,\text{RMS}} = \frac{I_{L,\text{RMS}}}{\sqrt{\frac{\sqrt{3}}{4\pi} M^2 - \frac{5}{7} M + \frac{7}{6}},}$$  (58)

$$I_{T3,\text{RMS}} = \frac{I_{L,\text{RMS}}}{\sqrt{\frac{1}{4\pi} M^2 - \frac{\sqrt{3}}{\sqrt{8} M + 1 + \frac{2}{\pi},}}}$$  (59)

$$I_{T4,\text{RMS}} = \frac{I_{L,\text{RMS}}}{\sqrt{1 \frac{1}{4\pi} M^2 + \frac{\sqrt{3}}{\sqrt{8} M - \frac{2}{\pi},}}}$$  (60)

where the RMS current of the inductor $I_{L,\text{RMS}}$ is given by (30). As shown in Fig. 9, the current stress on the semiconductor devices is asymmetric and depends on the modulation index $M$. In the most extreme case example, for the modulation index range $M = 0 \ldots 2/\sqrt{3}$, the high-side switch $T_{a3}$ conducts the total motor current, while the low-side switch $T_{a4}$ conducts no current. Therefore, the current rating of the semiconductor devices must be carefully selected in order to account for this asymmetric current stress.

3) Semiconductor Conduction Losses: The conduction losses of the Y-VSI semiconductor devices are described by (40) and are proportional to the square of the inductor RMS current $I_{L,\text{RMS}}$. By using the expression (30) for the RMS inductor current, the conduction losses are calculated for DPWM

$$P_{cd} = \frac{\hat{P}_{\text{m}}^2}{2} \frac{9M^2 - 4\sqrt{3}M + 12}{16} R_{T\text{on}}.$$  (61)

4) Semiconductor Switching Losses: First, the switching losses of the buck half-bridges are calculated. The buck half-bridge $\bar{a}_1$ is switched during the buck regime of Fig. 7, i.e. when $u_{\text{m}}(\phi) \leq U_i$. Thanks to DPWM, the switching transition of the buck half-bridge $\bar{a}_1$ during the buck regime are reduced compared to SWPM. More precisely, no switching transition occur during the denoted clamping region of Fig. 7. The commutation voltage of the buck half-bridge $\bar{a}_1$ is constant and equal to the input voltage $U_{sw,1} = U_i$. The commutation current is equal to the inductor current and hence varies over time $i_{sw,1}(\phi) = i_{\text{m},a}(\phi)$. An integration of the local switching losses according to (46) is performed in order to derive the total switching losses caused by the buck half-bridges. The resulting sum of switching losses for the three buck half-bridges, when DPWM modulation is used, is

$$P_{sw,1} = 3f_s \left( k_0 \frac{2\pi}{\sqrt{3}} - \phi_o + k_1 \frac{2\pi}{\sqrt{3}} f_m \left( \frac{4 - \sqrt{3}}{4} - \frac{1}{2} \sin(\phi_o) \right) \right),$$  (62)

where the sinus of the transition angle $\phi_o$ is

$$\sin(\phi_o) = \frac{3\sqrt{3}M^2 - 4 + 2\sqrt{3}}{6M}.$$  (63)

The switching parameters $k_0$ and $k_1$ of (62) are calculated for the constant commutation voltage of the buck half-bridges $U_{sw,1} = U_i$.

Subsequently, the switching losses of the boost half-bridges are calculated. The boost half-bridge $\bar{a}_2$ is switched only during the boost regime of Fig. 7, i.e. when $u_{\text{m}}(\phi) > U_i$. The commutation voltage of the boost half-bridge $\bar{a}_2$ is equal to the inverter output voltage and hence varies over time $u_{sw,2}(\phi) = u_{\text{m}}(\phi)$. The commutation current is equal to the inductor current $i_{sw,2}(\phi) = i_{\text{m},a}(\phi)$ and is also time-varying. An integration of the local switching losses according to (49) is performed in order to derive the total switching losses caused by the boost half-bridges. The resulting sum of switching losses for the three boost half-bridges, when DPWM modulation is used, is approximated by

$$P_{sw,2} = 3f_s \left( k_0 + k_1 \frac{1}{2} \frac{\sqrt{3}}{f_m} \sin(\phi_o) \right) \frac{\pi}{\pi},$$  (64)

where $\sin(\phi_o)$ is given in (63). The switching parameters $k_0$ and $k_1$ of (64) are calculated for the highest commutation voltage of the boost half-bridges $U_{sw,2} = u_{\text{m}}(\frac{\pi}{2}) = \sqrt{3}U_{\text{m}}$. The total switching losses of the Y-VSI are the sum of the respective buck half-bridges’ and boost half-bridges’ switching losses (51). According to DPWM, the phase with the most negative motor voltage is clamped to the negative DC rail $n$, for one third of the fundamental period $T_m/3$ (cf. Fig. 7). Thereby, it is possible to reduce the total switching transitions of the Y-VSI by 33% compared to SPWM. Accordingly, a significant reduction of the switching losses is achieved thanks to DPWM.

5) Passive Component Selection: The integrated output filter $(L_o - C_o)$ of the Y-VSI is now analysed. It is assumed that a Y-VSI inverter, designed for SPWM modulation, pre-exists. In this case, the filter inductors $L_o$ and the filter capacitors $C_o$ are selected based on (52) and (54), respectively. The current of the filter inductor is non-sinusoidal, as is described by (27) and shown in Fig. 7(d). The maximum current of the inductor depends on the modulation index $M$, is given in (29) and is plotted in Fig. 11(a). The DPWM results in a lower maximum
TABLE III: Component stresses summary for a Y-VSI employing SPWM or DPWM modulation strategy. The numeric values are calculated for the motor drive of Tab. I, and for the nominal operating condition, i.e. modulation index $M = 4/3$.

<table>
<thead>
<tr>
<th>SPWM</th>
<th>DPWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_1, T_2$ Voltage PK</td>
<td>$U_{T1} = U_{T2} = 40$ V</td>
</tr>
<tr>
<td>$T_3, T_4$ Voltage PK</td>
<td>$U_{T3} = U_{T4} = 80$ V</td>
</tr>
<tr>
<td>$I_{T1 RMS}$</td>
<td>$12.2$ A</td>
</tr>
<tr>
<td>$I_{T2 RMS}$</td>
<td>$8.5$ A</td>
</tr>
<tr>
<td>$I_{T3 RMS}$</td>
<td>$13.2$ A</td>
</tr>
<tr>
<td>$I_{T4 RMS}$</td>
<td>$4.9$ A</td>
</tr>
<tr>
<td>Conduction Losses Total</td>
<td>$P_{cl} = 11.8$ W</td>
</tr>
<tr>
<td>Switching Losses Buck</td>
<td>$P_{sw1} = 7.7$ W</td>
</tr>
<tr>
<td>$I_{0} = 6.77 \mu A$, $I_{1} = 0.68 \mu A$, for $U_{T1}$</td>
<td></td>
</tr>
<tr>
<td>Switching Losses Boost</td>
<td>$P_{sw2} = 8.7$ W</td>
</tr>
<tr>
<td>$I_{0} = 10.91 \mu A$, $I_{1} = 1.09 \mu A$, for $U_{T3}$</td>
<td></td>
</tr>
<tr>
<td>Losses Total</td>
<td>$P_{cl} + P_{sw1} + P_{sw2} = 28.3$ W</td>
</tr>
<tr>
<td>Efficiency Reduction</td>
<td>$\Delta \eta = -2.8%$</td>
</tr>
</tbody>
</table>

| **Filter Inductor** | $L_{f} = 5 \mu H$ |
| **Current Ripple PK** | $\Delta I_{m} = 3.6$ A |
| **Current PK** | $I_{m} = 22.2$ A |
| **Current RMS** | $I_{m RMS} = 13.3$ A |
| **Filter Capacitor** | $C_{f} = 2 \mu F$ |
| **Votlage Ripple PK** | $\Delta U_{C} = 0.7$ V |

* Switching parameters $k_0$ and $k_1$ are calculated based on [53].

The resulting input capacitance value $C_1$ is inversely proportional to the switching frequency $f_s$, and is typically small. It is noted here, that there is no need for low-frequency energy storage within the input capacitor $C_1$, for a balanced three-phase system. In summary, the input capacitor must conduct a high-frequency switched current with a high RMS value $I_{C_1 RMS}$, while a low capacitance $C_1$ is typically required. Therefore, ceramic or film capacitors are suggested for the $C_1$ realization.

IV. EXPERIMENTAL VALIDATION

The proposed Y-VSI inverter concept is tested within the fuel-cell application of Fig. 1 and Tab. I. A $10$ kW fuel-cell unit requires a continuous supply of oxygen, which is provided by a $280$ krpmp high-speed electric compressor [5]. A motor drive system, directly supplied by the fuel-cell controls the electric compressor. The compressor drive system uses $10\%$ of the fuel-cell power, i.e. $1$ kW.

A. Design Procedure

The previously derived component stresses in Sec. III depend on the switching frequency $f_s$, however the switching frequency is until now not explicitly defined. The switching frequency $f_s$ represents a crucial design trade-off. A high switching frequency allows to reduce the volume of the passive filter components, but at the same time increases the semiconductor switching losses and accordingly requires a larger semiconductor heatsink volume. In order to select an appropriate switching frequency, a multi-objective optimization routine, with respect to inverter efficiency $\eta$ and power density $\rho$, is employed [55]–[57], which assesses the performance of several Y-VSI inverter designs. The optimization routine includes the $200$ V rated GaN semiconductor devices (EPC 2034 MOSFETs [53]), the semiconductor heatsinks [58], the inductive components $L_o$, [54], [59] and the ceramic capacitors $C_o, C_1$.

Based on the optimization results, a switching frequency of $f_s = 300$ kHz is selected for the Y-VSI. The boxed volume of the integrated AC filter ($L_o$ and $C_1$) is $36.4$ cm$^3$. Subsequently, the number of parallel semiconductor devices per switch ($T_{al}$ - $T_{ad}$ of Fig. 3) is selected. A low number of parallel devices yields low (capacitive) switching losses, but high
conduction losses. On the contrary, a high number of parallel devices results in high switching losses but low conduction losses. The number of parallel devices is determined by the minimum of the overall semiconductor losses (i.e., sum of conduction and switching losses). In the case at hand, two parallel devices per switch are optimal. A breakdown of the semiconductor losses into conduction and switching losses is depicted in Fig. 12. As expected, DPWM modulation yields lower semiconductor losses (-33.2%) compared to SPWM modulation, mainly thanks to the reduced number of switching transitions. The Y-VSI component parameters are given in Tab. IV.

Using the analytic formulas derived in Sec. III, the inverter component stresses are calculated and summarized in Tab. III. There, the SPWM and DPWM modulation strategies are compared. The Tab. III serves as a general design guideline and can be extended for motor drive systems with different specifications. After the designer selects an appropriate switching frequency $f_s$, based on the available semiconductor technology, Tab. III can be easily used in order to design a Y-VSI inverter.

For the sake of completeness, a conventional B-VSI (cf. Fig. 2) is designed for the specifications of Tab. I. The detailed design process of a B-VSI can be found in [21]. The selected B-VSI benchmark design, features the same switching frequency $f_s = 300$ kHz, for both the DC/DC stage as well as the DC/AC stage, respectively. The total volume of the DC/DC stage, as shown in Fig. 13, is 32 cm$^3$, while the total volume of the DC/AC stage, as depicted in Fig. 14, is 42 cm$^3$. The superior performance of the Y-VSI generates 35.3% less semiconductor losses reduction compared to the B-VSI [21]. Therefore, a Y-VSI requires the switching of only three half-bridges in total, at any given point in time. Furthermore, the buck half-bridge $\bar{a}_1$ of the Y-VSI switches the low input voltage $U_i = 60$ V, while the boost half-bridge $\bar{a}_2$ switches the time-varying output voltage $u_{in}(t) \leq 80$ V (6). Note that both these voltages are lower than the high DC link voltage $U_{DC} = 80$ V of a B-VSI. For the above reasons the Y-VSI benefits from low semiconductor losses. It is noted, that the semiconductor losses reduction achieved by means of the Y-VSI, simultaneously enables a low semiconductor heat sink volume [58].

A similar analysis is performed for DPWM modulation in Fig. 12(b). There, the Y-VSI generates 35.3% less semiconductor losses than the B-VSI, which can be explained as follows. According to DPWM, only two half-bridges of the Y-VSI are switched at any given point in time (cf. Fig. 7). Contrary, three half-bridges in total (one half-bridge at the DC/DC stage and two half-bridges at the DC/AC stage) are switched, in the case of the B-VSI. Therefore, the B-VSI generates considerably higher semiconductor losses than the Y-VSI.

B. Experimental Results

Two inverter hardware prototypes are purposely assembled: (i) Y-VSI of Fig. 3. The hardware prototype is shown in Fig. 13 and the respective component parameters are given in Tab. IV. Experimentally measured waveforms for SWPM are shown in Fig. 14(a), where the three output voltages of the inverter are offset sinusoids. Experimentally measured waveforms for DWPM are shown in Fig. 14(b). There, the three output voltages of the inverter are non-sinusoidal, however, the load line-to-line voltages are sinusoidal.
Fig. 13: Y-VSI hardware prototype (113 mm × 49 mm × 30 mm) achieving a power density of 6.6 kW/dm³ (108 W/in³).

TABLE IV: Parameter values of the Y-VSI hardware prototype, corresponding to the schematic diagram notation of Fig. 3.

<table>
<thead>
<tr>
<th>Y-VSI</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching frequency</td>
<td>f_s</td>
</tr>
<tr>
<td>L_i</td>
<td>10 mH</td>
</tr>
<tr>
<td>C_i</td>
<td>2 μF</td>
</tr>
<tr>
<td>C_o</td>
<td>10 μF</td>
</tr>
</tbody>
</table>

Fig. 14: Experimentally measured waveforms for the Y-VSI inverter employing (a) SPWM and (b) DPWM modulation, at nominal operating condition P = 1 kW. (yellow) Phase a, (red) phase b and (blue) phase c output voltages. (green) Phase a output voltage ripple.

Fig. 15: B-VSI hardware prototype (106 mm × 50 mm × 35 mm) achieving a power density of 6 kW/dm³ (98 W/in³).

TABLE V: Parameter values of the B-VSI hardware prototype, corresponding to the schematic diagram notation of Fig. 2.

<table>
<thead>
<tr>
<th>B-VSI - DC/DC stage</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching frequency</td>
<td>f_s,i</td>
</tr>
<tr>
<td>L_i</td>
<td>10 mH</td>
</tr>
<tr>
<td>C_i</td>
<td>2 μF</td>
</tr>
<tr>
<td>C_o DC</td>
<td>10 μF</td>
</tr>
</tbody>
</table>

Fig. 16: Experimentally measured waveforms for the B-VSI inverter at nominal operating condition P = 1 kW. (yellow) Phase a, (red) phase b and (blue) phase c output voltages. (green) Phase a output voltage ripple.

(ii) B-VSI of Fig. 2. The hardware prototype is depicted in Fig. 15, while the component parameters are summarized in Tab. V. Experimentally measured waveforms are shown in Fig. 16 for SWPM modulation. This hardware prototype serves as the state-of-the-art solution against which the Y-VSI hardware prototype is compared to.

In order to enable a meaningful comparison, both the above
hardware demonstrators feature the same switching frequency of \( f_s = 300 \text{ kHz} \). It is noted, that during the experimental measurements the compressor is replaced by an equivalent resistive load \( R = 2 \Omega \). The resistive load significantly simplifies the test setup, but does not affect the operation or the performance of the inverter prototypes.

First, the performance of the two hardware prototypes is experimentally compared. The conventional B-VSI hardware prototype achieves a power density of \( \rho = 6 \text{ kW/dm}^3 \) (including case, cooling system and control electronics). The Y-VSI hardware prototype achieves a power density of \( \rho = 6.6 \text{ kW/dm}^3 \), which is \( \Delta \rho = +10\% \) higher compared to the B-VSI. The Y-VSI benefits from a lower number of inductive components (three) compared the B-VSI (four). This is the main reason behind the higher Y-VSI power density.

At \( P = 1 \text{ kW} \) nominal operation, the B-VSI achieves a low efficiency of \( \eta = 96\% \) (i.e. 40 W of losses), for sinusoidal modulation strategy (SPWM). The majority of the losses originate from the semiconductor devices (i.e. 35.4 W calculated in Fig. 12(a)). As discussed in Sec. IV-A, there are two main reasons behind the B-VSI low efficiency. The B-VSI is a two-stage converter, as a result four half-bridges are switched at any given point in time (for SPWM). Furthermore, all the semiconductor devices process the high DC link voltage \( U_{\text{DC}} = 80 \text{ V} \).

By employing the SPWM of Fig. 6, the Y-VSI achieves a nominal efficiency of \( \eta = 97.2\% \) (i.e. 28 W of losses), which is \( \Delta \eta = +1.2\% \) more efficient compared to the B-VSI (also employing SPWM). The Y-VSI delivers power to the motors more efficiently (for SPWM). The B-VSI employs the same AC filter component values, i.e. \( L_o = 5 \mu\text{H}, C_o = 2 \mu\text{F} \). By comparing the voltage ripple generated by SPWM and DPWM modulation (cf. Fig. 14), it is evident that the latter DPWM results in an overall lower voltage ripple \( \Delta u_{\text{an}} \). This is expected, since DPWM reduces the total number of switching transitions, which cause the voltage ripple in the first place.

V. CONCLUSIONS

Motor drive systems supplied by a fuel-cell/battery are especially demanding when it comes to the design of the inverter. Besides a high performance (high efficiency \( \eta \) and power density \( \rho \)), the inverter has to cope with the wide DC voltage variation of the fuel-cell/battery. Therefore, buck-boost inverter topologies are required, which can guarantee the nominal speed/voltage range of the motor independent of the DC input voltage fluctuation.

A promising buck-boost inverter topology, denoted as Y-VSI, is presented within this paper (cf. Fig. 3). The Y-VSI is based on a three-phase modular concept, where three identical phase-modules are connected to a common star “Y” point (cf. Fig. 4). The Y-VSI benefits from four key advantages:

(i) Buck-boost capability. Each phase-module comprises a buck-boost DC/DC converter, hence the Y-VSI can generate output AC voltages that are higher or lower than the input DC voltage.

(ii) High efficiency. The Y-VSI processes the transmitted power \( P \) in a unique way. In the typical case, only three out of the six half-bridges are switched, at any given point in time. As a result, low switching losses are generated, hence high inverter efficiency is achieved. Based on the low number of switched half-bridges, the Y-VSI can be considered as a single-stage inverter.
(iii) Integrated AC output filter. The Y-VSI comprises an integrated output filter, hence generates sinusoidal motor voltages/currents. Furthermore, the Y-VSI protects the motor from high $du/dt$, thus the long-term reliability of the motor is guaranteed. As a result, no additional filter is required between the inverter and the motor.

(iv) Straightforward control. Each phase-module is equivalent to a DC/DC converter, hence can be controlled independently, based on well established control concepts. As a result, the Y-VSI benefits from a simple and uncomplicated control system (cf. Fig. 8).

Two modulation strategies are comparatively evaluated for the Y-VSI:

(i) Sinusoidal modulation (SPWM) of Fig. 6, which features sinusoidal output voltages.

(ii) Discontinuous modulation (DPWM) of Fig. 7. There, each output voltages is non-sinusoidal, however the difference between two output voltages, which is equal to the motor line-to-line voltage, is sinusoidal. By means of DPWM, it is possible to reduce the switching transition of the Y-VSI by 33%, and hence significantly reduce the overall switching losses.

The stresses on the inverter components are analytically derived for both modulation strategies, and a summary is given in Tab. III. A comparison of the two modulation strategies reveals that the latter DPWM yields higher efficiency than the former SPWM.

The Y-VSI performance is validated within the context of the application of Fig. 1 and Tab. I. In the application at hand, a motor drive system is supplied by a fuel-cell and controls a high-speed 280 krpm 1 kW electric compressor. The Y-VSI hardware prototype of Fig. 13, which achieves a power density of $\rho = 6.6 \text{ kW/dm}^3$ and an efficiency of $\eta = 98.3\%$, is purposely assembled. The hardware prototype employs the latest generation of GaN semiconductor devices and features a switching frequency of $f_s = 300 \text{ kHz}$. Finally, the Y-VSI is compared to the state-of-the-art inverter topology of Fig. 2, which features two energy conversion stages. The Y-VSI outperforms the state-of-the-art hardware prototype of Fig. 15, by $\Delta \eta = +2.3\%$ in terms of efficiency and by $\Delta \rho = +10\%$ in terms of power density.

In summary, the Y-VSI is a promising technology for modern variable speed motor drives. The integrated output filter of the Y-VSI allows for the safe use of WBG semiconductor devices. The high $du/dt$ of WBG devices is effectively suppressed by the integrated filter, hence the motor reliability is ensured. Therefore, the Y-VSI fits well with applications, where high performance, sinusoidal motor voltages/currents and wide voltage operating range are of high importance.

**APPENDIX A**

**COMPONENT STRESSES FOR LOW MODULATION INDEXES**

**A. Sinusoidal Modulation (SPWM)**

For the sake of completeness, the component stresses of the Y-VSI are derived for a low modulation index $M = 0 \ldots 1$. For SPWM within this modulation index range, the Y-VSI continuously operates in buck regime, according to Fig. 5(a). There, the boost half-bridges e.g. $\bar{a}_2$ are clamped, while only the buck half-bridges e.g. $\bar{a}_1$ are switched. In this case, the Y-VSI is equivalent to a simple two-level VSI. The RMS current stress on the semiconductor devices is

$$I_{T1,RMS} = \frac{I_m}{\sqrt{2}} \sqrt{\frac{M}{2}} \quad I_{T2,RMS} = \frac{I_m}{\sqrt{2}} \sqrt{1 - \frac{M}{2}}, \quad (67)$$

$$I_{T3,RMS} = \frac{I_m}{\sqrt{2}} \quad I_{T4,RMS} = 0,$$

and is plotted in Fig. 9.

The conduction losses of the Y-VSI semiconductor devices are described by (40) and are proportional to the square of the inductor RMS current $I_{L,RMS}$. For the examined modulation range $M = 0 \ldots 1$, the filter inductor current is equal to the motor current and hence

$$I_{L,RMS} = \frac{I_m}{\sqrt{2}} \quad (68)$$

The resulting conduction losses are

$$P_{cd} = \frac{I_m^2}{2} R_{Con} \quad (69)$$

The switching losses are subsequently analysed. The boost half-ridges are clamped and therefore exhibit no switching losses, i.e. $P_{sw,2} = 0$. Therefore, only the buck half-bridges contribute to the switching losses. The equation (46) is used in order to derive the total switching losses caused by the buck half-bridges

$$P_{sw} = P_{sw,1} = 3 f_s (k_0 + k_1 - \frac{2}{\pi}) I_m, \quad (70)$$

where the switching parameters $k_0$ and $k_1$ are calculated for the constant commutation voltage of $U_{sw,1} = U_i$.

**B. Discontinuous Modulation (DPWM)**

The component stresses of the Y-VSI are derived for DPWM and a low modulation index $M = 0 \ldots 2/\sqrt{3}$. For DPWM within this modulation index range, the Y-VSI continuously operates in buck regime, according to Fig. 5(a). The RMS current stress on the semiconductor devices is

$$I_{T1,RMS} = \frac{I_m}{\sqrt{2}} \sqrt{\frac{3 \sqrt{3} M}{4 \pi}} \quad I_{T2,RMS} = \frac{I_m}{\sqrt{2}} \sqrt{1 - \frac{3 \sqrt{3} M}{4 \pi}}, \quad (71)$$

$$I_{T3,RMS} = \frac{I_m}{\sqrt{2}} \quad I_{T4,RMS} = 0$$

The conduction losses of DPWM are the same as in the case of SWPM (69). The switching losses are subsequently analysed. Similarly to SPWM, the boost half-ridges are clamped and therefore exhibit no switching losses, i.e. $P_{sw,2} = 0$. Only the buck half-bridges contribute to the switching losses. The equation (46) is used in order to derive the total switching
losses caused by the buck half-bridges
\[ P_{sw} = P_{sw,1} = 3f_{s}\left(\frac{3}{2}k_0 + \left(1 - \frac{\sqrt{3}}{4}k_1\frac{1}{\pi}f_m\right)\right), \tag{72} \]
where the switching parameters \( k_0 \) and \( k_1 \) are calculated for the constant commutation voltage of \( U_{sw,1} = U_i \).

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