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Three-Phase Sinusoidal Output Buck-Boost GaN Y-Inverter for Advanced Variable Speed AC Drives

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***Abstract*—Motor drive systems supplied by a fuel-cell/battery are especially demanding when it comes to the design of the inverter. Besides a high performance (high efficiency η and power density ρ), the inverter has to cope with the wide DC voltage variation of the fuel-cell/battery that supplies the motor drive. A promising three-phase inverter topology, denoted as Y-VSI, is presented in this paper. The Y-VSI is a modular three-phase inverter, and comprises three identical phase-modules connected to a common star "Y" point. Each phase-module is equivalent to a buck-boost DC/DC converter, which allows the AC output voltages to be higher or lower than the DC input voltage. Thereby, the Y-VSI effectively copes with the wide variation of the fuel-cell/battery voltage. Each phase-module can be operated in a similar fashion to a conventional DC/DC converter, independently of the remaining two phases. Accordingly, a straightforward and simple operation/control of the Y-VSI is possible. In addition, the Y-VSI features an integrated output filter. This allows for continuous/sinusoidal motor voltage waveforms, eliminating the need of an additional filter between the inverter and the motor. This paper details the operating principle of the Y-VSI, and comparatively evaluates two modulation strategies. In order to validate the proposed concepts, a Y-VSI hardware prototype is assembled within the context of a high-speed motor drive. In the investigated drive system, a fuel-cell supplies the Y-VSI, which in return controls a 280 krpm 1 kW electric compressor. The Y-VSI hardware prototype is compared against a state-of-the-art hardware prototype, which features two energy conversion stages. It is shown that the Y-VSI is $\Delta\eta = +2.3\%$ more efficient and at the same time $\Delta\rho = +10\%$ more power dense compared to the conventional inverter solution.**

***Index Terms*—Drive system, High-speed, Inverter, Fuel-cell, Battery, Control system**

I. Introduction

The electrification of vehicles has created new application opportunities for the power electronics industry [1]–[3]. One such application example is shown in **Fig. 1(a)**. There, a $10\,\mathrm{kW}$ fuel-cell is depicted, which is part of a fuel-cell vehicle powertrain. An auxiliary drive system controls a high-speed $1\,\mathrm{kW}$ electric compressor, which in return provides the required oxygen for the fuel-cell unit operation [4]. This compressor drive system is directly supplied by the fuel-cell DC voltage $U_\mathrm{i} = 60\,\mathrm{V}...120\,\mathrm{V}$ and uses 10% of the fuel-cell power. The employed high-speed $280\,\mathrm{krpm}$ electric compressor [5] has a nominal phase voltage amplitude of $\hat{U}_\mathrm{o} = 40\,\mathrm{V}$. The system specifications are summarized in **Tab. I**.

In general, motor drives placed on board of vehicles, demand efficient inverter systems in a small form factor. Besides the high performance, the new generation of inverter systems is expected to offer additional functionalities:

(i) Buck-boost operation. The inverter system must cope with the wide voltage variation of a fuel-cell. The fuel-cell voltage is highly dependent on the operating point, as depicted in **Fig. 1(b)**. The fuel-cell voltage is high when no current is drawn, while the fuel-cell voltage is decreasing as the drawn current increases [6]. The inverter has to always guarantee the full speed range of the motor. That is, the inverter must be able to generate the nominal motor voltage, which is proportional to the motor speed, independent of the input voltage fluctuation. It is noted, that similar consideration apply

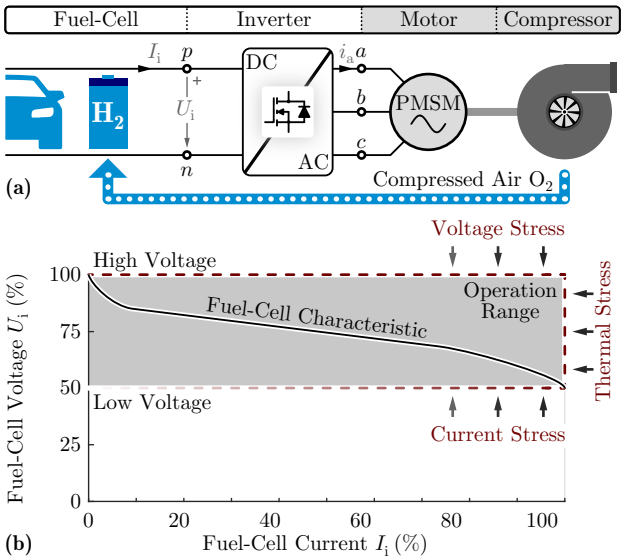

Fig. 1: Motor drive application. **(a)** An electric compressor provides oxygen to the fuel-cell, while a motor drive, directly supplied by the same fuel-cell, controls the electric compressor. **(b)** Fuel-cell voltage-current characteristics.

TABLE I: Specifications of **Fig. 1** motor drive. The nominal operating condition is highlighted in bold.

Fuel-cell voltage	U_i	**60 V**...120 V
Fuel-cell power	P	0 W...**10 kW**
Inverter output freq.	f_m	0 Hz...**5 kHz**
Inverter power	P	0 W...**1.1 kW**
Motor speed	n	0 rpm...**280 krpm**
Motor voltage	$\hat{U}_\mathrm{m}$	0 V...**40 V** (phase, PK)
Motor power	P	0 W...**1 kW**

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for inverters supplied by a battery. In this case, the DC input voltage can significantly fluctuate, depending on the charging status and the operating temperature of the battery.

(ii) High quality motor voltage. High-speed motors are an essential component of power dense motor drives, thanks to their small volume/weight. However, such motors are sensitive to poor current quality, which induces high rotor losses [7], [8]. Therefore, the inverter must guarantee high quality, sinusoidal motor voltages/currents. In addition, the fast switching speeds of the latest generation of wide-bandgap (WBG) semiconductor devices cause high $\mathrm{d}u/\mathrm{d}t > 30\,\mathrm{kV/\mu s}$ [9], [10], which poses a great concern for the motor reliability. The most common problem is premature bearing failure due to high common-mode (CM) $\mathrm{d}u/\mathrm{d}t$ [11]–[13]. For the above reasons, a DM/CM sine-wave output filter must be placed between the inverter and the motor.

There has been extensive research in literature, towards inverter topologies with a wide input-to-output voltage ratio. A conventional voltage source inverter (VSI), only features buck-type functionality, hence cannot be directly used in the examined application. However, by exchanging the DC link capacitor of a VSI, with an LC DC link impedance network, then the Z-source inverter (ZSI) is derived [14], [15]. The ZSI utilizes shoot-through zero states [16], [17], and its unique DC link impedance network, in order to achieve buck-boost capability, i.e. generates AC output voltages which are higher or lower than the input voltage. However, the ZSI suffers from increased voltage/current stress under boost operation, a fact that effectively limits its usability [18]–[20].

Buck-boost inverters with two energy conversion stages, as shown in **Fig. 2**, have found broad acceptance. In order to enable boost functionality, a boost-type DC/DC converter is placed before a VSI. The dedicated boost-type DC/DC converter (DC/DC stage) adapts the fluctuating input voltage U_i to a higher DC link voltage U_DC, when necessary. The DC link voltage supplies the VSI, which generates the AC motor voltages (DC/AC stage). A DM/CM filter is placed after the VSI in order to ensure high quality voltage for the motor. This popular inverter solution is denoted as boost-VSI (B-VSI). A two-stage inverter [21]–[24] processes the transmitted power twice, first in the DC/DC stage and then in the DC/AC stage, thus the overall performance is compromised. The increased number of inductive components and semiconductor losses originating from the DC/DC stage result in a low efficiency and a relatively large volume.

A current source inverter (CSI) based solution can be used instead of the B-VSI [25], [26]. The CSI is inherently a boost-type inverter [27]–[29], i.e. it generates AC output voltages which are strictly greater than the input voltage. In order to enable buck functionality, in addition to the inherent boost functionality of the CSI, a buck-type DC/DC converter must precede the CSI. Therefore, a two-stage inverter topology results, denoted as buck-CSI (B-CSI) [30], [31]. The switches of the CSI have to be realized with two anti-series connected devices (two anti-series MOSFETs or a MOSFET anti-series connected with a diode) [32], a fact that potentially leads to higher complexity, reliability concerns and higher conduction losses. This is a drawback of the B-CSI which limits its practical use.

In response to the shortcomings of the state-of-the-art inverter solutions, the Y-VSI inverter topology [33], [34] of **Fig. 3**, is proposed in this paper. The Y-VSI is based on the well established idea of modular three-phase inverters [35]–[41], where three identical DC/DC converters are connected to a common star "Y" point. In the case of the Y-VSI, each phase-module is equivalent to a non-isolated buck-boost DC/DC converter, while the three phase-modules are connected to the negative DC rail n (star point). The modular concept employed by the Y-VSI is highlighted in **Fig. 4**. The Y-VSI benefits from four key features:

(i) Buck-boost capability. Thanks to the inherent buck-boost characteristics of each phase-module, the AC output voltage can be higher or lower than the DC input voltage.

(ii) High efficiency. The Y-VSI processes the transmitted power P in a unique way. In the typical case, only three out of the six half-bridges are switched, at any given point in time. As a result, low switching losses are generated and a high inverter efficiency is achieved.

(iii) High quality motor voltage. The Y-VSI features an integrated $L_\mathrm{o} - C_\mathrm{o}$ output filter, hence generates continuous/sinusoidal motor voltages. Therefore, no additional filter is required, between the inverter and the motor.

(iv) Simple control strategy. Each phase-module can be controlled independently of the remaining two phases and employs a simple control configuration, similar to conventional DC/DC converters.

In a first step, the operating principle of the Y-VSI is explained in **Sec. II**. In particular, two modulation strategies are proposed, while the uncomplicated control of the Y-VSI is highlighted. In **Sec. III**, the voltage/current stresses on the different inverter components are analytically derived, and are followed by a comprehensive design guideline. The proposed concept is experimentally validated in **Sec. IV**. A Y-VSI hardware prototype and a conventional B-VSI hardware prototype are purposely assembled and compared for the specifications of **Tab. I**. The experimental results validate the performance benefits derived from the Y-VSI technology. Finally, the conclusions are drawn in **Sec. V**.

II. Operation Principle

A three-phase inverter system can be constructed in a modular way [36]–[41] as is visualised in **Fig. 4**. Three identical phase-modules, each comprising a non-isolated DC/DC converter, are connected to a common star "Y" point. Following this modular inverter concept, the Y-VSI of **Fig. 3** consists of three buck-boost DC/DC converters [42] connected to the negative DC rail n (star point). The phase a module comprises two half-bridges, the buck half-bridge $\bar{a}_1$ and the boost half-bridge $\bar{a}_2$, connected to the opposite terminals of an inductor L_o. When the inverter output voltage is lower than the input voltage $u_\mathrm{an} \leq U_\mathrm{i}$, the Y-VSI operates in buck regime of **Fig. 5(a)**, where only the buck half-bridge $\bar{a}_1$ is switched.

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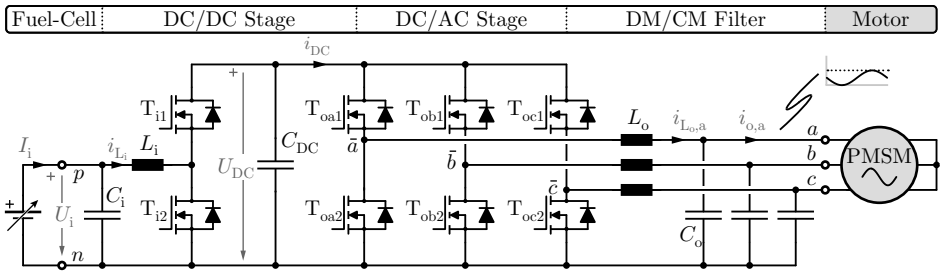

Fig. 2: State-of-the-art boost voltage source inverter (B-VSI) solution for a motor drive with a wide input-to-output voltage ratio. The B-VSI is a two-stage converter: a dedicated DC/DC stage steps-up the fuel-cell voltage U_i to a higher DC link voltage U_DC, while a DC/AC stage generates the three-phase motor voltage system. A differential-mode/common-mode (DM/CM) filter is placed between the inverter and the motor, in order to ensure continuous/sinusoidal motor voltages.

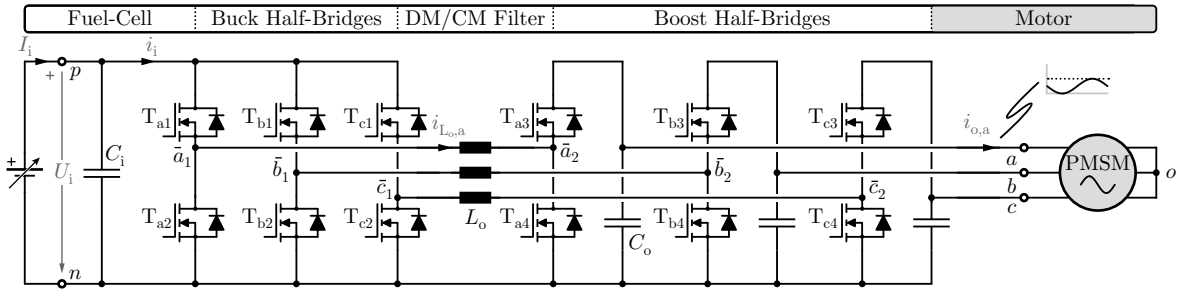

Fig. 3: Proposed Y voltage source inverter (Y-VSI) solution for a motor drive with a wide input-to-output voltage ratio. Three identical buck-boost phase-modules comprise the Y-VSI, as is highlighted in **Fig. 4**. The Y-VSI features an integrated differential-mode/common-mode (DM/CM) output filter, thereby sinusoidal motor voltages/currents are generated.

Contrary, when the inverter output voltage is higher than the input voltage $u_\mathrm{an} > U_\mathrm{i}$, the Y-VSI operates in boost regime of **Fig. 5(b)**, where only the boost half-bridge $\bar{a}_2$ is switched. Furthermore, phase a includes an output capacitor C_o, placed between the output terminal a and the negative DC rail n. The Y-VSI generates three sinusoidal motor phase voltages

$$\begin{aligned} u_\mathrm{m,a}(t) &= u_\mathrm{ao} = \hat{U}_\mathrm{m}\cos(\omega_\mathrm{m}t) \\ u_\mathrm{m,b}(t) &= u_\mathrm{bo} = \hat{U}_\mathrm{m}\cos(\omega_\mathrm{m}t - \frac{2\pi}{3}), \\ u_\mathrm{m,c}(t) &= u_\mathrm{co} = \hat{U}_\mathrm{m}\cos(\omega_\mathrm{m}t + \frac{2\pi}{3}) \end{aligned} \tag{1}$$

where $\omega_\mathrm{m} = 2\pi f_\mathrm{m}$ is the motor fundamental angular velocity. The resulting sinusoidal motor currents are

$$\begin{aligned} i_\mathrm{m,a}(t) &= \hat{I}_\mathrm{m}\cos(\omega_\mathrm{m}t - \phi) \\ i_\mathrm{m,b}(t) &= \hat{I}_\mathrm{m}\cos(\omega_\mathrm{m}t - \frac{2\pi}{3} - \phi). \\ i_\mathrm{m,c}(t) &= \hat{I}_\mathrm{m}\cos(\omega_\mathrm{m}t + \frac{2\pi}{3} - \phi) \end{aligned} \tag{2}$$

For the sake of simplicity, the motor voltage is considered to be in phase with the motor current, i.e. unity power factor $\cos(\phi) = 1 \leftrightarrow \phi = 0$. The modulation index that relates the motor phase voltage amplitude $\hat{U}_\mathrm{m}$ to the fuel-cell voltage U_i is defined

$$M = \frac{\hat{U}_\mathrm{m}}{\frac{1}{2}U_\mathrm{i}}. \tag{3}$$

The modulation index M can exceed the value of $2/\sqrt{3}$, which is the limit of a conventional VSI, thanks to the inherent buck-boost capability of the Y-VSI. Each phase-module is independent of the remaining two phases, thus the analysis is from now focused on phase a, when possible.

A. Sinusoidal Modulation (SPWM)

The sinusoidal motor voltage u_ao cannot be directly generated by phase-module a. The motor phase voltage u_ao assumes negative values, during the negative half-cycle ($\pi/2 < \varphi < 3\pi/2$), while the output voltage of the phase a module (DC/DC converter) must be strictly positive $u_\mathrm{an} \geq 0$. Instead of sinusoidal voltages, the phase-modules $[a, b, c]$ generate sinusoidal voltages with an offset u_off

$$\begin{aligned} u_\mathrm{an}(t) &= \hat{U}_\mathrm{m}\cos(\omega_\mathrm{m}t) + u_\mathrm{off} \\ u_\mathrm{bn}(t) &= \hat{U}_\mathrm{m}\cos(\omega_\mathrm{m}t - \frac{2\pi}{3}) + u_\mathrm{off}, \\ u_\mathrm{cn}(t) &= \hat{U}_\mathrm{m}\cos(\omega_\mathrm{m}t + \frac{2\pi}{3}) + u_\mathrm{off} \end{aligned} \tag{4}$$

such that the output voltages remains always positive e.g. $u_\mathrm{an}(t) \geq 0$. In a first step, a constant offset voltage is selected

$$u_\mathrm{off} = \hat{U}_\mathrm{m}. \tag{5}$$

Therefore, three sinusoidal voltages with the same constant offset voltage are generated with respect to the Y-VSI star point n. The phase a output voltage is

$$u_\mathrm{an}(\varphi) = \hat{U}_\mathrm{m}(\cos(\varphi) + 1). \tag{6}$$

The Y-VSI output voltages in this case are visualized in **Fig. 6(a)**. Even though the inverter output voltages are offseted sinusoids, the line-to-line voltages $u_\mathrm{ab}, u_\mathrm{bc}$ and u_ca are sinusoidal. Accordingly, sinusoidal motor phase currents/voltages appear. Since the inverter output voltages have an offseted

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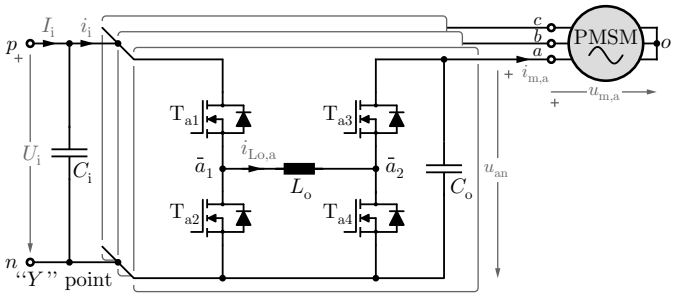

Fig. 4: Modular three-phase inverter concept. Three identical buck-boost DC/DC converter are referenced to a common star "Y" point (negative DC rail n) in order to assemble a modular three-phase inverter system.

sinusoidal shape, the current modulation strategy is denoted as sinusoidal pulse width modulation (SPWM). It is noted that, the offset voltage $u_{\text{off}} = \hat{U}_{\text{m}}$ is common to all three phases and hence constitutes by definition a common-mode (CM) voltage component. A CM voltage component cannot drive any current in a three-phase motor with a floating neutral point o (or grid neutral point, in the case of grid connected inverter).

The characteristic waveforms of a Y-VSI employing SPWM are analysed in the following. Depending on the instantaneous motor voltage $u_{\text{ao}}(t)$ value, the output inverter voltage $u_{\text{an}}(t)$ can be higher or lower than the input voltage U_{i}. Accordingly, phase-module a operates in buck or boost regime as highlighted in **Fig. 6(a)**

$$\begin{array}{lll} \text{buck regime} & m_{\text{a}}(\varphi) \leq 1, & +\varphi_{\text{o}} < \varphi < 2\pi - \varphi_{\text{o}} \\ \text{boost regime} & m_{\text{a}}(\varphi) > 1, & -\varphi_{\text{o}} < \varphi < +\varphi_{\text{o}} \end{array}, \tag{7}$$

where m_{a} is the modulation factor, showing the instantaneous ratio between the inverter output voltage and the input voltage

$$m_{\text{a}}(\varphi) = u_{\text{an}}(\varphi)/U_{\text{i}}. \tag{8}$$

The transition angle from boost to buck regime is

$$\varphi_{\text{o}} = \cos^{-1}\left(\frac{U_{\text{i}} - \hat{U}_{\text{m}}}{\hat{U}_{\text{m}}}\right) \overset{(3)}{=} \cos^{-1}\left(\frac{2}{M} - 1\right). \tag{9}$$

During buck regime in **Fig. 6(c)**, the half-bridge $\bar{a}_1$ (devices $T_{\text{a1}} - T_{\text{a2}}$) is operated with the switching frequency f_{s}, while the high-side switch T_{a3} of the half-bridge $\bar{a}_2$ is continuously turned-on (clamped). In this case, phase-module a reduces to a simple buck converter as is highlighted in **Fig. 5(a)**. During boost regime in **Fig. 6(c)**, the half-bridge $\bar{a}_2$ (devices $T_{\text{a3}} - T_{\text{a4}}$) is operated with the switching frequency f_{s}, while the high-side switch T_{a1} of the half-bridge $\bar{a}_1$ is continuously turned-on (clamped). In this case, phase-module a reduces to a simple boost converter as is highlighted in **Fig. 5(b)**. Depending on the instantaneous output voltage reference $u_{\text{an}}(t)$, the inverter transitions seamlessly between buck and boost regime.

The two half-bridges $\bar{a}_1$ and $\bar{a}_2$ are operated in a mutually exclusive fashion. That is, only one half-bridge is in switching operation, while the high-side switch of the other half-bridge is continuously turned on. In total, only three half-bridges are switched, at any given point in time. As a result, low

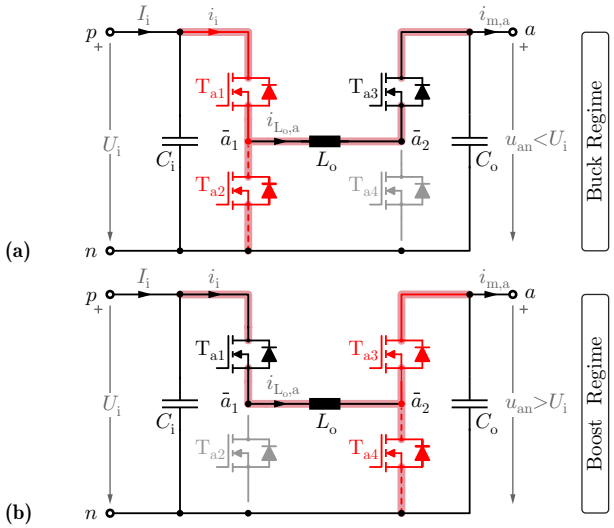

Fig. 5: **(a)** Buck regime of the Y-VSI, where the output voltage is lower than the input voltage $u_{\text{an}}(t) \leq U_{\text{i}}$ and **(b)** boost regime, where the output voltage is greater than the input voltage $u_{\text{an}}(t) > U_{\text{i}}$.

switching losses are generated and high inverter efficiency is achieved. Note that a simple VSI employing SWPM results in continuous switching of three half-bridges, which is the same as the Y-VSI. A VSI is a single-stage inverter from a power conversion perspective. Accordingly, a Y-VSI can also be considered as a single-stage inverter topology, based on the number of switched half-bridges.

The characteristic waveforms of phase a, which are illustrated in **Fig. 6**, are half period symmetric. Therefore, the analytic expressions of those waveforms are calculated for only half of the fundamental period, i.e. in the interval $0 < \varphi = \omega_{\text{m}} t < \pi$. The duty cycles d_{a_1} and d_{a_2} which control the high-side switches of the half-bridges $\bar{a}_1$ and $\bar{a}_2$, respectively, are now calculated. Each point in time t of the offseted sinusoidal output voltage $u_{\text{an}}(t)$, can be considered as a quasi-static operating point of the DC/DC converter phase-module. This is true because the switching frequency is much higher compared to the motor fundamental frequency $f_{\text{s}} \gg f_{\text{m}}$. Thereby, the duty cycles d_{a_1} and d_{a_2} can be derived

$$d_{\text{a}_1}(\varphi) = \min\left[1, m_{\text{a}}(\varphi)\right] = \begin{cases} 1, & 0 < \varphi \leq \varphi_{\text{o}} \\ m_{\text{a}}(\varphi), & \varphi_{\text{o}} < \varphi \leq \pi \end{cases}, \tag{10}$$

$$d_{\text{a}_2}(\varphi) = \min\left[1, \frac{1}{m_{\text{a}}(\varphi)}\right] = \begin{cases} \dfrac{1}{m_{\text{a}}(\varphi)}, & 0 < \varphi \leq \varphi_{\text{o}} \\ 1, & \varphi_{\text{o}} < \varphi \leq \pi \end{cases}. \tag{11}$$

The resulting duty cycles for the SPWM modulation are visualized in **Fig. 6(b)** and are calculated based on **(6)** as

$$d_{\text{a}_1}(\varphi) = \begin{cases} 1, & 0 < \varphi \leq \varphi_{\text{o}} \\ \dfrac{M(1 + \cos(\varphi))}{2}, & \varphi_{\text{o}} < \varphi \leq \pi \end{cases}, \tag{12}$$

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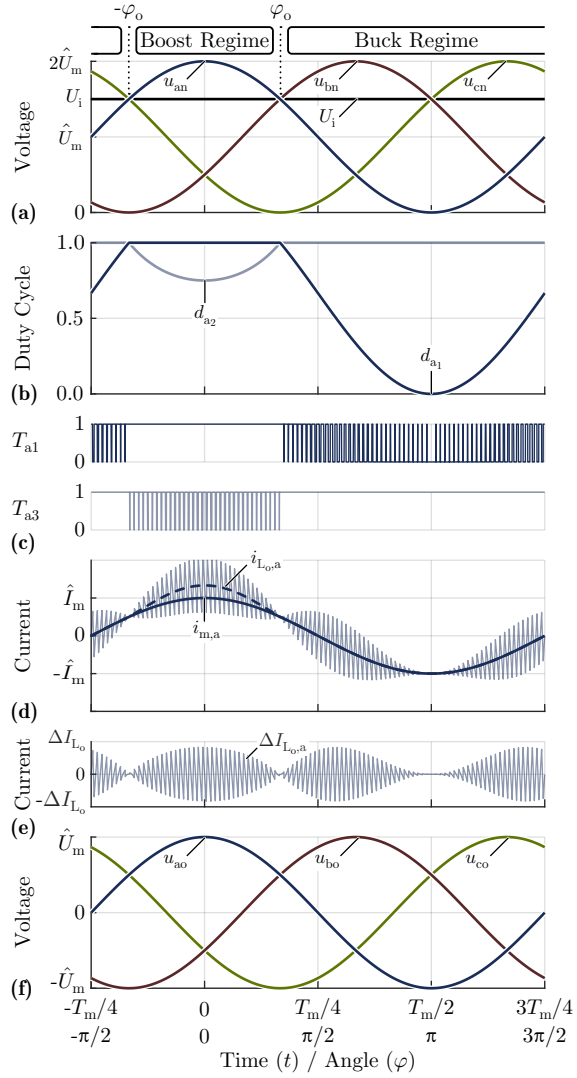

Fig. 6: Sinusoidal modulation strategy (SPWM) characteristic waveforms. **(a)** Inverter output voltages (offseted sinusoidal shape). **(b)** Phase a duty cycles followed by **(c)** gate signals. **(d)** Phase a filter inductor current and motor current, **(e)** filter inductor current ripple and **(f)** motor voltages.

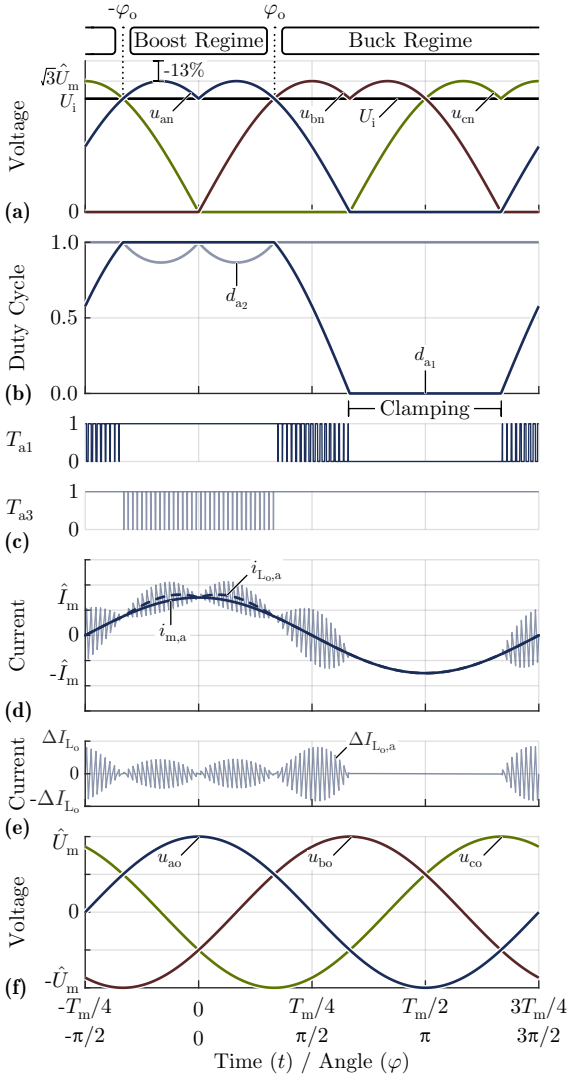

Fig. 7: Discontinuous modulation strategy (DPWM) characteristic waveforms. **(a)** Inverter output voltages (non-sinusoidal shape). **(b)** Phase a duty cycles followed by **(c)** gate signals. **(d)** Phase a filter inductor current and motor current, **(e)** filter inductor current ripple and **(f)** motor voltages.

TABLE II: Y-VSI characteristic waveforms, for sinusoidal modulation (SPWM) and discontinuous modulation (DPWM).

	SPWM ($M \geq 1$)		**DPWM** ($M \geq 4/3$)	
$u_{\text{off}}(\varphi)$	$\hat{U}_{\text{m}}$		$-\min[u_{\text{ao}}(\varphi), u_{\text{bo}}(\varphi), u_{\text{co}}(\varphi)]$	
$u_{\text{an}}(\varphi)$	$\hat{U}_{\text{m}}(\cos(\varphi)+1)$		$\begin{cases} \hat{U}_{\text{m}}(\cos(\varphi)-\cos(\varphi+\frac{2\pi}{3})), \\ 0, \end{cases}$	$0<\varphi<2\pi/3$ $2\pi/3<\varphi<\pi$
φ_{o}	$\cos^{-1}\left(\frac{2}{M}-1\right)$		$\cos^{-1}\left(\frac{2}{\sqrt{3}M}\right)+\frac{\pi}{6}$	
$d_{\text{a}_1}(\varphi)$	$\begin{cases} 1, \\ \frac{M(1+\cos(\varphi))}{2}, \end{cases}$	$0<\varphi\leq\varphi_{\text{o}}$ $\varphi_{\text{o}}<\varphi\leq\pi$	$\begin{cases} 1, \\ \frac{M(\cos(\varphi)-\cos(\varphi+\frac{2\pi}{3}))}{2}, \\ 0, \end{cases}$	$0<\varphi\leq\varphi_{\text{o}}$ $\varphi_{\text{o}}<\varphi\leq 2\pi/3$ $2\pi/3<\varphi\leq\pi$
$d_{\text{a}_2}(\varphi)$	$\begin{cases} \frac{2}{M(1+\cos(\varphi))}, \\ 1, \end{cases}$	$0<\varphi\leq\varphi_{\text{o}}$ $\varphi_{\text{o}}<\varphi\leq\pi$	$\begin{cases} \frac{2}{M(\cos(\varphi)-\cos(\varphi+\frac{2\pi}{3}))}, \\ 1, \end{cases}$	$0<\varphi\leq\varphi_{\text{o}}$ $\varphi_{\text{o}}<\varphi\leq\pi$
$i_{\text{L}_{\text{o}},\text{a}}(\varphi)$	$\begin{cases} \hat{I}_{\text{m}}\cos(\varphi)\frac{M}{2}(\cos(\varphi)+1), \\ \hat{I}_{\text{m}}\cos(\varphi), \end{cases}$	$0<\varphi\leq\varphi_{\text{o}}$ $\varphi_{\text{o}}<\varphi\leq\pi$	$\begin{cases} \hat{I}_{\text{m}}\cos(\varphi)\frac{M}{2}(\cos(\varphi)-\cos(\varphi+\frac{2\pi}{3})), \\ \hat{I}_{\text{m}}\cos(\varphi), \end{cases}$	$0<\varphi\leq\varphi_{\text{o}}$ $\varphi_{\text{o}}<\varphi\leq\pi$

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$$d_{\mathrm{a_2}}(\varphi) = \begin{cases} \dfrac{2}{M(1+\cos(\varphi))}, & 0 < \varphi \leq \varphi_\mathrm{o} \\ 1, & \varphi_\mathrm{o} < \varphi \leq \pi \end{cases}. \tag{13}$$

Each phase-module features an integrated output filter ($L_\mathrm{o}-C_\mathrm{o}$) which allows for the continuous output voltages of **Fig. 6(a)**. The filter inductor characteristics are now analysed. The inductor current comprises a fundamental current component $i_{\mathrm{L_o}}(\varphi)$ and a current ripple $\Delta i_{\mathrm{L_o}}(\varphi)$ which is the result of the PWM operation. The fundamental inductor current is

$$i_{\mathrm{L_o,a}}(\varphi) = \frac{i_{\mathrm{m,a}}}{d_{\mathrm{a_2}}} = \begin{cases} \hat{I}_\mathrm{m}\cos(\varphi)\dfrac{1}{d_{\mathrm{a_2}}}, & 0 < \varphi \leq \varphi_\mathrm{o} \\ \hat{I}_\mathrm{m}\cos(\varphi), & \varphi_\mathrm{o} < \varphi \leq \pi \end{cases}. \tag{14}$$

In the case of SPWM, the inductor current is depicted in **Fig. 6(d)** and is calculated based on **(2)** and **(13)** as

$$i_{\mathrm{L_o,a}}(\varphi) = \begin{cases} \hat{I}_\mathrm{m}\cos(\varphi)\dfrac{M}{2}(\cos(\varphi)+1), & 0 < \varphi \leq \varphi_\mathrm{o} \\ \hat{I}_\mathrm{m}\cos(\varphi), & \varphi_\mathrm{o} < \varphi \leq \pi \end{cases}. \tag{15}$$

The inductor current waveform is non-sinusoidal. The maximum inductor current occurs during boost regime for $\varphi = 0$ and is

$$\hat{I}_{\mathrm{L_o}} = \hat{I}_\mathrm{m} M, \tag{16}$$

which is greater than the motor current amplitude $\hat{I}_\mathrm{m}$. The inductor current of **(15)** can be approximated by a simpler waveform

$$i_{\mathrm{L_o,a}}(\varphi) = \hat{I}_\mathrm{m}\left(\frac{M+1}{2}\cos(\varphi) + \frac{M-1}{2}\right), \tag{17}$$

which allows to calculate the RMS current of the filter inductor

$$I_{\mathrm{L_o,RMS}} = \frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\frac{\sqrt{3M^2-2M+3}}{2}. \tag{18}$$

The current ripple of the inductor $\Delta i_{\mathrm{L_o}}$ is isolated in **Fig. 6(e)**. The maximum occurring current ripple value (single-side amplitude) is

$$\Delta I_{\mathrm{L_o}} = \max\left[1, 4\frac{M-1}{M}\right]\cdot\frac{U_\mathrm{i}}{8L_\mathrm{o}f_\mathrm{s}}. \tag{19}$$

Finally, the output capacitor C_o is analysed. The voltage u_an across the capacitor is continuous, thus the Y-VSI provides a high quality voltage for the motor and no additional filtering is required at the AC output side. A voltage ripple $\Delta u_{\mathrm{C_o}}$ is superimposed to the filter capacitor C_o voltage due to the PWM operation of the Y-VSI. The maximum occurring voltage ripple value (single-side amplitude) is

$$\Delta U_{\mathrm{C_o}} = \Delta U_\mathrm{an} = \max\left[\frac{U_\mathrm{i}}{64L_\mathrm{o}C_\mathrm{o}f_\mathrm{s}^2}, \frac{M\hat{I}_\mathrm{m}}{8C_\mathrm{o}f_\mathrm{s}}\right]. \tag{20}$$

A voltage ripple of $\Delta U_\mathrm{an} < 2\,\mathrm{V}$ should be achieved, in order to avoid parasitic bearing currents [43], [44].

The characteristic waveforms, corresponding to SPWM modulation strategy, are summarized in **Tab. II**. The derived formulas are valid for a modulation index $M \geq 1$. For this modulation index range, the Y-VSI transitions between buck and boost regime (cf. **Fig. 5** and **6**). For a lower modulation index $M = 0...1$ the Y-VSI operates exclusively in buck regime, over the whole fundamental period, hence is equivalent to a simple VSI. The properties of the Y-VSI in the modulation range $M = 0...1$ are discussed in **Appx. A**.

B. Discontinuous Modulation (DPWM)

The offset voltage u_off of **(4)**, was selected to be constant for the sinusoidal modulation (SPWM), in **(5)**. However, this is not necessary: The offset voltage u_off is a degree of freedom that can be utilized in order to further improve the inverter performance. By selecting a time-varying offset voltage $u_\mathrm{off}(t)$ significant performance advantages can be achieved.

In the case of a two-level VSI, this degree of freedom has been extensively detailed in literature. By employing a time-varying offset voltages and/or common-mode voltage injection [45], [46], different modulation strategies are derived: For example, in the case of third harmonic injection [47], a sinusoidal offset voltage (third harmonic) is injected, while in the case of triangular voltage insertion [48], a triangular offset voltage is used. These modulation strategies allow for an optimal utilization of the VSI DC link voltage. In the case of discontinuous modulation (DPWM) [49], it is possible to generate a three-phase voltage system for the motor by switching only two out of the three phases of the VSI. Accordingly, the switching losses of the VSI are significantly reduced. There are many variants of DPWM [50], but in all cases a discontinuous offset voltage is injected.

The DPWM modulation concept is now extended for the Y-VSI. In particular, the time-varying offset voltage is

$$u_\mathrm{off}(t) = -\min[u_\mathrm{ao}(t), u_\mathrm{bo}(t), u_\mathrm{co}(t)]. \tag{21}$$

The Y-VSI output voltages are equal to the sum of the respective motor voltages and the offset voltage, according to **(4)**. The three-phase output voltages are illustrated in **Fig. 7(a)**, while the output voltage of phase a in particular is

$$u_\mathrm{an}(\varphi) = \begin{cases} u_\mathrm{ao} - u_\mathrm{bo}, & -\dfrac{2\pi}{3} < \varphi < 0 \\ u_\mathrm{ao} - u_\mathrm{co}, & 0 < \varphi < \dfrac{2\pi}{3} \\ u_\mathrm{ao} - u_\mathrm{ao}, & \dfrac{2\pi}{3} < \varphi < \dfrac{4\pi}{3} \end{cases} \tag{22}$$

$$u_\mathrm{an}(\varphi) = \begin{cases} \hat{U}_\mathrm{m}\left[\cos(\varphi) - \cos(\varphi - \dfrac{2\pi}{3})\right], & -\dfrac{2\pi}{3} < \varphi < 0 \\ \hat{U}_\mathrm{m}\left[\cos(\varphi) - \cos(\varphi + \dfrac{2\pi}{3})\right], & 0 < \varphi < \dfrac{2\pi}{3} \\ 0, & \dfrac{2\pi}{3} < \varphi < \dfrac{4\pi}{3} \end{cases}. \tag{23}$$

According to DPWM, the phase with the most negative motor voltage is clamped to the negative DC rail n, for one third of the fundamental period $T_\mathrm{m}/3$. Phase a in particular is clamped for the interval $\frac{2\pi}{3} < \varphi < \frac{4\pi}{3}$ in **Fig. 7(c)**. The output voltages of **Fig. 7(a)** have a non-sinusoidal shape, however the line-to-line motor voltages are sinusoidal. Therefore it

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is possible by means of DPWM to generate a sinusoidal three-phase motor voltage system with non-sinusoidal inverter output voltages. The DPWM modulation benefits from two key advantages compared to SPWM: **(i)** Reduction of the total Y-VSI switching transitions by 33% [21]. During one third of the fundamental motor period $T_\mathrm{m}/3$ (i.e. the interval $\frac{2\pi}{3} < \varphi < \frac{4\pi}{3}$), the phase-module a is clamped, thus no switching losses are generated from this phase-module. **(ii)** Reduction of the voltage stress on the boost half-bridges $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ by 13%. The phase a boost half-bridge $\bar{a}_2$ processes/switches the output voltage u_an. The DPWM can generate the same motor phase voltage amplitude $\hat{U}_\mathrm{m}$ as SWPM, but with the non-sinusoidal output voltages of **Fig. 7(a)**. The maximum value of those output voltages is $U_\mathrm{an,PK} = \sqrt{3}\hat{U}_\mathrm{m}$ which is 13% lower compared to the respective value for SPWM $U_\mathrm{an,PK} = 2\hat{U}_\mathrm{m}$.

The characteristic waveforms of a Y-VSI employing DPWM are analysed in the following. Depending on the instantaneous motor voltage $u_\mathrm{ao}(t)$ value, the output inverter voltage $u_\mathrm{an}(t)$ can be higher or lower than the input voltage U_i. Accordingly, the phase-module a operates in boost regime (cf. **Fig. 5(b)**) or buck regime (cf. **Fig. 5(a)**). The two operation regimes are highlighted on **Fig. 7(a)** and are analytically expressed in **(7)**. The angle φ_o, where the transition from boost to buck regime occurs, is

$$\varphi_\mathrm{o} = \cos^{-1}\left(\frac{U_\mathrm{i}}{\sqrt{3}\hat{U}_\mathrm{m}}\right) + \frac{\pi}{6} \overset{(3)}{=} \cos^{-1}\left(\frac{2}{\sqrt{3}M}\right) + \frac{\pi}{6}. \quad (24)$$

The duty cycles d_{a_1} and d_{a_2}, that control the half-bridges $\bar{a}_1$ and $\bar{a}_2$, are illustrated in **Fig. 7(b)** and are calculated based on **(10)** and **(11)** as

$$d_{\mathrm{a}_1}(\varphi) = \begin{cases} 1, & 0 < \varphi \leq \varphi_\mathrm{o} \\ \dfrac{M(\cos(\varphi) - \cos(\varphi + \frac{2\pi}{3}))}{2}, & \varphi_\mathrm{o} < \varphi \leq \dfrac{2\pi}{3} \\ 0, & \dfrac{2\pi}{3} < \varphi \leq \pi \end{cases}, \quad (25)$$

$$d_{\mathrm{a}_2}(\varphi) = \begin{cases} \dfrac{2}{M(\cos(\varphi) - \cos(\varphi + \frac{2\pi}{3}))}, & 0 < \varphi \leq \varphi_\mathrm{o} \\ 1, & \varphi_\mathrm{o} < \varphi \leq \pi \end{cases}. \quad (26)$$

The integrated output filter is finally analysed, starting from the filter inductor L_o. In the case of DPWM, the inductor current is depicted in **Fig. 7(d)** and is calculated base on **(2)**, **(14)** and **(26)** as

$$i_{\mathrm{L_o,a}}(\varphi) = \begin{cases} \hat{I}_\mathrm{m}\cos(\varphi)\dfrac{M}{2}(\cos(\varphi) - \cos(\varphi + \dfrac{2\pi}{3})), & 0 < \varphi \leq \varphi_\mathrm{o} \\ \hat{I}_\mathrm{m}\cos(\varphi), & \varphi_\mathrm{o} < \varphi \leq \pi \end{cases}. \quad (27)$$

The inductor current waveform is non-sinusoidal, and is approximated by a simpler waveform

$$i_{\mathrm{L_o}}(\varphi) = \hat{I}_\mathrm{m}\left(\frac{M\sqrt{3}+2}{4}\cos(\varphi) + \frac{M\sqrt{3}-2}{4}\right). \quad (28)$$

The maximum inductor current is greater than the motor current amplitude $\hat{I}_\mathrm{m}$ and occurs during boost regime

$$\hat{I}_{\mathrm{L_o}} = \hat{I}_\mathrm{m}\frac{\sqrt{3}}{2}M, \quad (29)$$

while the RMS current of the filter inductor is

$$I_{\mathrm{L_o,RMS}} = \frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\frac{\sqrt{9M^2 - 4\sqrt{3}M + 12}}{4}. \quad (30)$$

A current ripple is superimposed to the inductor current due to the PWM operation of the Y-VSI (cf. **Fig. 7(d)**). The current ripple of the inductor $\Delta i_{\mathrm{L_o}}$ is isolated in **Fig. 6(e)**, while the maximum occurring current ripple value (single-side amplitude) is

$$\Delta I_{\mathrm{L_o}} = \max\left[1, 4\frac{\frac{\sqrt{3}}{2}M - 1}{\frac{\sqrt{3}}{2}M}\right] \cdot \frac{U_\mathrm{i}}{8L_\mathrm{o}f_\mathrm{s}}. \quad (31)$$

Finally, the output capacitor C_o is analysed. A voltage ripple is superimposed to the continuous output voltages of **Fig. 7(a)**, due to the PWM operation of the Y-VSI. The maximum occurring voltage ripple value across the filter capacitor C_o (single-side amplitude) is

$$\Delta U_{\mathrm{C_o}} = \Delta U_\mathrm{an} = \max\left[\frac{U_\mathrm{i}}{64L_\mathrm{o}C_\mathrm{o}f_\mathrm{s}^2}, \frac{\frac{\sqrt{3}}{2}M\hat{I}_\mathrm{m}}{8C_\mathrm{o}f_\mathrm{s}}\right]. \quad (32)$$

A voltage ripple of $\Delta U_\mathrm{an} < 2\,\mathrm{V}$ should be achieved, in order to avoid parasitic bearing currents.

The characteristic waveforms, corresponding to DPWM modulation strategy, are summarized in **Tab. II** and are valid for a modulation index $M \geq 4/3$. For this modulation index range, the Y-VSI alternates between buck and boost regime (cf. **Fig. 5** and **7**). For a low modulation index $M = 0...2/\sqrt{3}$ the Y-VSI operates exclusively in buck regime, over the whole fundamental period, hence is equivalent to a simple VSI. The properties of the Y-VSI in the modulation range $M = 0...2/\sqrt{3}$ are discussed in **Appx. A**. Finally for a modulation index $M = 2/\sqrt{3}...4/3$, the Y-VSI alternates several times between buck and boost regime during the fundamental period. The analytic formulas of **Tab. II** can be used as an approximation in the modulation range $M = 2/\sqrt{3}...4/3$.

C. Control System

A complete control system is now conceptualized for the Y-VSI and is illustrated in **Fig. 8**. The goal of the control system is to maintain the desired motor speed set-point $\omega = \omega^*$. To this end, a standard cascaded speed-torque controller, referenced to the dq-axis frame, is used for the motor. The motor controller receives the speed ω, the position angle ε, and the terminal currents $[i_\mathrm{m,a}, i_\mathrm{m,b}, i_\mathrm{m,c}]$ as input. In return, the motor controller outputs the motor terminal voltage references $[u^*_\mathrm{m,a}, u^*_\mathrm{m,b}, u^*_\mathrm{m,c}]$.

The Y-VSI ensures that the motor voltages $[u_\mathrm{m,a}, u_\mathrm{m,b}, u_\mathrm{m,c}]$ follow the respective sinusoidal references $[u^*_\mathrm{m,a}, u^*_\mathrm{m,b}, u^*_\mathrm{m,c}]$. Each phase-module of the Y-VSI is operated independently, hence the control block diagram is visualized for only phase a

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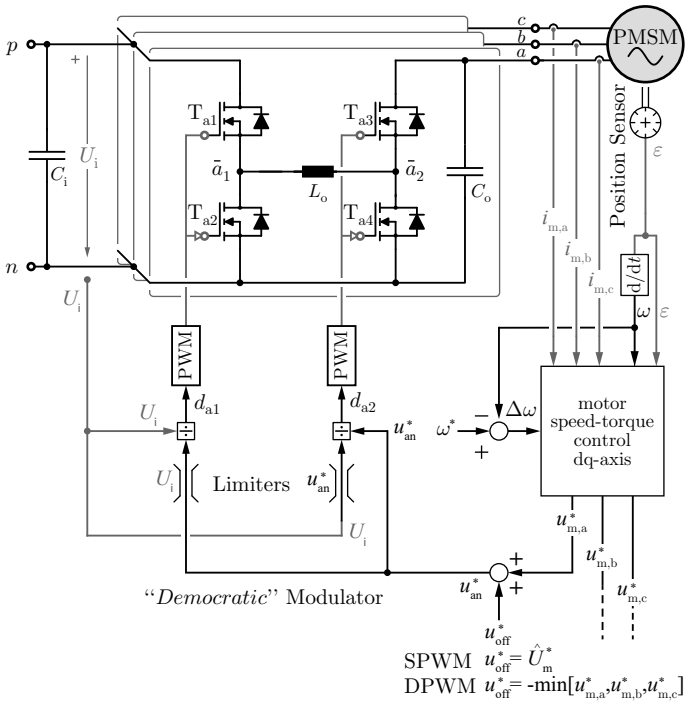

Fig. 8: Y-VSI control block diagram. A standard cascaded speed-torque controller is used, in order to maintain the desired motor speed set-point $\omega = \omega^*$. The motor controller outputs the three motor voltage references, e.g. $u^*_{m,a}$, that the Y-VSI must generate. Each phase-module of the Y-VSI is operated independently, hence only phase a is depicted. The modulator translates the inverter output voltage reference u^*_{an} into appropriate duty cycles d_{a1} and d_{a2}.

in **Fig. 8**. An offset voltage u^*_{off} is added to the motor terminal voltage reference $u^*_{m,a}$, in order to form the strictly positive phase-module output voltage reference u^*_{an}. The added offset depends on the employed modulation strategy In the case of SPWM, the offset is constant and is given by **(5)**, while in the case of DPWM the offset is time-varying and is given by **(21)**. Finally, the modulator translates the voltage reference u^*_{an} directly into the duty cycles d_{a1} and d_{a2}. The depicted block diagram of the modulator in **Fig. 8** is based on the formulas **(10)** and **(11)**. The modulator follows a "*democratic*" strategy, in the sense that both the buck half-bridge $\bar{a}_1$ and boost half-bridge $\bar{a}_2$ are switched (but not simultaneously) in order to generate the reference voltage u^*_{an}.

The presented in **Fig. 8** control system is suitable for motor drive applications with slow dynamic response, such as compressor drives (cf. **Fig. 1**). In the case of servo drives, which require fast dynamic response, the inductor L_o current must be directly controlled. A Y-VSI control system with direct inductor current control is presented in [33].

III. Component Stresses

In this section, the stresses on the different inverter components are analytically derived. The presented results are general and can be used for drive systems (or grid connected inverters) with any specifications. The analytic expressions are applied to a drive system of **Fig. 1** and **Tab. I**. For the considered drive application example, the nominal fuel-cell voltage is $U_i = 60\,\mathrm{V}$, while the motor voltage ranges within $\hat{U}_m = 0\,\mathrm{V}...40\,\mathrm{V}$ (phase amplitude). The nominal motor voltage/power operation ($\hat{U}_m = 40\,\mathrm{V}, P = 1\,\mathrm{kW}$), that corresponds to a modulation index of $M = 4/3$, yields the highest component stresses. For the sake of simplicity, a resistive load $R = 3\hat{U}^2_{m,max}/2P_{max} = 2.4\,\Omega$ is assumed, which corresponds to a unity power factor, $\cos(\phi) = 1$. Thereby, the transferred power P, fuel-cell current I_i and motor fundamental phase current amplitude $\hat{I}_m$ can be derived as a function of the modulation index

$$P = M^2\frac{3U_i^2}{8R},\ I_i = M^2\frac{3U_i}{8R},\ \hat{I}_m = M\frac{U_i}{2R}. \tag{33}$$

In order to further simplify the analysis, the current ripple of the filter inductor L_o is neglected, unless stated otherwise. Furthermore, the two half-bridges comprising each phase-module (e.g. half-bridges $\bar{a}_1$ and $\bar{a}_2$ for phase-module a) are assumed to be identical.

A. Sinusoidal Modulation (SPWM)

The component stresses are analytically derived for a modulation index range $M = 1...2$. For this modulation range the Y-VSI generates motor voltages amplitudes $\hat{U}_m$ greater than the input voltage U_i (buck and boost regime). For a low modulation index $M = 0...1$, the Y-VSI is equivalent to a simple two-level VSI (buck regime) as shown in **Fig. 5(a)**. The component stresses for a low modulation index case are derived in **Appx. A**.

1) Semiconductor Voltage Stress: The semiconductors of the buck half-bridges $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ are blocking/switching the DC input voltage U_i independent of the employed modulation strategy

$$U_{T1} = U_{T2} = U_i. \tag{34}$$

In contrast, the boost half-bridges $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ are blocking the time-varying inverter output voltages (e.g. voltage $u_{an}(\varphi)$ for half-bridge $\bar{a}_2$), which depend on the employed modulation strategy. Therefore, the maximum inverter output voltage value from **Fig. 6(a)** defines the voltage stress on the boost half-bridge semiconductor devices

$$U_{T3} = U_{T4} = 2\hat{U}_m. \tag{35}$$

2) Semiconductor Current Stress: The RMS current stress of the semiconductor devices is plotted in **Fig. 9** and is analytically approximated by

$$I_{T1,RMS} = I_{L_o,RMS}\sqrt{-\frac{\sqrt{3}}{\pi^2}M^2 + (1-\frac{\sqrt{3}}{\pi^2})M + 1 - \frac{2}{\sqrt{3}}}, \tag{36}$$

$$I_{T2,RMS} = I_{L_o,RMS}\sqrt{+\frac{\sqrt{3}}{\pi^2}M^2 - (1-\frac{\sqrt{3}}{\pi^2})M + \frac{2}{\sqrt{3}}}, \tag{37}$$

$$I_{T3,RMS} = I_{L_o,RMS}\sqrt{+\frac{1}{2\pi^2}M^2 - \frac{8}{15}M + \frac{3}{2}}, \tag{38}$$

$$I_{T4,RMS} = I_{L_o,RMS}\sqrt{-\frac{1}{2\pi^2}M^2 + \frac{8}{15}M - \frac{1}{2}}, \tag{39}$$

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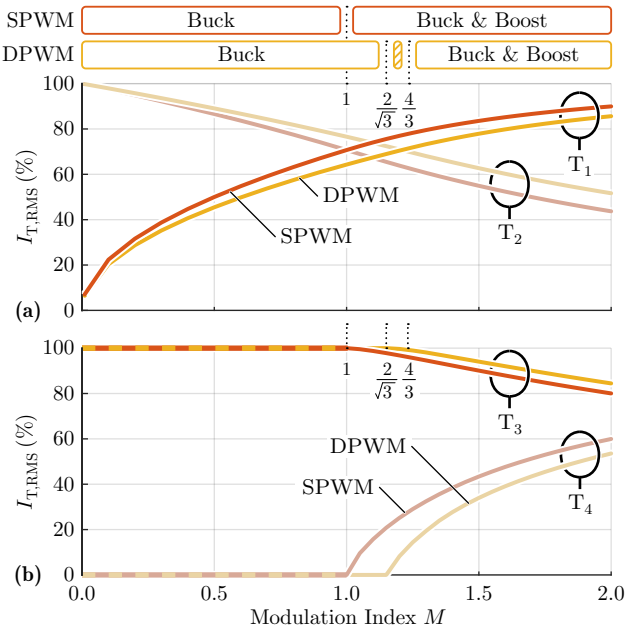

Fig. 9: **(a)** Buck half-bridge high-side T_1 and low-side T_2 switch RMS current stress, normalized with respect to the RMS inductor current $I_{\mathrm{L_o,RMS}}$. **(b)** Boost half-bridge high-side T_3 and low-side T_4 switch RMS current stress, also normalized with respect to $I_{\mathrm{L_o,RMS}}$.

where the RMS current of the inductor $I_{\mathrm{L_o,RMS}}$ is given by **(18)**. As shown in **Fig. 9**, the current stress on the semiconductor devices is asymmetric and depends on the modulation index M. In the most extreme case example, for the modulation index range $M = 0...1$, the high-side switch T_{a3} conducts the total motor current, while the low-side switch T_{a4} conducts no current. Therefore, the current rating of the semiconductor devices must be carefully selected in order to account for this asymmetric current stress.

3) Semiconductor Conduction Losses: The conduction losses of the Y-VSI semiconductor devices are

$$P_{\mathrm{cd}} = 6 I^2_{\mathrm{L_o,RMS}} R_{\mathrm{T,on}}, \tag{40}$$

where $R_{\mathrm{T,on}}$ is the on-state resistance of each (unipolar) power semiconductor device and $I_{\mathrm{L_o,RMS}}$ is the RMS current of the filter inductor L_{o}. It is reminded that, the current ripple is neglected, for the inductor RMS current calculation. Therefore, the conduction losses are calculated for SPWM based on **(18)** and **(40)**

$$P_{\mathrm{cd}} = 6 \frac{\hat{I}^2_{\mathrm{m}}}{2} \frac{3M^2 - 2M + 3}{4} R_{\mathrm{T,on}}. \tag{41}$$

4) Semiconductor Switching Losses: In a half-bridge, the switching energy dissipation E_{sw}, associated with a hard switching transition, is approximated as a linear function of the commutation current I_{sw} as

$$E_{\mathrm{sw}}(I_{\mathrm{sw}}) = k_0 + k_1 I_{\mathrm{sw}}. \tag{42}$$

Accordingly, the switching power dissipation for a switching frequency f_{s} is

$$P_{\mathrm{sw}}(I_{\mathrm{sw}}) = f_{\mathrm{s}} E_{\mathrm{sw}} = f_{\mathrm{s}} \left(k_0 + k_1 I_{\mathrm{sw}}\right). \tag{43}$$

The parameters k_0 and k_1 depend on the commutation (switched) voltage U_{sw}. Namely, the parameter k_0 represents the constant part of the switching losses and is calculated in literature [51] (assuming unipolar power semiconductors) as

$$k_0(U_{\mathrm{sw}}) = Q_{\mathrm{oss}}(U_{\mathrm{sw}}) \cdot U_{\mathrm{sw}}, \tag{44}$$

where Q_{oss} is the electric charge stored in the non-linear output parasitic capacitance C_{oss} of the MOSFET

$$Q_{\mathrm{oss}}(U_{\mathrm{sw}}) = \int_0^{U_{\mathrm{sw}}} C_{\mathrm{oss}}(u) \mathrm{d}u. \tag{45}$$

Besides the commutation voltage U_{sw}, the parameter k_1 depends on the semiconductor technology and the gate driver configuration [52], [53].

The switching losses of the Y-VSI are now derived, staring from the buck half-bridges. The buck half-bridge $\bar{a}_1$ is switched only during the buck regime of **Fig. 6**, i.e. when $u_{\mathrm{an}}(\varphi) \leq U_{\mathrm{i}}$. The commutation voltage of the buck half-bridge $\bar{a}_1$ is constant and equal to the input voltage $U_{\mathrm{sw},1} = U_{\mathrm{i}}$. The commutation current is equal to the inductor current and hence varies over time $i_{\mathrm{sw},1}(\varphi) = i_{\mathrm{L_o,a}}(\varphi)$. An integration of the local (instantaneous) switching losses of **(43)** must be performed over the fundamental period T_{m} in order to derive the total switching losses caused by the buck half-bridges

$$P_{\mathrm{sw},1} = \frac{3 f_{\mathrm{s}}}{\pi} \int_{\phi_{\mathrm{o}}}^{\pi} \left[k_0 + k_1 i_{\mathrm{L_o}}(\varphi)\right] \mathrm{d}\varphi. \tag{46}$$

The switching parameters k_0 and k_1 are calculated for the constant commutation voltage of $U_{\mathrm{sw},1} = U_{\mathrm{i}}$. The resulting sum of switching losses for the three buck half-bridges, when SPWM modulation is used, is

$$P_{\mathrm{sw},1} = 3 f_{\mathrm{s}} \left(k_0 \frac{\pi - \varphi_{\mathrm{o}}}{\pi} + k_1 \frac{2}{\pi} \hat{I}_{\mathrm{m}} (1 - \frac{1}{2} \sin(\varphi_{\mathrm{o}})) \right), \tag{47}$$

where the sin of the transition angle φ_{o} is

$$\sin(\varphi_{\mathrm{o}}) \overset{(9)}{=} \frac{2}{M} \sqrt{M - 1}. \tag{48}$$

Furthermore, the switching parameters k_0 and k_1 of **(47)** are calculated for the constant commutation voltage of the buck half-bridges $U_{\mathrm{sw},1} = U_{\mathrm{i}}$.

The boost half-bridge $\bar{a}_2$ is switched only during the boost regime of **Fig. 6**, i.e. when $u_{\mathrm{an}}(\varphi) > U_{\mathrm{i}}$. The commutation voltage of the boost half-bridge $\bar{a}_2$ is equal to the inverter output voltage and hence varies over time $u_{\mathrm{sw},2}(\varphi) = u_{\mathrm{an}}(\varphi)$. The commutation current is equal to the inductor current $i_{\mathrm{sw},2}(\varphi) = i_{\mathrm{L_o,a}}(\varphi)$ and is also time-varying. An integration of the local switching losses of **(43)** must be performed over the fundamental period T_{m} in order to derive the total switching losses caused by the boost half-bridges

$$P_{\mathrm{sw},2} = \frac{3 f_{\mathrm{s}}}{\pi} \int_{0}^{\phi_{\mathrm{o}}} \left[k_0(\varphi) + k_1(\varphi) i_{\mathrm{L_o}}(\varphi)\right] \mathrm{d}\varphi, \tag{49}$$

where the switching parameters $k_0(\varphi)$ and $k_1(\varphi)$ are varying over time and depend on the instantaneous commutation voltage $u_{\mathrm{sw},2}(\varphi)$. The resulting sum of switching losses for

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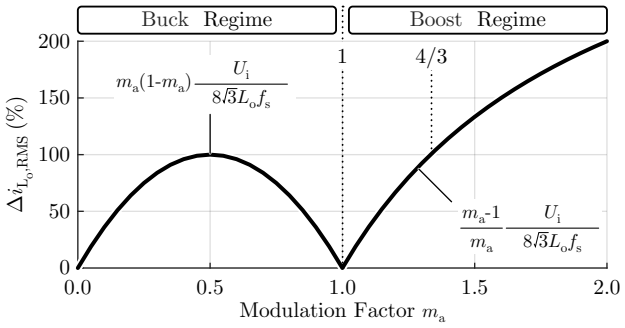

Fig. 10: Local (instantaneous) RMS current of the filter inductor L_o, normalized with respect to $\frac{U_i}{8\sqrt{3}L_o f_s}$. The local RMS current ripple depends on the modulation factor $m_a(\varphi) = u_{an}(\varphi)/U_i$ of **(8)**.

the three boost half-bridges, when SPWM modulation is used, is approximated by

$$P_{sw,2} = 3f_s(k_0 + k_1 M \hat{I}_m)\frac{\sin(\varphi_o)}{\pi}, \tag{50}$$

where $\sin(\varphi_o)$ is given in **(48)**. The switching parameters k_0 and k_1 of **(50)** are calculated for the highest commutation voltage of the boost half-bridges $U_{sw,2} = u_{an}(0) = 2\hat{U}_m$. The total switching losses of the Y-VSI are the sum of the perspective buck half-bridges' and boost half-bridges' switching losses

$$P_{sw} = P_{sw,1} + P_{sw,2}. \tag{51}$$

5) Passive Components Selection: The integrated output filter ($L_o - C_o$) of the Y-VSI is now analysed in detail, starting from the filter inductors L_o. The current of the filter inductor is non-sinusoidal, as is described by **(15)** and shown in **Fig. 6(d)**. The maximum current stress on the inductor depends on the modulation index M, is given in **(16)** and is plotted in **Fig. 11(a)**. The peak current ripple of the filter inductor is given by **(19)**. Accordingly, in order to limit this current ripple to a maximum value of ΔI_{L_o}, the inductance value must be selected as

$$L_o \geq \max\left[1, 4\frac{M-1}{M}\right] \cdot \frac{U_i}{8\Delta I_{L_o} f_s}, \tag{52}$$

where $M = M_{max}$ is the highest possible modulation index within the inverter operating range. In general, there is a direct relation between the inductor losses and the RMS inductor current ripple $\Delta I_{L_o,RMS}$, as a high RMS current ripple results in a high frequency RMS flux density and hence substantial core losses [54]. In addition, a high RMS current ripple causes high-frequency winding losses due to skin and proximity effect. Therefore, the RMS inductor current ripple $\Delta I_{L_o,RMS}$ is a reasonable performance indicator for the design of the inductive components and is calculated in the following. The local (instantaneous) RMS current ripple of the filter inductor

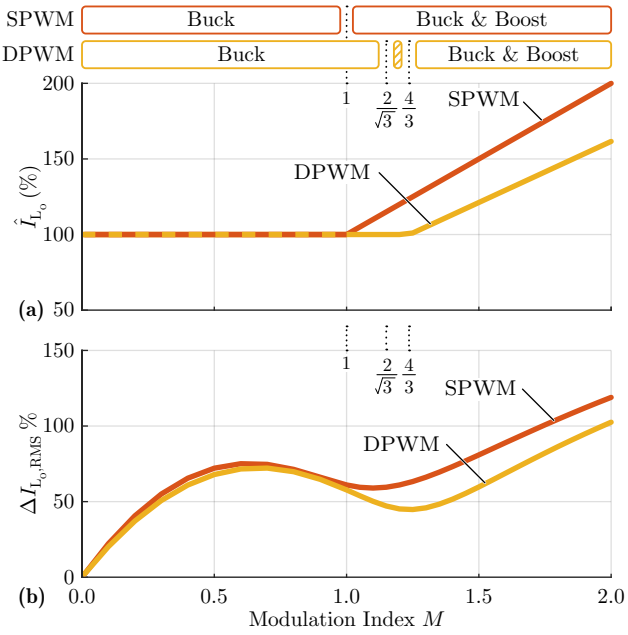

Fig. 11: Filter inductor L_o current stress, calculated for SPWM and DPWM modulation strategies. **(a)** Maximum inductor current, normalized with respect to the motor current amplitude $\hat{I}_m$ and **(b)** inductor RMS current ripple, normalized with respect to the value $\frac{U_i}{8\sqrt{3}L_o f_s}$.

is

$$\Delta i_{L_o,a,RMS}(\varphi) = \begin{cases} 4m_a(1-m_a)\dfrac{U_i}{8\sqrt{3}L_o f_s}, & 0 < \varphi \leq \varphi_o \\ 4\dfrac{m_a - 1}{m_a}\dfrac{U_i}{8\sqrt{3}L_o f_s}, & \varphi_o < \varphi \leq \pi \end{cases}, \tag{53}$$

where $m_a(\varphi)$ is the modulation factor and is given in **(8)**. The relation between the local RMS current ripple of the inductor $\Delta i_{L_o,a,RMS}$ and the modulation factor m_a is visualized in **Fig. 10**. In order to calculate the global (total) RMS current ripple, an integration of the local RMS current ripple **(53)** over the fundamental period T_m is performed. The global RMS current ripple is calculated numerically and is plotted in **Fig. 11(b)**. Finally, the filter capacitors C_o are selected. The peak voltage ripple across the filter capacitor is given in **(20)**. Accordingly, in order to limit this voltage ripple to a maximum value of ΔU_{C_o}, the capacitance value must be selected as

$$C_o \geq \max\left[\frac{U_i}{64L_o\Delta U_{C_o} f_s^2}, \frac{M\hat{I}_m}{8\Delta U_{C_o} f_s}\right]. \tag{54}$$

A voltage ripple of $\Delta U_{C_o} = \Delta U_{an} < 2\,\text{V}$ should be selected, for a safe motor operation. Finally, an RC damping circuit is placed in parallel to the filter capacitor C_o, in order to avoid unwanted resonances of the output filter [38].

B. Discontinuous Modulation (DPWM)

The component stresses are analytically derived for a modulation index range $M = 4/3...2$. For this modulation range the Y-VSI generates motor voltage amplitudes $\hat{U}_m$ greater than the input voltage U_i (buck and boost regime). For a low

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modulation index $M = 0...2/\sqrt{3}$, the Y-VSI is equivalent to a simple two-level VSI (buck regime) as shown in **Fig. 5(a)**. The component stresses for a low modulation index case are derived in **Appx. A**.

1) Semiconductor Voltage Stress: The semiconductors of the buck half-bridges $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ are blocking/switching the DC input voltage U_i independent of the employed modulation strategy

$$U_\mathrm{T1} = U_\mathrm{T2} = U_\mathrm{i}. \tag{55}$$

In contrast, the boost half-bridges $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ are blocking the time-varying inverter output voltages (e.g. $u_\mathrm{an}(\varphi)$ for half-bridge $\bar{a}_2$), which depend on the employed modulation strategy. Therefore the maximum inverter output voltage value from **Fig. 7(a)** defines the voltage stress on the boost half-bridge semiconductor devices

$$U_\mathrm{T3} = U_\mathrm{T4} = \sqrt{3}\hat{U}_\mathrm{m}. \tag{56}$$

2) Semiconductor Current Stress: The RMS current stress on the semiconductor devices is plotted in **Fig. 9** and is analytically approximated by

$$I_\mathrm{T1,RMS} = I_\mathrm{L_o,RMS}\sqrt{-\frac{\sqrt{3}}{4\pi}M^2 + \frac{5}{7}M - \frac{1}{6}}, \tag{57}$$

$$I_\mathrm{T2,RMS} = I_\mathrm{L_o,RMS}\sqrt{+\frac{\sqrt{3}}{4\pi}M^2 - \frac{5}{7}M + \frac{7}{6}}, \tag{58}$$

$$I_\mathrm{T3,RMS} = I_\mathrm{L_o,RMS}\sqrt{+\frac{1}{4\pi}M^2 - \frac{\sqrt{3}}{\sqrt{8}}M + 1 + \frac{2}{\pi}}, \tag{59}$$

$$I_\mathrm{T4,RMS} = I_\mathrm{L_o,RMS}\sqrt{-\frac{1}{4\pi}M^2 + \frac{\sqrt{3}}{\sqrt{8}}M - \frac{2}{\pi}}, \tag{60}$$

where the RMS current of the inductor $I_\mathrm{L_o,RMS}$ is given by **(30)**. As shown in **Fig. 9**, the current stress on the semiconductor devices is asymmetric and depends on the modulation index M. In the most extreme case example, for the modulation index range $M = 0...2/\sqrt{3}$, the high-side switch T_a3 conducts the total motor current, while the low-side switch T_a4 conducts no current. Therefore, the current rating of the semiconductor devices must be carefully selected in order to account for this asymmetric current stress.

3) Semiconductor Conduction Losses: The conduction losses of the Y-VSI semiconductor devices are described by **(40)** and are proportional to the square of the inductor RMS current $I_\mathrm{L_o,RMS}$. By using the expression **(30)** for the RMS inductor current, the conduction losses are calculated for DPWM

$$P_\mathrm{cd} = 6\frac{\hat{I}_\mathrm{m}^2}{2}\frac{9M^2 - 4\sqrt{3}M + 12}{16}R_\mathrm{T,on}. \tag{61}$$

4) Semiconductor Switching Losses: First, the switching losses of the buck half-bridges are calculated. The buck half-bridge $\bar{a}_1$ is switched during the buck regime of **Fig. 7**, i.e. when $u_\mathrm{an}(\varphi) \leq U_\mathrm{i}$. Thanks to DPWM, the switching transition of the buck half-bridge $\bar{a}_1$ during the buck regime are reduced compared to SWPM. More precisely, no switching transition occur during the denoted clamping region of **Fig. 7**. The commutation voltage of the buck half-bridge $\bar{a}_1$ is constant and equal to the input voltage $U_\mathrm{sw,1} = U_\mathrm{i}$. The commutation current is equal to the inductor current and hence varies over time $i_\mathrm{sw,1}(\varphi) = i_\mathrm{L_o,a}(\varphi)$. An integration of the local switching losses according to **(46)** is performed in order to derive the total switching losses caused by the buck half-bridges. The resulting sum of switching losses for the three buck half-bridges, when DPWM modulation is used, is

$$P_\mathrm{sw,1} = 3f_\mathrm{s}\left(k_0\frac{\frac{2\pi}{3} - \varphi_\mathrm{o}}{\pi} + k_1\frac{2}{\pi}\hat{I}_\mathrm{m}(\frac{4-\sqrt{3}}{4} - \frac{1}{2}\sin(\varphi_\mathrm{o}))\right), \tag{62}$$

where the sinus of the transition angle φ_o is

$$\sin(\varphi_\mathrm{o}) \overset{(24)}{=} \frac{3\sqrt{3M^2 - 4} + 2\sqrt{3}}{6M}. \tag{63}$$

The switching parameters k_0 and k_1 of **(62)** are calculated for the constant commutation voltage of the buck half-bridges $U_\mathrm{sw,1} = U_\mathrm{i}$.

Subsequently, the switching losses of the boost half-bridges are calculated. The boost half-bridge $\bar{a}_2$ is switched only during the boost regime of **Fig. 7**, i.e. when $u_\mathrm{an}(\varphi) > U_\mathrm{i}$. The commutation voltage of the boost half-bridge $\bar{a}_2$ is equal to the inverter output voltage and hence varies over time $u_\mathrm{sw,2}(\varphi) = u_\mathrm{an}(\varphi)$. The commutation current is equal to the inductor current $i_\mathrm{sw,2}(\varphi) = i_\mathrm{L_o,a}(\varphi)$ and is also time-varying. An integration of the local switching losses according to **(49)** is performed in order to derive the total switching losses caused by the boost half-bridges. The resulting sum of switching losses for the three boost half-bridges, when DPWM modulation is used, is approximated by

$$P_\mathrm{sw,2} = 3f_\mathrm{s}\left(k_0 + k_1\frac{M\sqrt{3}}{2}\hat{I}_\mathrm{m}\right)\frac{\sin(\varphi_\mathrm{o})}{\pi}, \tag{64}$$

where $\sin(\varphi_\mathrm{o})$ is given in **(63)**. The switching parameters k_0 and k_1 of **(64)** are calculated for the highest commutation voltage of the boost half-bridges $U_\mathrm{sw,2} = u_\mathrm{an}(\frac{\pi}{6}) = \sqrt{3}\hat{U}_\mathrm{m}$. The total switching losses of the Y-VSI are the sum of the respective buck half-bridges' and boost half-bridges' switching losses **(51)**. According to DPWM, the phase with the most negative motor voltage is clamped to the negative DC rail n, for one third of the fundamental period $T_\mathrm{m}/3$ (cf. **Fig. 7**). Thereby, it is possible to reduce the total switching transitions of the Y-VSI by 33% compared to SPWM. Accordingly, a significant reduction of the switching losses is achieved thanks to DPWM.

5) Passive Component Selection: The integrated output filter ($L_\mathrm{o}-C_\mathrm{o}$) of the Y-VSI is now analysed. It is assumed that a Y-VSI inverter, designed for SPWM modulation, pre-exists. In this case, the filter inductors L_o and the filter capacitors C_o are selected based on **(52)** and **(54)**, respectively. The current of the filter inductor is non-sinusoidal, as is described by **(27)** and shown in **Fig. 7(d)**. The maximum current of the inductor depends on the modulation index M, is given in **(29)** and is plotted in **Fig. 11(a)**. The DPWM results in a lower maximum

TABLE III: Component stresses summary for a Y-VSI employing SPWM or DPWM modulation strategy. The numeric values are calculated for a the motor drive of **Tab. I**, and for the nominal operating condition, i.e. modulation index $M = 4/3$.

		SPWM		**DPWM**
T_1, T_2 Voltage PK	**(34)**	$U_{\mathrm{T1}} = U_{\mathrm{T2}} = 40\,\mathrm{V}$	**(55)**	$U_{\mathrm{T1}} = U_{\mathrm{T2}} = 40\,\mathrm{V}$
T_3, T_4 Voltage PK	**(35)**	$U_{\mathrm{T3}} = U_{\mathrm{T4}} = 80\,\mathrm{V}$	**(56)**	$U_{\mathrm{T3}} = U_{\mathrm{T4}} = 69.3\,\mathrm{V}$
T_1 Current RMS	**(36)**	$I_{\mathrm{T1,RMS}} = 11.2\,\mathrm{A}$	**(57)**	$I_{\mathrm{T1,RMS}} = 10.4\,\mathrm{A}$
T_2 Current RMS	**(37)**	$I_{\mathrm{T2,RMS}} = 8.5\,\mathrm{A}$	**(58)**	$I_{\mathrm{T2,RMS}} = 9.7\,\mathrm{A}$
T_3 Current RMS	**(38)**	$I_{\mathrm{T3,RMS}} = 13.2\,\mathrm{A}$	**(59)**	$I_{\mathrm{T3,RMS}} = 14.0\,\mathrm{A}$
T_4 Current RMS	**(39)**	$I_{\mathrm{T4,RMS}} = 4.9\,\mathrm{A}$	**(60)**	$I_{\mathrm{T4,RMS}} = 2.8\,\mathrm{A}$
Conduction Losses Total	**(41)**	$P_{\mathrm{cd}} = 11.8\,\mathrm{W}$	**(61)**	$P_{\mathrm{cd}} = 9.8\,\mathrm{W}$
		$R_{\mathrm{T,on}} = 20\,\mathrm{m\Omega}$, for $100\,^{\circ}\mathrm{C}$		$R_{\mathrm{T,on}} = 20\,\mathrm{m\Omega}$, for $100\,^{\circ}\mathrm{C}$
Switching Losses Buck	**(47)**	$P_{\mathrm{sw},1} = 7.7\,\mathrm{W}$	**(62)**	$P_{\mathrm{sw},1} = 2.9\,\mathrm{W}$
		$^{*}k_0 = 6.77\,\mu\mathrm{J}$, $k_1 = 0.68\,\mu\mathrm{J/A}$, for U_{T1}		$^{*}k_0 = 6.77\,\mu\mathrm{J}$, $k_1 = 0.68\,\mu\mathrm{J/A}$, for U_{T1}
Switching Losses Boost	**(50)**	$P_{\mathrm{sw},2} = 8.7\,\mathrm{W}$	**(64)**	$P_{\mathrm{sw},2} = 6.2\,\mathrm{W}$
		$^{*}k_0 = 10.91\,\mu\mathrm{J}$, $k_1 = 1.09\,\mu\mathrm{J/A}$, for U_{T3}		$^{*}k_0 = 8.58\,\mu\mathrm{J}$, $k_1 = 0.86\,\mu\mathrm{J/A}$, for U_{T3}
Losses Total		$P_{\mathrm{cd}} + P_{\mathrm{sw},1} + P_{\mathrm{sw},2} = 28.3\,\mathrm{W}$		$P_{\mathrm{cd}} + P_{\mathrm{sw},1} + P_{\mathrm{sw},2} = 18.9\,\mathrm{W}$
Efficiency Reduction		$\Delta\eta = -2.8\%$		$\Delta\eta = -1.9\%$
Filter Inductor	**(52)**	$L_{\mathrm{o}} = 5\,\mu\mathrm{H}$	**(52)**	$L_{\mathrm{o}} = 5\,\mu\mathrm{H}$
Current Ripple PK		$\Delta I_{\mathrm{L_o}} = 3.6\,\mathrm{A}$		$\Delta I_{\mathrm{L_o}} = 3.6\,\mathrm{A}$
Current PK	**(16)**	$\hat{I}_{\mathrm{L_o}} = 22.2\,\mathrm{A}$	**(29)**	$\hat{I}_{\mathrm{L_o}} = 19.3\,\mathrm{A}$
Current RMS	**(18)**	$I_{\mathrm{L_o,RMS}} = 13.3\,\mathrm{A}$	**(30)**	$I_{\mathrm{L_o,RMS}} = 12.8\,\mathrm{A}$
Filter Capacitor	**(54)**	$C_{\mathrm{o}} = 2\,\mu\mathrm{F}$	**(54)**	$C_{\mathrm{o}} = 2\,\mu\mathrm{F}$
Voltage Ripple PK		$\Delta U_{\mathrm{C_o}} = 0.7\,\mathrm{V}$		$\Delta U_{\mathrm{C_o}} = 0.7\,\mathrm{V}$

*Switching parameters k_0 and k_1 are calculated based on [53].

current and hence a lower stress on the inductor, compared to SPWM. Subsequently, the RMS current ripple of the inductor $\Delta I_{\mathrm{L_o,RMS}}$, which is directly related to the inductor losses, is calculated. In order to calculate the global (total) RMS current ripple, an integration of the local RMS current ripple **(53)** over the fundamental period T_{m} is performed. The global RMS current ripple is calculated numerically and is plotted in **Fig. 11(b)**. It is deduced that DPWM causes less current ripple stress on the filter inductor compared to SPWM.

C. Remaining Component Stresses

The capacitor C_{i} conducts the switched input current $i_{\mathrm{i}}(t)$ of the Y-VSI. The worst case current, flowing through the input capacitor over a switching period T_{s} is $i_{\mathrm{i}}(t) = \frac{1}{2}\hat{I}_{\mathrm{o}}\mathrm{rec}(2\pi f_{\mathrm{s}} t)$ The input capacitor current is in this case rectangular, with 50% duty cycle and has an amplitude of $\hat{I}_{\mathrm{o}}/2$. Accordingly, a high (local) RMS current stress on the input capacitor $I_{C_{\mathrm{i}},\mathrm{RMS}} = \hat{I}_{\mathrm{o}}/2$ results. Based on the rectangular current waveform $i_{\mathrm{i}}(t) = \frac{1}{2}\hat{I}_{\mathrm{o}}\mathrm{rec}(2\pi f_{\mathrm{s}} t)$, the worst case voltage ripple across the input capacitor C_{i} and/or the fuel-cell is

$$\Delta U_{\mathrm{i}} = \frac{\hat{I}_{\mathrm{m}}}{8 f_{\mathrm{s}} C_{\mathrm{i}}}. \tag{65}$$

Therefore, in order to limit the input voltage ripple to a sufficiently low value ΔU_{i} the input capacitance must be

$$C_{\mathrm{i}} \geq \frac{\hat{I}_{\mathrm{m}}}{8 f_{\mathrm{s}} \Delta U_{\mathrm{i}}}. \tag{66}$$

The resulting input capacitance value C_{i} is inversely proportional to the switching frequency f_{s} and is typically small. It is noted here, that there is no need for low-frequency energy storage within the input capacitor C_{i}, for a balanced three-phase system. In summary, the input capacitor must conduct a high-frequency switched current with a high RMS value $I_{C_{\mathrm{i}},\mathrm{RMS}}$, while a low capacitance C_{i} is typically required. Therefore, ceramic or film capacitors are suggested for the C_{i} realization.

IV. Experimental Validation

The proposed Y-VSI inverter concept is tested within the fuel-cell application of **Fig. 1** and **Tab. I**. A $10\,\mathrm{kW}$ fuel-cell unit requires a continuous supply of oxygen, which is provided by a $280\,\mathrm{krpm}$ high-speed electric compressor [5]. A motor drive system, directly supplied by the fuel-cell controls the electric compressor. The compressor drive system uses 10% of the fuel-cell power, i.e. $1\,\mathrm{kW}$.

A. Design Procedure

The previously derived component stresses in **Sec. III** depend on the switching frequency f_{s}, however the switching frequency is until now not explicitly defined. The switching frequency f_{s} represents a crucial design trade-off. A high switching frequency allows to reduce the volume of the passive filter components, but at the same time increases the semiconductor switching losses and accordingly requires a larger semiconductor heatsink volume. In order to select an appropriate switching frequency, a multi-objective optimization routine, with respect to inverter efficiency η and power density ρ, is employed [55]–[57], which assesses the performance of several Y-VSI inverter designs. The optimization routine includes the $200\,\mathrm{V}$ rated GaN semiconductor devices (EPC 2034 MOSFETs [53]), the semiconductor heatsinks [58], the inductive components L_{o}, [54], [59] and the ceramic capacitors $C_{\mathrm{o}}, C_{\mathrm{i}}$.

Based on the optimization results, a switching frequency of $f_{\mathrm{s}} = 300\,\mathrm{kHz}$ is selected for the Y-VSI. The boxed volume of the integrated AC filter (L_{o} and C_{o}) is $36.4\,\mathrm{cm}^3$. Subsequently, the number of parallel semiconductor devices per switch ($T_{\mathrm{a1}} - T_{\mathrm{a4}}$ of **Fig. 3**) is selected. A low number of parallel devices yields low (capacitive) switching losses, but high

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conduction losses. On the contrary, a high number of parallel devices results in high switching losses but low conduction losses. The number of parallel devices is determined by the minimum of the overall semiconductor losses (i.e. sum of conduction and switching losses). In the case at hand, two parallel devices per switch are optimal. A breakdown of the semiconductor losses into conduction and switching losses is depicted in **Fig. 12**. As expected, DPWM modulation yields lower semiconductor losses (-33.2%) compared to SPMW modulation, mainly thanks to the reduced number of switching transitions. The Y-VSI component parameters are given in **Tab. IV**.

Using the analytic formulas derived in **Sec. III**, the inverter component stresses are calculated and summarized in **Tab. III**. There, the SPWM and DPWM modulation strategies are compared. The **Tab. III** serves as a general design guideline and can be extended for motor drive systems with different specifications. After the designer selects an appropriate switching frequency f_s, based on the available semiconductor technology, **Tab. III** can be easily used in order to design a Y-VSI inverter.

For the sake of completeness, a conventional B-VSI (cf. **Fig. 2**) is designed for the specifications of **Tab. I**. The detailed design process of a B-VSI can be found in [21]. The selected B-VSI benchmark design, features the same switching frequency of $f_\mathrm{s} = 300\,\mathrm{kHz}$, for both the DC/DC stage as well as the DC/AC stage. The boxed volume of the DC/DC stage filter ($L_\mathrm{i}, C_\mathrm{i}$ and C_DC) is $10.7\,\mathrm{cm}^3$, while the boxed volume of the DC/AC stage filter (L_o and C_o) is $32\,\mathrm{cm}^3$. Therefore, the total filter volume of the B-VSI is $42.7\,\mathrm{cm}^3$. Note that the filter volume of the B-VSI ($42.7\,\mathrm{cm}^3$) is higher than the respective volume for the Y-VSI ($36.4\,\mathrm{cm}^3$), due to the higher number of four inductors. In addition, the same $200\,\mathrm{V}$ rated GaN devices are used, as in the case of the Y-VSI. In particular, two parallel devices per switch are used for the DC/DC stage and one device per switch is used in the DC/AC stage. The semiconductor losses of the conventional B-VSI [21], are depicted in **Fig. 12**. The selected number of parallel devices yields the lowest overall semiconductor losses. Note in **Fig. 12(a)** that the DC/AC stage switching losses ($15.5\,\mathrm{W}$) are higher than the DC/AC stage conduction losses ($8.3\,\mathrm{W}$). Therefore, using two instead of one parallel device per switch for the DC/AC stage would further increase the switching losses. The increase in the switching losses would outweigh the decrease in the conduction losses, thereby resulting in higher overall semiconductor losses. Thus, one device per switch is optimal. The B-VSI component parameters are summarized in **Tab. V**.

Fig. 12(a) reveals that the Y-VSI employing SPWM generates 20.1% less semiconductor losses, compared to the B-VSI employing SWPM, for the same switching frequency of $f_\mathrm{s} = 300\,\mathrm{kHz}$. The superior performance of the Y-VSI can be explained as follows. The B-VSI features two energy conversion stages. In the case of SPWM, one half-bridge is switched at the DC/DC stage and three half-bridges are switched at the DC/AC stage. Therefore, four in total half-bridges are switched. In addition, all the half-bridges switch

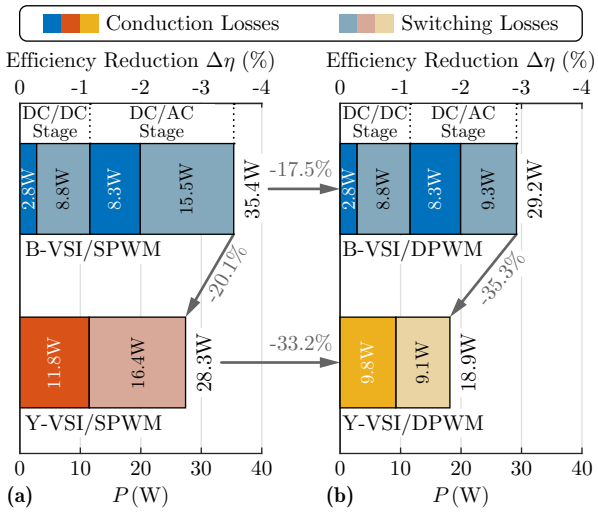

Fig. 12: Breakdown of the semiconductor losses of the Y-VSI and the B-VSI [21] into conduction and switching losses, for **(a)** SPWM and **(b)** DPWM. The numeric values are calculated for the nominal specifications of **Tab. I**, i.e. modulation index $M = 4/3$.

the high DC link voltage $U_\mathrm{DC} = 80\,\mathrm{V}$. The Y-VSI processes the transmitted power $P = 1\,\mathrm{kW}$ in a completely differently way. When SPWM is employed, only one half-bridge per phase-module is switched, at any given point in time (cf. **Fig. 6**). Therefore, a Y-VSI requires the switching of only three half-bridges in total, at any given point in time. Furthermore, the buck half-bridge $\bar{a}_1$ of the Y-VSI switches the low input voltage $U_\mathrm{i} = 60\,\mathrm{V}$, while the boost half-bridge $\bar{a}_2$ switches the time-varying output voltage $u_\mathrm{an}(t) \leq 80\,\mathrm{V}$ **(6)**. Note that both these voltages are lower than the high DC link voltage $U_\mathrm{DC} = 80\,\mathrm{V}$ of a B-VSI. For the above reasons the Y-VSI benefits from low semiconductor losses. It is noted, that the semiconductor losses reduction achieved by means of the Y-VSI, simultaneously enables a low semiconductor heatsink volume [58].

A similar analysis is performed for DPWM modulation in **Fig. 12(b)**. There, the Y-VSI generates 35.3% less semiconductor losses than the B-VSI, which can be explained as follows. According to DPWM, only two half-bridges of the Y-VSI are switched at any given point in time (cf. **Fig. 7**). Contrary, three half-bridges in total (one half-bridge at the DC/DC stage and two half-bridges at the DC/AC stage) are switched, in the case of the B-VSI. Therefore, the B-VSI generates considerably higher semiconductor losses than the Y-VSI.

B. Experimental Results

Two inverter hardware prototypes are purposely assembled: **(i)** Y-VSI of **Fig. 3**. The hardware prototype is shown in **Fig. 13** and the respective component parameters are given in **Tab. IV**. Experimentally measured waveforms for SWPM are shown in **Fig. 14(a)**, where the three output voltages of the inverter are offseted sinusoids. Experimentally measured waveforms for DWPM are shown in **Fig. 14(b)**. There, the three output voltages of the inverter are non-sinusoidal, however, the load line-to-line voltages are sinusoidal.

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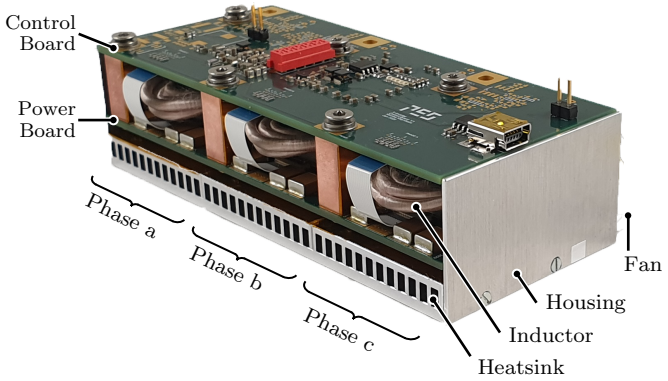

Fig. 13: Y-VSI hardware prototype (113 mm × 49 mm × 30 mm) achieving a power density of 6.6 kW/dm^3 (108 W/in^3).

TABLE IV: Parameter values of the Y-VSI hardware prototype, corresponding to the schematic diagram notation of **Fig. 3**.

Y-VSI	
Switching frequency f_s	300 kHz
Switches (2 devices parallel)	200 V EPC 2034
Inductance L_o	5 µH
Capacitance C_o	2 µF
Capacitance C_i	10 µF

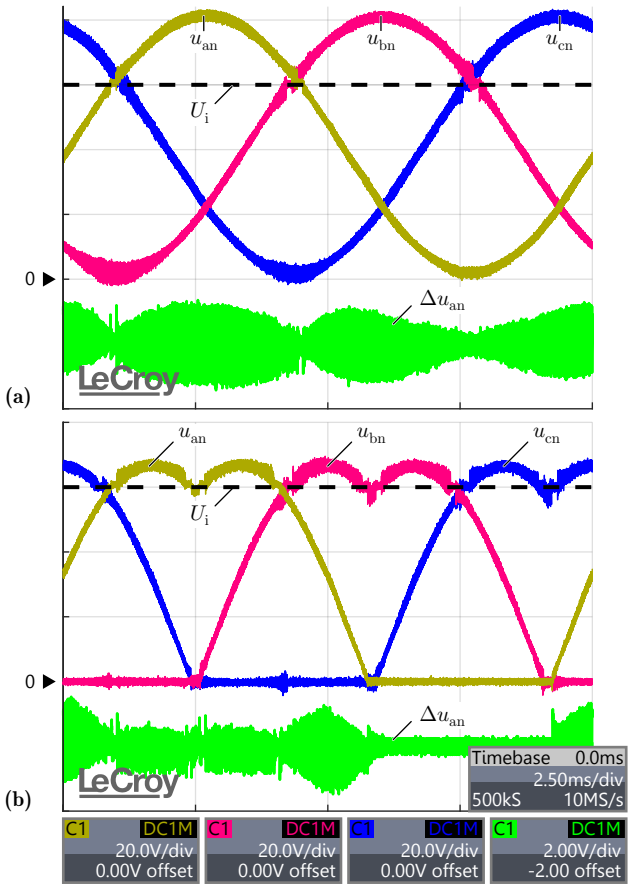

Fig. 14: Experimentally measured waveforms for the Y-VSI inverter employing **(a)** SPWM and **(b)** DPWM modulation, at nominal operating condition $P = 1$ kW. (yellow) Phase a, (red) phase b and (blue) phase c output voltages. (green) Phase a output voltage ripple.

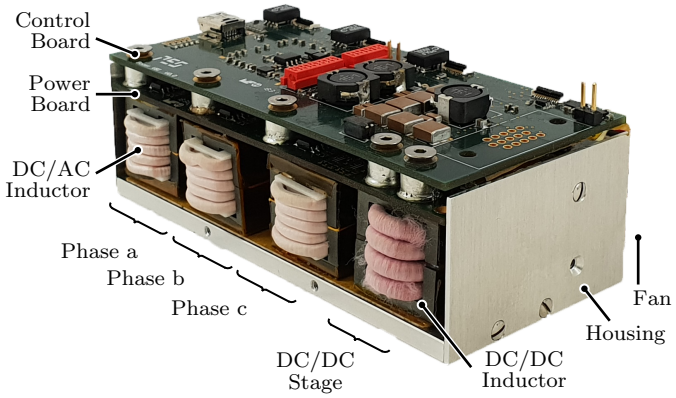

Fig. 15: B-VSI hardware prototype (106 mm × 50 mm × 35 mm) achieving a power density of 6 kW/dm^3 (98 W/in^3).

TABLE V: Parameter values of the B-VSI hardware prototype, corresponding to the schematic diagram notation of **Fig. 2**.

B-VSI - DC/DC stage	
Switching frequency $f_{s,i}$	300 kHz
Switches (2 devices parallel)	200 V EPC 2034
Inductance L_i	1.5 µH
Capacitance C_i	10 µF
Capacitance C_{DC}	25 µF
B-VSI - DC/AC stage	
Switching frequency $f_{s,o}$	300 kHz
Switches (1 device)	200 V EPC 2034
Inductance L_o	5 µH
Capacitance C_o	2 µF

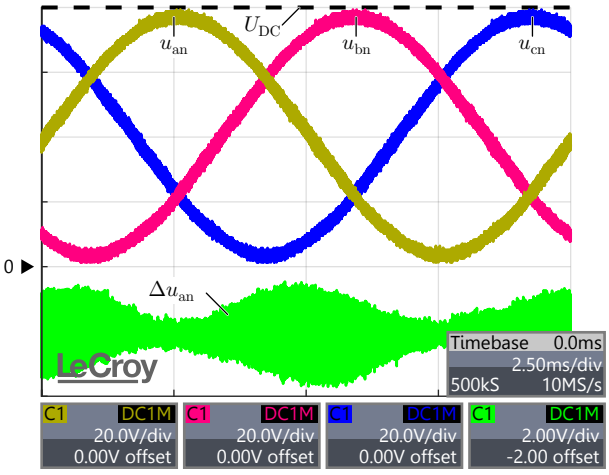

Fig. 16: Experimentally measured waveforms for the B-VSI inverter at nominal operating condition $P = 1$ kW. (yellow) Phase a, (red) phase b and (blue) phase c output voltages. (green) Phase a output voltage ripple.

(ii) B-VSI of **Fig. 2**. The hardware prototype is depicted in **Fig. 15**, while the component parameters are summarized in **Tab. V**. Experimentally measured waveforms are shown in **Fig. 16** for SWPM modulation. This hardware prototype serves as the state-of-the-art solution against which the Y-VSI hardware prototype is compared to.

In order to enable a meaningful comparison, both the above

hardware demonstrators feature the same switching frequency of $f_s = 300\,\text{kHz}$. It is noted, that during the experimental measurements the compressor is replaced by an equivalent resistive load $R = 2\,\Omega$. The resistive load significantly simplifies the test setup, but does not affect the operation or the performance of the inverter prototypes.

First, the performance of the two hardware prototypes is experimentally compared. The conventional B-VSI hardware prototype achieves a power density of $\rho = 6\,\text{kW/dm}^3$ (including case, cooling system and control electronics). The Y-VSI hardware prototype achieves a power density of $\rho = 6.6\,\text{kW/dm}^3$, which is $\Delta\rho = +10\%$ higher compared to the B-VSI. The Y-VSI benefits from a lower number of inductive components (three) compared the B-VSI (four). This is the main reason behind the higher Y-VSI power density.

At $P = 1\,\text{kW}$ nominal operation, the B-VSI achieves a low efficiency of $\eta = 96\%$ (i.e. $40\,\text{W}$ of losses), for sinusoidal modulation strategy (SWPM). The majority of the losses originate from the semiconductor devices (i.e. $35.4\,\text{W}$ calculated in **Fig. 12(a)**). As discussed in **Sec. IV-A**, there are two main reasons behind the B-VSI low efficiency. The B-VSI is a two-stage converter, as a result four half-bridges are switched at any given point in time (for SPWM). Furthermore, all the semiconductor devices process/switch the high DC link voltage $U_{\text{DC}} = 80\,\text{V}$.

By employing the SPWM of **Fig. 6**, the Y-VSI achieves a nominal efficiency of $\eta = 97.2\%$ (i.e. $28\,\text{W}$ of losses), which is $\Delta\eta = +1.2\%$ more efficient compared to the B-VSI (also employing SPWM). The Y-VSI delivers power to the motor more efficiently than the B-VSI, as discussed in **Sec. IV-A**. That is, at any moment in time, only three out of the six half-bridges of the Y-VSI are operated with the switching frequency f_s, while the remaining three half-bridges are clamped. By employing the discontinuous modulation strategy (DPWM) of **Fig. 7**, the Y-VSI achieves an even higher efficiency of $\eta = 98.3\%$ (i.e. $17\,\text{W}$ of losses). The Y-VSI is in this case $\Delta\eta = +2.3\%$ more efficient than the B-VSI, employing SPWM. The DPWM further reduces the number of switching transitions, thus adds to the previously described advantages of the Y-VSI. At each moment in time, only two out of the six half-bridges are operated with the switching frequency f_s, while the remaining four half-bridges are clamped. The efficiency curves of the two inverter prototypes are plotted in **Fig. 17**.

Finally, the motor voltage quality is assessed. The voltage ripple Δu_{an} at the load terminal a is measured in **Fig. 16**, for the case of the B-VSI employing SPWM. The voltage ripple Δu_{an} is the result of the PWM operation of the half-bridge $\bar{a}$. In particular, the switch-node $\bar{a}$ two-level PWM voltage acquires two voltage values $u_{\bar{a}\text{n}} = \{0\,\text{V}, 80\,\text{V}\}$, and is processed by the full sin-wave output filter ($L_o = 5\,\mu\text{H}, C_o = 2\,\mu\text{F}$). Thanks to the DM/CM attenuation of the output filter (-31dB at the frequency $f_s = 300\,\text{kHz}$), a worst case voltage ripple value of $\Delta U_{\text{an}} = 1.4\,\text{V}$ appears at the load terminal a. This voltage ripple value is low, hence ensures a safe motor operation.

The voltage ripple Δu_{an} of the load terminal a is also measured for the Y-VSI in **Fig. 14**. The voltage ripple Δu_{an}, is caused by the PWM operation of the half-bridges $\bar{a}_1$ and $\bar{a}_2$. Thanks to the integrated AC filter of the Y-VSI, the voltage ripple is $\Delta U_{\text{an}} < 1\,\text{V}$ (for either SPWM or DPWM). The Y-VSI benefits from a slightly better motor voltage quality than the B-VSI, for the system specifications at hand (i.e. modulation index $M = 4/3$). It is reminded that the B-VSI and Y-VSI employ the same AC filter component values, i.e. $L_o = 5\,\mu\text{H}, C_o = 2\,\mu\text{F}$. By comparing the voltage ripple generated by SPWM and DPWM modulation (cf. **Fig. 14**), it is evident that the latter DPWM results in an overall lower voltage ripple Δu_{an}. This is expected, since DPWM reduces the total number of switching transitions, which cause the voltage ripple in the first place.

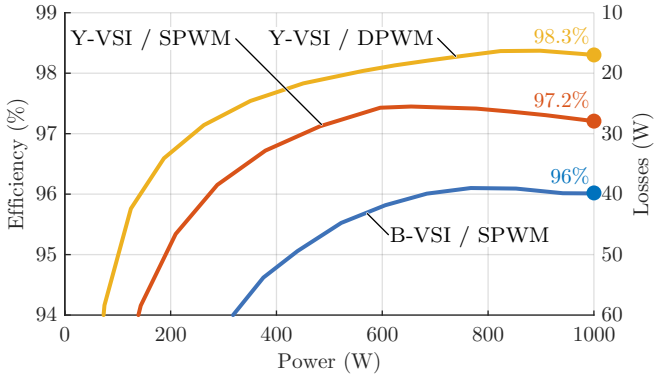

Fig. 17: Efficiency profile of (blue) conventional B-VSI employing SPWM, (orange) Y-VSI employing SPWM and (yellow) Y-VSI employing DPWM. The Yokogawa WT3000E high accuracy power analyzer is used for the efficiency measurements.

V. Conclusions

Motor drive systems supplied by a fuel-cell/battery are especially demanding when it comes to the design of the inverter. Besides a high performance (high efficiency η and power density ρ), the inverter has to cope with the wide DC voltage variation of the fuel-cell/battery. Therefore, buck-boost inverter topologies are required, which can guarantee the nominal speed/voltage range of the motor independent of the DC input voltage fluctuation.

A promising buck-boost inverter topology, denoted as Y-VSI, is presented within this paper (cf. **Fig. 3**). The Y-VSI is based on a three-phase modular concept, where three identical phase-modules are connected to a common star "Y" point (cf. **Fig. 4**). The Y-VSI benefits from four key advantages:

(i) Buck-boost capability. Each phase-module comprises a buck-boost DC/DC converter, hence the Y-VSI can generate output AC voltages that are higher or lower than the input DC voltage.

(ii) High efficiency. The Y-VSI processes the transmitted power P in a unique way. In the typical case, only three out of the six half-bridges are switched, at any given point in time. As a result, low switching losses are generated, hence high inverter efficiency is achieved. Based on the low number of switched half-bridges, the Y-VSI can be considered as a single-stage inverter.

(iii) Integrated AC output filter. The Y-VSI comprises an integrated output filter, hence generates sinusoidal motor voltages/currents. Furthermore, the Y-VSI protects the motor from high $\mathrm{d}u/\mathrm{d}t$, thus the long-term reliability of the motor is guaranteed. As a result, no additional filter is required between the inverter and the motor.
(iv) Straightforward control. Each phase-module is equivalent to a DC/DC converter, hence can be controlled independently, based on well established control concepts. As a result, the Y-VSI benefits from a simple and uncomplicated control system (cf. **Fig. 8**).

Two modulation strategies are comparatively evaluated for the Y-VSI:
(i) Sinusoidal modulation (SPWM) of **Fig. 6**, which features sinusoidal output voltages.
(ii) Discontinuous modulation (DPWM) of **Fig. 7**. There, each output voltages is non-sinusoidal, however the difference between two output voltages, which is equal to the motor line-to-line voltage, is sinusoidal. By means of DPWM, it is possible to reduce the switching transition of the Y-VSI by 33%, and hence significantly reduce the overall switching losses.
The stresses on the inverter components are analytically derived for both modulation strategies, and a summary is given in **Tab. III**. A comparison of the two modulation strategies reveals that the latter DPWM yields higher efficiency than the former SPWM.

The Y-VSI performance is validated within the context of the application of **Fig. 1** and **Tab. I**. In the application at hand, a motor drive system is supplied by a fuel-cell and controls a high-speed $280\,\mathrm{krpm}\,1\,\mathrm{kW}$ electric compressor. The Y-VSI hardware prototype of **Fig. 13**, which achieves a power density of $\rho = 6.6\,\mathrm{kW/dm^3}$ and an efficiency of $\eta = 98.3\%$, is purposely assembled. The hardware prototype employs the latest generation of GaN semiconductor devices and features a switching frequency of $f_\mathrm{s} = 300\,\mathrm{kHz}$. Finally, the Y-VSI is compared to the state-of-the-art inverter topology of **Fig. 2**, which features two energy conversion stages. The Y-VSI outperforms the state-of-the-art hardware prototype of **Fig. 15**, by $\Delta\eta = +2.3\%$ in terms of efficiency and by $\Delta\rho = +10\%$ in terms of power density.

In summary, the Y-VSI is a promising technology for modern variable speed motor drives. The integrated output filter of the Y-VSI allows for the safe use of WBG semiconductor devices. The high $\mathrm{d}u/\mathrm{d}t$ of WBG devices is effectively suppressed by the integrated filter, hence the motor reliability is ensured. Therefore, the Y-VSI fits well with applications, where high performance, sinusoidal motor voltages/currents and wide voltage operating range are of high importance.

APPENDIX A
COMPONENT STRESSES FOR LOW MODULATION INDEXES

A. Sinusoidal Modulation (SPWM)

For the sake of completeness, the component stresses of the Y-VSI are derived for a low modulation index $M = 0...1$. For SPWM within this modulation index range, the Y-VSI continuously operates in buck regime, according to **Fig. 5(a)**. There, the boost half-bridges e.g. $\bar{a}_2$ are clamped, while only the buck half-bridges e.g. $\bar{a}_1$ are switched. In this case, the Y-VSI is equivalent to a simple two-level VSI. The RMS current stress on the semiconductor devices is

$$\begin{aligned} I_{\mathrm{T1,RMS}} &= \frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\sqrt{\frac{M}{2}}, \quad I_{\mathrm{T2,RMS}} = \frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\sqrt{1-\frac{M}{2}}, \\ I_{\mathrm{T3,RMS}} &= \frac{\hat{I}_\mathrm{m}}{\sqrt{2}}, \qquad\qquad I_{\mathrm{T4,RMS}} = 0, \end{aligned} \tag{67}$$

and is plotted in **Fig. 9**.

The conduction losses of the Y-VSI semiconductor devices are described by **(40)** and are proportional to the square of the inductor RMS current $I_{\mathrm{L_o,RMS}}$. For the examined modulation range $M = 0...1$, the filter inductor current is equal to the motor current and hence

$$I_{\mathrm{L_o,RMS}} = \frac{\hat{I}_\mathrm{m}}{\sqrt{2}}. \tag{68}$$

The resulting conduction losses are

$$P_\mathrm{cd} = 6\frac{\hat{I}_\mathrm{m}^2}{2}R_\mathrm{T,on}. \tag{69}$$

The switching losses are subsequently analysed. The boost half-ridges are clamped and therefore exhibit no switching losses, i.e. $P_{\mathrm{sw,2}} = 0$. Therefore, only the buck half-bridges contribute to the switching losses. The equation **(46)** is used in order to derive the total switching losses caused by the buck half-bridges

$$P_\mathrm{sw} = P_{\mathrm{sw,1}} = 3f_\mathrm{s}(k_0 + k_1\frac{2}{\pi}\hat{I}_\mathrm{m}), \tag{70}$$

where the switching parameters k_0 and k_1 are calculated for the constant commutation voltage of $U_{\mathrm{sw,1}} = U_\mathrm{i}$.

B. Discontinuous Modulation (DPWM)

The component stresses of the Y-VSI are derived for DPWM and a low modulation index $M = 0...2/\sqrt{3}$. For DPWM within this modulation index range, the Y-VSI continuously operates in buck regime, according to **Fig. 5(a)**. The RMS current stress on the semiconductor devices is

$$\begin{aligned} I_{\mathrm{T1,RMS}} &= \frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\sqrt{\frac{3\sqrt{3}M}{4\pi}} \quad I_{\mathrm{T2,RMS}} = \frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\sqrt{1-\frac{3\sqrt{3}M}{4\pi}} \\ I_{\mathrm{T3,RMS}} &= \frac{\hat{I}_\mathrm{m}}{\sqrt{2}} \qquad\qquad I_{\mathrm{T4,RMS}} = 0 \end{aligned} \tag{71}$$

The conduction losses of DPWM are the same as in the case of SWPM **(69)**. The switching losses are subsequently analysed. Similarly to SPWM, the boost half-ridges are clamped and therefore exhibit no switching losses, i.e. $P_{\mathrm{sw,2}} = 0$. Only the buck half-bridges contribute to the switching losses. The equation **(46)** is used in order to derive the total switching

losses caused by the buck half-bridges

$$P_{\mathrm{sw}} = P_{\mathrm{sw},1} = 3f_{\mathrm{s}}(\frac{2}{3}k_0 + (1 - \frac{\sqrt{3}}{4})k_1\frac{2}{\pi}\hat{I}_{\mathrm{m}}), \qquad (72)$$

where the switching parameters k_0 and k_1 are calculated for the constant commutation voltage of $U_{\mathrm{sw},1} = U_{\mathrm{i}}$.

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