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Protection of MV/LV Solid-State Transformers in the Distribution Grid

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***Abstract*—Solid-State Transformers (SSTs) are a promising technology since they combine a high efficiency with the integration of new functionalities and services in the grid. A SST establishes the interface between a MV AC three-phase grid and a LV AC or DC grid. For this reason a SST is subject to electrical stresses due to faults occurring in the grid. The MV and LV grids are in return exposed to failures of the SSTs. Therefore, a suitable design of the SST and its corresponding protection devices has to be found. This paper identifies the different stresses which are relevant for a SST, analyzes the protection mechanisms which are currently used for low-frequency transformers and proposes adapted protection schemes for SSTs. MV short circuits and overvoltages are identified as the most critical stresses and are analyzed in detail. Finally, some guidelines are extracted for designing a robust SST.**

***Index Terms*—Solid-State Transformer, Power-Electronic Transformer, Distribution Transformer, Medium Voltage, Protection, Overvoltage, Overcurrent, Short Circuit, Earthing.**

I. Introduction

Today, the interfacing between the different voltage levels in the grid is done with *Low-Frequency Transformers* (LFTs). The need to integrate renewable energy sources into LV AC or DC grids and the progress of the semiconductor technology has led to the idea of *Solid-State Transformers* (SSTs) where the power conversion is realized with a medium-frequency link [1]–[3]. SSTs are aimed to interface the MV AC grid ($6-36\,\mathrm{kV}$) with LV AC or DC grids ($50-400\,\mathrm{V}$). SSTs achieve a high efficiency conversion from AC to DC [4], [5] while allowing power flow control, active filtering, reactive power compensation, etc. [3].

Different topologies are suitable for SSTs featuring unidirectional or bidirectional energy conversion, using single or multi-cell converter types. The topologies of SSTs [1], [5], [6], the suitable components [7]–[9], and the operation in a grid [10]–[13] have already been examined in detail in the literature while the interface between SSTs and grids remains a widely open topic.

In **Fig. 1**, a common SST converter structure is shown where three single-phase MV voltage source inverters are employed [4]–[6]. The position of the protection and grid coupling devices for the MV and LV grids are also shown. Different kinds of grid integrations are feasible for such SSTs:

- The SST is used as a replacement for a LFT in a traditional distribution grid. In this case, the power flow is mainly directed from MV to LV and no monitoring or control of the loads is possible [4].
- The SST forms the interface between the MV grid and a smart grid with renewable energy production and control capabilities [3].
- An industrial grid where the SST is used as a unidirectional power supply connected to the MV grid (information processing systems, drive systems, power-to-gas, etc.) [14].
- The SST is used as a part of a traction power supply chain in order to replace LFTs [9], [15]. In this case, the SST does not form the interface between two grids and is not considered further in this paper.

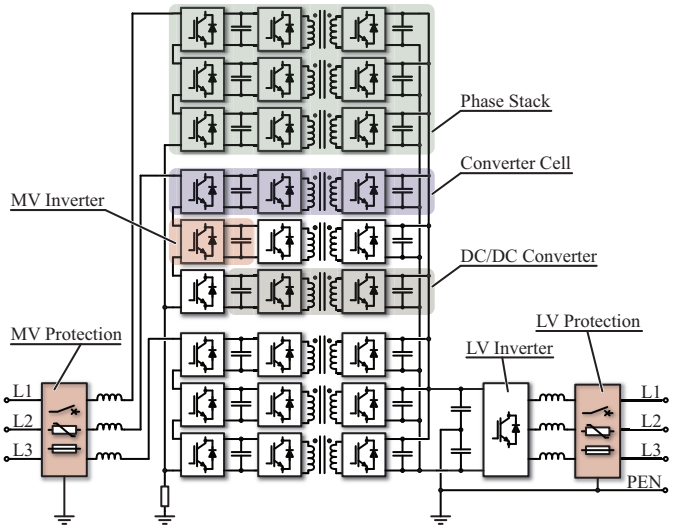

Fig. 1. Three-phase AC/AC SST according to [4], [6] with the protection devices. The AC/DC MV inverters of the SST are composed of stacked single-phase inverters and are coupled together via DC/DC converters. A three-phase LV inverter with a neutral conductor is used.

Out of these options, the usage of the SST in a traditional distribution grid leads to the largest stresses due to the lack of monitoring or control capabilities. For this reason, this case will be further considered. Still, the presented results can easily be adapted to the other usages.

In order to describe the stresses in more detail, a typical MV/LV grid is shown in **Fig. 2** where the lines, transformers, and loads are shown. The most important faults occurring for LFTs/SSTs can be classified as follows:

1) *Internal Fault:* A fault inside the transformer can produce an important stress for the grid due to the resulting short or open circuit [16], [17].
2) *Lightning Surge:* Direct or indirect atmospheric discharges are quite frequent in MV grids and cause massive overvoltages [17]–[20].
3) *Switching Transient:* Switching transients (overvoltages and overcurrents) occur when a fault is cleared or, more commonly, when a switch is opened or closed for a grid topology reconfiguration [18], [21].
4) *MV Short Circuit:* In a three-phase grid, different types of short circuits are possible producing overvoltage transients and overcurrent stresses [16], [17], [22], [23].
5) *LV Short Circuit:* The implications of LV and MV short circuits on the distribution transformer are similar. The main difference is that the LV grids have a neutral conductor, which provides a solid grounding [16], [17], [24].

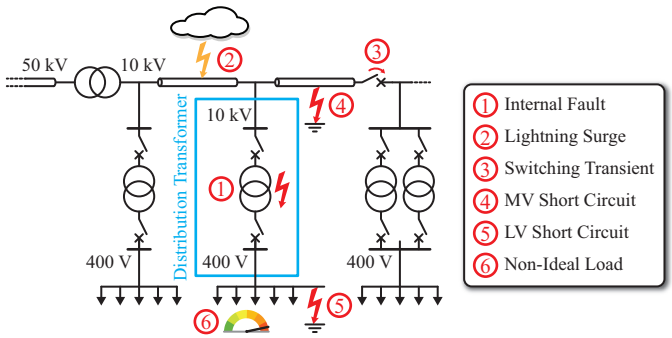

Fig. 2. Typical three-phase MV/LV distribution grid topology (bus arrangement) with three MV/LV substations. The HV, MV, and LV lines are shown as well as the LV loads. The encircled numbers list the faults that are relevant for the highlighted distribution transformer.

6) *Non-Ideal Load:* In addition to the above mentioned faults, non-ideal loads, e.g. overload, load step, asymmetric load, load with THD, etc., can also represent a relevant stress component for the distribution transformer [16], [17], [24].

Most of the above-mentioned faults are only acceptable during short time intervals without leading to a partial black out of the grid and the destruction of some devices. The grid is thus a hostile environment for a transformer and, in this context, LFTs are much more robust than SSTs, which are composed of filters, power electronic devices, capacitors, sensors, control units, etc. For this reason, this paper examines in detail the protection of SSTs operated between MV and LV grids. The paper is organized as follows. In Section II, the general protection requirements are analyzed and the protection scheme of LFTs is reviewed. In Section III, this scheme is adapted for SSTs and the impact of short circuits and overvoltages is examined in more detail. Finally, Section IV, presents some guidelines for designing robust SSTs.

II. Protection Requirements & LFTs

A. Protection Requirements

The role of the protection system of the distribution transformer is to protect the transformer from a grid fault, the grid from a transformer fault, the MV grid against the LV grid, the LV grid against the MV grid, and the transformer against internal faults. The stresses applied to the transformer can be divided into two main categories: *overcurrents* and *overvoltages*.

The magnitudes of the overcurrents depend on the impedances of the grid components and of the fault type (line-to-earth fault, line-to-line fault, overload, etc.). Since most short circuits are not self-extinguishing, the protection devices must be able to interrupt the short circuit currents in case of a grid fault or to isolate the transformer after an internal fault.

In order to achieve a reliable overcurrent protection, the following concepts are required for the design of the protection system: *selectivity*, *sensitivity*, *speed*, *safety*, and *reliability* [16], [17], [24].

The most important concept for achieving a reliable protection is selectivity as it minimizes or suppresses any implications of the faults on the final customers [17], [24]. The idea is that the downstream protection devices (towards LV, low power) are most sensitive and therefore the first to trip during an overcurrent situation.

The *current selectivity* defines lower fault current limits near the end customers. The *time selectivity* adds delays for tripping the protection devices in the direction of the MV/HV grids. These time delays also help to identify the fault and to avoid false alarms (nuisance tripping). Finally, the *logic selectivity* is based on

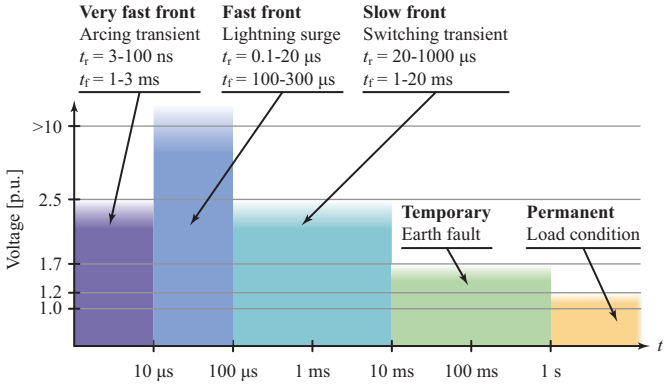

Fig. 3. Time-voltage characteristics for MV grid overvoltages (normalized with respect to the nominal system voltage according to [27]). The times t_r and t_f represent rise and fall times of the surges (usually specified by double exponential shapes). The given levels are only typical values which can vary for different grids [17], [18], [26], [28].

communication between the different protection devices in order to localize and identify the fault [16], [24].

One implication of the selectivity is that the MV/LV distribution transformer should be able to carry a substantial fault current for some time. In the case of a LV short circuit, the MV/LV distribution transformer should be the last device to trip in the whole LV grid [16], [17], [25].

Overvoltage conditions are critical with respect to the *insulation coordination* of the transformer [26]. The overvoltage transients are also producing temporary overcurrents in the grid. **Fig. 3** depicts typical time-voltage characteristics of different overvoltage conditions in the MV grid [18], [26]. A similar diagram also exists for LV grids [20], [24].

Now that the stresses applied to a distribution transformer are identified, as well as the policies regulating protection concepts, it is possible to analyze the typical protection scheme of a LFT.

B. Protection of LFTs

LFTs are very robust with respect to overvoltages and overcurrents. The required ratings are specified in the relevant IEC/IEEE norms for the LFT itself (without external protection devices). For a 1 MVA transformer connected to the 10 kV grid (phase-to-phase RMS nominal system voltage [27]), the following limits are imposed:

- 12 kV, maximum operating voltage (MV side), excludes surge and transient overvoltages [27], [28].
- A short duration phase-to-phase RMS overvoltage capability of 20 kV for 1 min [28].
- Lightning impulse voltages of up to 75 kV [28], [29].
- A minimum short circuit ratio of 5.0% (to limit short circuit currents) [28].
- A current overload capability of 25× the rated current for 2 s, 11.3× for 10 s and 3× for 300 s [30].[1]

A comparison of these ratings with the requirements defined in Section II-A indicates that additional protection devices are required, as shown in **Fig. 4**. It contains fuses and breakers,[2] in order to allow the system to isolate the LFT in case of a short circuit fault or an overload condition [17], [21], [24]. Usually, the

[1] These values can slightly vary between LFT types and are given here as typical examples.

[2] Breakers can interrupt short circuit currents; disconnectors only disconnect the unloaded line. Alternatively, fuse/load switch combinations can be used instead of breakers. The fuse interrupts the short circuit current and the load switch, which can only interrupt the load current, is responsible for overload protection [16], [17].

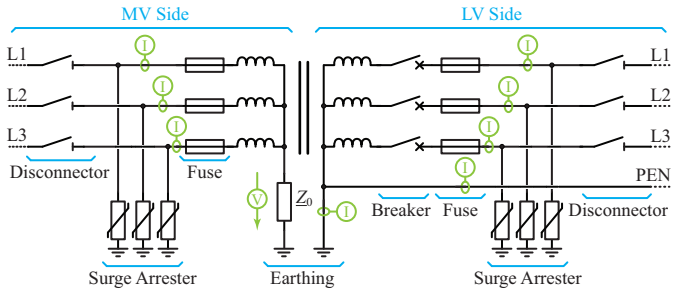

Fig. 4. Star-star distribution LFT with typical protection devices. The MV side of the transformer is earthed via an impedance while the LV side has a solid ground connection (with a TN-C earthing system [24]). The encircled green I and V labels show different current and voltage monitoring possibilities [16], [17].

overload protection is done on the LV side with breakers and only fuses are present on the MV side. Disconnectors are added on both sides in order to allow earthing and a voltage-free maintenance. The protection circuit further includes surge arresters to limit the impacts of lightning surges while the transformer insulation itself is able to deal with slow front, temporary, and permanent overvoltages (cf. Fig. 3) [17], [19].

C. Earthing of LFTs

An important aspect for the operation of LFT is the earthing of the LFT: according to Fig. 4 the star point earthing is different for the LFT's LV and MV sides.

The LV side of a LFT has a solid ground connection for safety reasons and in order to provide a protective earth neutral (PEN) conductor [22], [24], [31]. This implies that the short circuit currents are only limited by the impedances of lines and transformers. On the MV side, only three conductors are distributed, allowing different choices for the earthing, i.e. solid ground ($\underline{Z}_0 \to 0$), ungrounded ($\underline{Z}_0 \to \infty$ or delta windings), resistance grounding ($\underline{Z}_0 \approx R_0$), and Petersen coil ($\underline{Z}_0 \approx \mathrm{j}\omega L_0$) [24], [31]. This choice has a decisive impact on the short circuit currents and voltages during earth faults and is a trade-off between short circuit currents, damping of voltage and current transients, and overvoltages but is also a grid policy which can vary between operators and / or countries [31].

In case of a MV single-line-to-earth fault, where the effect of earthing is considered to be most important [23], the three-phase system becomes asymmetric, cf. **Fig. 5**. During this fault, the star point of the SST is shifted with respect to earth. As a consequence, one or more line-to-ground voltages (V_g) will exceed their nominal value (V_p). This effect is quantified by the earth fault ratio $k_\mathrm{V} = V_\mathrm{g}/V_\mathrm{p}$. In case of an ungrounded system and for resistance grounding, $k_\mathrm{V} = 1.7$ and $k_\mathrm{V} \approx 1.3-1.7$ apply, respectively. Even for solid earthing $k_\mathrm{V} \approx 1.1-1.3$ is anticipated, due to the limited conductivity of earth ($R_\mathrm{F} > 0$ in Fig. 5(a)). The system is defined as effectively earthed if $k_\mathrm{V} < 1.4$ applies [19], [23]. An effectively earthed system will features small overvoltages during earth fault at the cost of higher fault currents.

Tab. I summarizes the advantages and limitations of different earthing systems (cf. Fig. 5). The factor k_I is the ratio between the single-line-to-earth fault current and the three-phase symmetrical short circuit current (short circuit between the three phases) [16], [23]. This determines the maximum accepted fault duration. It should be noted that these values can vary between grids (voltage level, short circuit power, etc.) and are here only given as typical examples.

TABLE I
ADVANTAGES AND LIMITATIONS OF THE DIFFERENT EARTHING USED FOR TYPICAL MV DISTRIBUTION GRIDS [19], [31].

Features	$R_0 = \infty$	$R_{0,\mathrm{high}}$	$R_{0,\mathrm{low}}$	$R_0 = 0$
Overcurrent	low	low	med.	high
Overvoltage	high	high	med.	low
k_V	1.7	1.4 – 1.7	1.2 – 1.4	1.1 – 1.3
k_I	< 0.01	< 0.01	0.05 – 0.2	0.5 – 1.7
Trans. Damping	low	low	high	med.
Device Protection	low	high	med.	med.
Service continuity	high	med.	low	low
Accept. fault duration	large	3.0 s	1.0 s	< 0.5 s

III. Fault Conditions and Protection of SSTs

A. SST Protection Scheme

The SST is a complex device and, as a consequence, a multitude of different failure modes are possible, e.g. failures of semiconductors, thermo-mechanical failures, control errors, measurement errors, or insulation breakdown (particularly critical for the MV converter [8], [9]). The SST has some current and voltage overload capabilities, where the employed semiconductors are identified to mainly restrict the SST's overcurrent and overvoltage capabilities [12], [32].

In case of overcurrents, thermal time constants in the range of several seconds apply for the packages of power semiconductor switches and milliseconds for the chips, which drastically limit the durations of excessive overcurrents. For a SST the typical maximum allowable overcurrent ratios are in the range of 1.5× for some minutes and 5× for some milliseconds [4], [12], [32], [33].

Regarding MV side overvoltage capabilities, increased breakdown voltages (dielectric breakdown but also flashover in air) apply for pulses with short durations (e.g. lightning pulses) [18], [21]. However, semiconductors are very sensitive to overvoltage conditions and may not withstand any overvoltages that exceed the maximum blocking voltage capabilities. For this reason, the acceptable transient overvoltage waveforms for a SST are mostly defined by the filters, which provide a smoothing effect for the surges [32], [34]. The breakdown voltages of the power semiconductors, thus, need to be selected such that they withstand the maximum voltage that appears for voltage pulses with longer durations, where the filter is not sufficiently effective. For MV IGBTs the voltage utilization at rated operating conditions is usually between 40 % and 60 % [9], [35] while SiC FETs can be used up to 80 % [36]. However, as explained, the voltage utilization, is also determined by transient overvoltages.

The lack of robustness of SSTs can be compensated with redundancy, as often done for multi-cell SST topologies [6], [9]. Furthermore, the SST is also capable to operate with the non-ideal loads mentioned in the introduction. In such cases, the DC-links of the SST (cf. Fig. 1) offer a decoupling between the MV and LV grids. This means that disturbances from one grid are not transmitted to the other one [13], [32]. Unlike LFTs, SSTs can measure and control voltages and currents or can even commence a shutdown when a fault occurs [3], [37].

Since the overcurrent and overvoltage capabilities of SSTs are limited, additional external protection devices are required. An adapted version of a LFT protection scheme (cf. Fig. 4) is proposed in **Fig. 6**. A breaker (or at least a fuse/load switch combination) is also required at the MV side, due to the SST's limited overcurrent capability (the semiconductors are too fragile to trigger MV fuses) and for disconnecting the SST from the grid [12], [16], [17], [33].

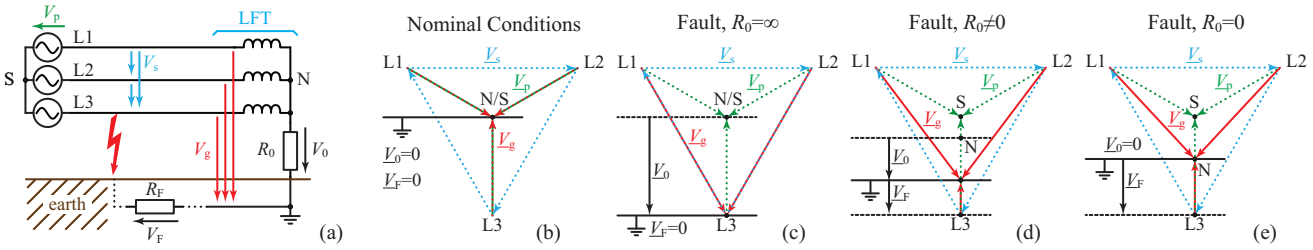

Fig. 5. (a) Single-line-to-ground fault of a LFT MV side supplied by an ungrounded generator [19]. (b) Typical phasors for the nominal conditions, (c) for an ungrounded star point, (d) resistance grounding, and (e) direct grounding. The earthing resistance is defined as R_0 and the fault resistance is R_F. For simplicity, purely ohmic impedances are used. In practice, the inductances of the line and of the transformer introduce additional phase shifts [23].

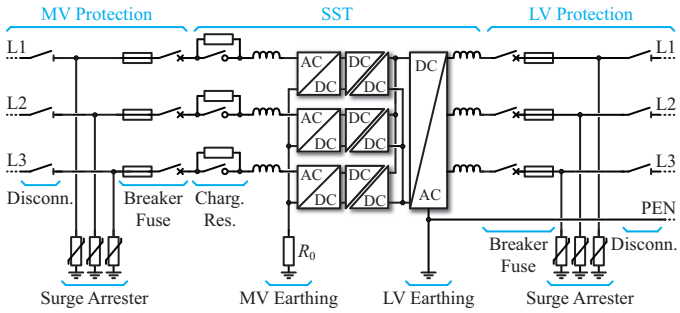

Fig. 6. Proposed SST protection scheme with the minimum number of protection devices. Compared to LFT (cf. Fig. 4), breakers at the MV side and charging resistors are required additionally. The earthing of the MV side is realized with a resistance and the LV side is solidly grounded.

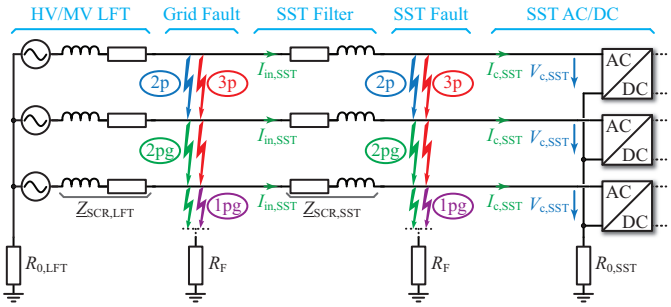

Fig. 7. Two bus equivalent circuit used for the computation of short circuit currents and voltages for the MV side. The different grid and SST fault types (line-to-earth, line-to-line, three-phase, etc.) are also shown along with the fault resistances considered in the calculation.

In addition to the actual protection circuitry, the MV rectifiers of the SST most commonly act as diode rectifiers during the startup procedure, making a precharging resistor necessary in order to limit the inrush current [9], [38]. The precharging resistor requires an additional bypass load switch at the MV side of the SST.

This protection scheme will now be analyzed in more detail for the most critical faults, i.e. LV and MV short circuits and overvoltages.

B. LV Short Circuit

The LV side of the SST has a solid ground connection and a PEN conductor [22], [24], [31]. A current can flow in this conductor if the load is not symmetric or during a fault. For short circuit considerations, a radial LV grid is assumed where the loads are completely fed by the SST. This is the case for most traditional (non-smart) LV grids or industrial grids.

The SST is capable of detecting the presence of LV short circuits and could immediately control all phase currents to zero. With this, however, the downstream breakers and / or fuses, i.e. the breakers and fuses placed between the LV side of the SST and the end-consumer, will not trip, since a LV fuse requires more than 5× the rated current for some seconds in order to trip [17], [24]. Due to this reason, the SST needs to inject a short circuit current during the fault [3], [10]. The respect of the selectivity represents an important overrating requirement for the LV inverter, not only regarding the semiconductors but also the filter inductors, which should not saturate at the required short circuit current.

Alternative solutions include the use of downstream breakers and fuses that are adapted to SSTs [12], [17] and / or the operation in a smart grid environment, where the communication between the devices enables a rapid identification of the fault such that the SST does not have to inject short circuit current for respecting the selectivity (due to the improved logic selectivity) [3], [12].

C. MV Short Circuit

1) Modelling: The MV short circuit analysis is more complex compared to LV faults, because no neutral conductor is distributed (different grounding methods, cf. Section II-C). The selectivity constraints are also reduced (SSTs downstream with respect to the fault) as long as the SST does not act as a generator [17], [24], [25]. Finally, the transformers which are feeding the MV grids (HV/MV transformers) and the generators connected to the MV grid will provide short circuit currents. If required, the SST could also provide some amount of current (double fed fault) [23].

The presented short circuit analysis is based on a single-line model where the MV/LV SST is fed by a HV/MV LFT as shown in **Fig. 7**. This work considers two possible cases for a SST that is confronted with a MV short circuit:

- A short circuit occurs in the grid or at the input of the SST. The SST shuts down the MV AC/DC stages, i.e. opens all switches of the MV AC/DC stages. After an initial transient, the input currents of the SST are zero. ($I_{c,SST} = I_{in,SST} = 0$ in Fig. 7).
- Due to an internal failure, the SST causes a short circuit after the filters. The SST shuts down the (remaining) MV AC/DC stages but a current is still present at the input ($I_{c,SST} = 0$, $I_{in,SST} \neq 0$ in Fig. 7).

In addition to a simple shut down of the MV AC/DC stages of the SST, the active current control during a grid fault could be considered. However, this will require a fast identification of the fault in order to react appropriately [10], [11], [13]. Furthermore this control strategy should preserve the power flow. Otherwise the mismatch between the MV and LV power flow will cause a rapid drift of the DC-link voltages. For these reasons, together with the requirement that a fault control strategy should be particularly robust, the possibility of active control is not further examined in this paper.

TABLE II
PARAMETERS USED TO ANALYZE MV SHORT CIRCUITS [4], [16], [28].

Name	Description
V	10 kV, phase-to-phase voltage, RMS
S	1 MVA, rated power
SCR_{LFT}	5 %, LFT short circuit ratio
XR_{LFT}	10, LFT reactance/resistance ratio
SCR_{SST}	open design parameter, SST short circuit ratio
XR_{SST}	100, SST reactance/resistance ratio
FIR	0.001, Fault impedance ratio
EIR_{LFT}	open design parameter, LFT earthing resistor
EIR_{SST}	open design parameter, SST earthing resistor

In order to extract figures of merit which are scalable for SSTs with different voltage and power levels, the parameters of the SST are scaled by means of a per-unit system where the rated line-to-line RMS voltage (V) and the rated power (S) are the base values used for scaling. The short circuit ratio (SCR) is the ratio between the nominal phase current and the symmetric three-phase short circuit current (fault 3p in Fig. 7) and can be expressed as (for the LFT and SST, cf. Fig. 7) [16], [28]:

$$SCR = Z_{SCR}\frac{S}{V^2}, \qquad \underline{Z}_{SCR} = Z_{SCR}\,\mathrm{e}^{\mathrm{j}\arctan(XR)}, \tag{1}$$

where XR is the ratio between the reactance and the resistance. The earthing and fault resistances are scaled with respect to the load impedance and form the earthing impedance ratio (EIR) and the fault impedance ratio (FIR):

$$EIR = R_0\frac{S}{V^2}, \qquad FIR = R_{\mathrm{F}}\frac{S}{V^2}. \tag{2}$$

2) Results: For the numerical analysis, typical values, listed in **Tab. II**, are chosen for a 1 MVA SST that is connected to the 10 kV grid. No line impedance (back to back connection) is considered between the LFT and the SST (most critical case).

If the SST shuts down in case of a MV grid fault, the three currents $I_{\mathrm{c,SST}}$ are zero and, thus, the current through the grounding resistor, $R_{0,\mathrm{SST}}$, and the corresponding voltage drop are zero, too. Additionally, the opening of the mechanical breaker will not produce any transient. Depending on the type of fault, however, increased input voltages, $V_{\mathrm{c,SST}}$ in Fig. 7, result if the SST shuts down. The occurring voltages are depicted in **Fig. 8(a)** for the different fault types, where the identified worst case scenario is the single-line-to-ground fault (1pg) leading to a maximum peak input voltage of

$$\hat{V}_{\mathrm{c,SST}} = \hat{V}_{\mathrm{p}}\left|\mathrm{e}^{\frac{\mathrm{j}2\pi}{3}} - \frac{EIR_{\mathrm{LFT}}}{SCR_{\mathrm{LFT}} + EIR_{\mathrm{LFT}} + FIR}\right|, \qquad \hat{V}_{\mathrm{p}} = \frac{\sqrt{2}}{\sqrt{3}}V. \tag{3}$$

The voltage stress reaches the line-to-line voltage (1.7 p.u.) with an unearthed LFT which corresponds to the earth fault ratio defined in Section II-C.[3] Since the MV rectifiers act as a diode rectifier when turned off, this voltage should be taken into consideration when choosing the maximum allowable DC-link voltage and the semiconductor blocking voltages.

In order to limit the short circuit current flowing in the grid in case of a failure of the SST, a SCR_{SST} of at least 5.0 % is required by the IEC norms [28]. A higher SCR_{SST} will limit the stress applied to the grid and to the SST, which could prevent further damages of the SST. **Fig. 8(b)** depicts the fault currents flowing inside the SST in case of an internal failure (SST fault in Fig. 7). A solidly grounded LFT, an unearthed LFT, and different SST short circuit impedances are considered while the MV inverters are turned off such that the SST earthing has no impact on the computed current.[4]

[3]The voltage computed with (3) is only valid for steady-state; this upper bound will never be reached if the duration of the short circuit is very small. Thus, for an infinite SST earthing impedance, the SST will never reach the steady-state value and the complete three-phase system will have a voltage offset. Still, the steady-state values are interesting in order to assess the worst case stress scenario.

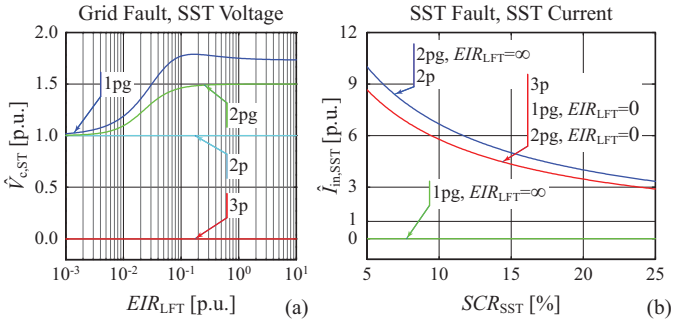

Fig. 8. (a) Steady-state voltage stresses ($\hat{V}_{\mathrm{c,SST}}$ normalized to phase peak voltage $\hat{V}_{\mathrm{p}}$) applied to the SST during different grid short circuits in dependence of the earthing of the LFT. (b) Converter steady-state currents ($\hat{I}_{\mathrm{in,SST}}$ normalized to the phase peak current $\hat{I}_{\mathrm{p}}$) during an internal SST fault. The currents are shown for different types of earthing of the LFT and different SST short circuit ratios.

The fault 2p produces the largest current, independent of the type of earthing. By contrast, the 1pg fault current is zero in case of an unearthed LFT (no current path exists). Globally, one can see that the value of the fault current can by adjusted by a proper choice of the short circuit ratio of the SST. The 3p fault current, which is almost equal to the 2p current, can easily be computed as:

$$\hat{I}_{\mathrm{in,SST}} = \hat{I}_{\mathrm{p}}\frac{1}{SCR_{\mathrm{LFT}} + SCR_{\mathrm{SST}}}, \qquad \hat{I}_{\mathrm{p}} = \frac{\sqrt{2}}{\sqrt{3}}\frac{S}{V}. \tag{4}$$

From the presented results, it can be seen that a SCR smaller than 10 % will lead to very large currents in the filter. For a typical 10 kV, 1 MVA multi-cell SST, however, the filter impedance required to sufficiently suppress harmonic components leads to $SCR \approx 7\,\%$ [4]. Therefore, the filter size is not primarily determined by harmonics filtering but by the SCR value that is required to allow an adequate handling of fault conditions [9].

It can be concluded that the filter should be able to deal with the short circuit current (determined by the SCR) until a breaker clears the fault (which can take several seconds, cf. Tab. I [9]). As long as the MV inverters are capable of turning off, the fault current will not flow in the SST (only in the filter in case of a failure occurring between the filters and the inverters). Therefore, a lower overcurrent rating can be used for the inverter since the bridges will not conduct the fault current [12], [32], [33]. In case of a failure of the inverters, the filter impedance limits the fault current inside the SST and protect the grid against to large overcurrents [28].

3) Advanced Short Circuit Protection: For the cases where having a high DC-link voltage and SCR value is not possible or desirable, additional protection devices need to be used [23]. An ultra-fast solid-state breaker can be employed to immediately disconnect the SST from the MV grid [37], [39] at the cost of reduced reliability and increased conduction losses. Furthermore the breaker should be capable of blocking the phase-to-phase voltage (cf. Fig. 8(a)) and dealing with the inductive switching overvoltage due to the current chopping [21]. Alternatively, a solid-state current limiter

[4]The results of Fig. 8(b) have been computed for short circuits between the SST filter impedances and the SST's AC/DC converters. The impacts of AC/DC converter failures on the SST's input currents are not considered. A detailed investigation reveals that the used considerations lead to worst case scenarios, which is due to the current limiting effect of $R_{0,\mathrm{SST}}$.

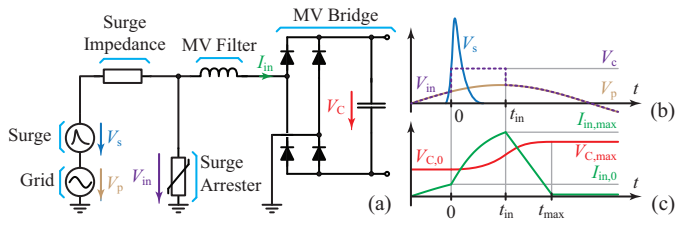

Fig. 9. (a) Equivalent circuit for single-phase overvoltage surge propagation in the SST. (b) Impact of the surge at the input of the SST and (c) typical surge propagation inside the SST.

can be installed in order to increase the short circuit impedance during a fault [39], [40]. However, an evaluation of the advantages and the disadvantages of such advanced protection measures is outside the scope of this work.

D. SST overvoltage

1) LV/MV Overvoltages: The overvoltage protection of the SST's LV side is similar to the protection of a solar inverter [20], [24], [41], [42]. Therefore, this paper only considers MV overvoltages. Furthermore, the investigation is limited to switching and lightning surges. The remaining overvoltages are either absorbed by the input filter of the SST (e.g. in case of very fast front or low-energy overvoltage pulses [43]) or, in case of enduring overvoltage conditions, e.g. due to a short circuit failure, require the SST to be rated for these (cf. Section III-C).

If surge arresters are placed as shown in Fig. 6, the clamping voltage has to be chosen together with the earth fault ratio in order to avoid thermal runaways [19]. The clamping voltage will also be higher in the case of an unearthed grid, cf. Fig. 8(a).

However, overvoltage surges often feature distinctive common-mode components, which appear across the earthing resistor (R_0 in Fig. 6) for an unearthed SST. This event denotes a considerable common-mode stress for the SST [44]. Nevertheless, the earthing resistor absorbs a part of the energy stored in the overvoltage surges and reduces the applied stress [32], [33]. The largest stress appears with a solid grounding of the SST and therefore this case will be further considered.

2) Modelling: If the SST is solidly grounded, the surge propagation inside the SST can be approximated with a single-phase equivalent surge as shown in **Fig. 9(a)**. The origin and propagation of the surge is replaced by a voltage source with an impedance as described in [28], [45]. During overvoltage situations, many SSTs can be modelled as diode rectifiers [1], [6] since the switching state of the inverters does not have a critical impact on the propagation of the surge [33].

A surge with sufficiently high voltage (lightning surge) is clamped by the surge arrester (clamping voltage V_c, cf. **Fig. 9(b)**), producing a nearly rectangular voltage at the input of the SST (V_{in}). Due to the line and surge impedances, the duration of this pulse is longer than the duration of the surge V_s. Even though this simplified model may not exactly represent the propagation of a surge in a MV grid (no wave reflections are considered) [45], [46], the corresponding pulse distortion is considered to be sufficient for the evaluation of the robustness of the SST. The switching surge are also approximated with rectangular excitations.[5]

Three characteristic values, which allow the computed results to be compared with different SSTs, are employed for describing

[5]Since the magnitude of a switching surge is smaller than the clamping voltage of the arresters, the input voltage is not rectangular. Still, the surge can be approximated by an equivalent rectangular excitation order to obtain a simplified model.

TABLE III
PARAMETERS USED TO ANALYZE MV OVERVOLTAGES [4], [21], [28].

Name	Description
V	10 kV, phase-to-phase voltage, RMS
S	1 MVA, rated power
SCR	open design parameter, SST short circuit ratio
XR	100, SST reactance/resistance ratio
CVR	1.4, capacitor voltage ratio
CER	open design parameter, capacitor energy ratio
$I_{in,0}$	0 A, initial current
$V_{c,lightning}$	$2.5\sqrt{2}\,V$, lightning surge (clamped by surge arrester)
$t_{in,lightning}$	500 µs, lightning surge duration
$V_{c,switching}$	$2.0\,\frac{\sqrt{2}}{\sqrt{3}}\,V$, switching surge level
$t_{in,switching}$	3000 µs, switching surge duration

the SST during overvoltages: the short circuit ratio (SCR, cf. (1)), the DC-link capacitor voltage ratio (CVR) and the capacitor energy ratio (CER):

$$CVR = \frac{V_{C,0}}{\frac{\sqrt{2}}{\sqrt{3}}V}, \qquad CER = \frac{\frac{C\,V_{C,0}^2}{2}}{\frac{S/3}{2f}}, \tag{5}$$

where V is the nominal phase-to-phase RMS voltage and S is the rated power. Thus, CVR is the ratio of the nominal DC-link voltage to the peak AC phase voltage and CVR is the ratio of the energy stored in the DC-link capacitor to the energy consumed by one phase during a grid half period.

3) Results: This Section presents the results obtained from numerical calculations, which approximate the switching and lightning surges with rectangular excitation V_c with duration t_{in}. **Tab. III** summarizes the parameters used for the calculations.

The surge arresters are designed with respect to the phase-to-phase voltage in order to be able to withstand temporary overvoltages (cf. Section III-C). The clamping voltage is 2.5 times larger than the rated stand-off operating voltage of the arresters [19]. For lightning surges, the input voltages reach the clamping voltages of the arresters. For the defined switching surges, the arresters are not fully clamping the voltage due to the lower magnitudes of the surges (2.0 the peak phase voltage). In order to assess the maximum possible overvoltages, the surges are triggered at the peak grid voltage. The employed procedure computes the input inductor peak current and the output capacitor maximum voltage as shown in **Fig. 9(c)**.

Fig. 10 depicts the voltage stresses caused by lightning or switching surges for different SCR and CER values. For designs with low CER values, lightning surges are more critical than switching surges with respect to the DC-link overvoltage. However, increased values of the CER more effectively reduce the impacts of lightning surges. This is due to the comparatively long durations of switching surges and the surge arresters being non-effective in case of switching surges. During a lightning surge, the maximal inductor current mainly depends on the value of the SCR (and not of the CER) because the DC-link voltage remains approximately constant during the fast current rise.

According to Fig. 10(a)-(b) a sufficiently large DC-link capacitance needs to be considered in order to avoid excessively high overvoltages inside the SST. Furthermore, the filter inductances, represented with SCR, need to be large enough to avoid high inrush currents in the events of lightning and switching surges as shown in Fig. 10(c)-(d), in particular in the case of large DC-link capacitances and switching surges (bottom right part of Fig. 10(d)).

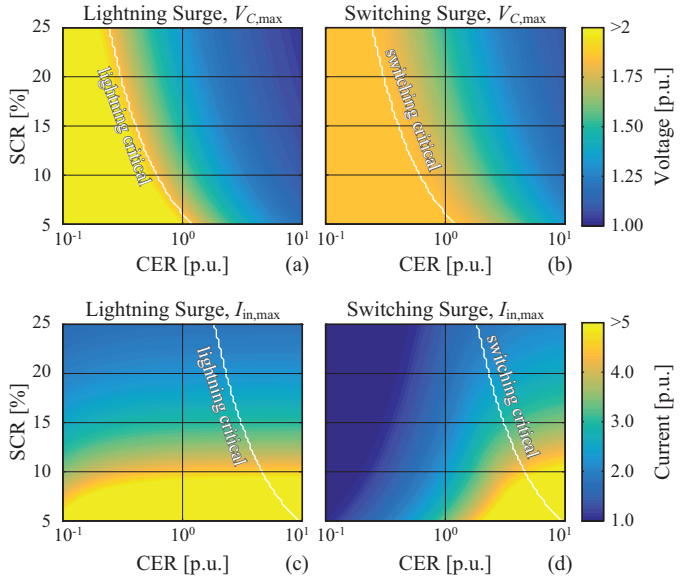

Fig. 10. (a), (b) Maximum voltages and (c), (d) currents for lightning and switching surges. The voltage $V_{C,\max}$ is normalized to the initial voltage $V_{C,0}$ and the maximum current $I_{\text{in,max}}$ to the nominal peak phase current $\widehat{I}_{\text{p}}$. All simulations have been conducted for $CVR = 1.4$ [4], [6]. The white line distinguishes the domain where switching surges are more critical than lightning surges.

For example, in case of $CER = 1.0$, $CVR = 1.4$, and a typical filter inductance, e.g. $SCR \approx 10\,\%$, the DC-link voltage reaches twice its nominal value in case of a switching surge (cf. Fig. 10(b)) and the current reaches four times the rated current during a lightning surge (cf. Fig. 10(c)). Thus, the selected power semiconductors need to be rated accordingly, to withstand the maximum possible instantaneous DC-link voltage and the corresponding surge current.

4) Advanced Overvoltage Protection: One can see that, even with metal oxide arresters, large stresses are applied to the SST during overvoltages. Additional protection devices can be used for limiting the impacts of surges:

- Three additional surge arresters, placed between the phases, enable a reduction of the clamping voltages between phases by at least 16 % and even more if the earth fault ratio is large [19].
- If the temporary overvoltages can be interrupted quickly, surge arresters with a lower clamping voltage could be selected (thermal time constant of arresters is several seconds) [19].
- Surge capacitors can be used to smooth the surges [34], [47], which, however, increases the reactive power consumption.
- Ultra-fast solid-state breakers, rated for the clamping voltage of the surge arresters, can be used for disconnecting the SST in the event of a surge [37], [39]. The disconnection and reconnection of the SST during a surge may however excite substantial perturbations in the MV grid.
- The use of additional protection devices with lower clamping voltages compared to metal-oxide arresters. Suitable devices or circuits include TVS diodes, thyristors, and braking choppers [34], [48], [49]. In order to avoid inrush currents through the AC/DC converters, these devices could be placed between the converter and the filter (AC side).
- Another approach is the suppression or mitigation of the transients in the MV grids. For example, switching transient can be almost suppressed if the breaker actions are synchronized with the phase of the grid. [50]. However, transients due to lightning or unpredictable faults cannot be avoided.

IV. Design Guidelines

From the presented analysis, some design guidelines can be extracted for a SST connected to the grid with standard protection devices (surge arresters, breakers, fuses):[6]

- The power semiconductors need to be capable to block more than 3× the nominal phase voltage. This guideline comes from the required nominal DC-link voltage for dealing with permanent overvoltage, the voltage utilization of the power devices, the overvoltages appearing during an earth fault, and the overvoltages due to switching and lightning surges (cf. Sections III-C and cf. Section III-D).
- Sufficiently large MV filter inductances are needed to provide short circuit current limitation and to limit the inrush currents in case of overvoltage pulses. A short circuit ratio of at least 10 % is required. Moreover, high enough saturation currents need to be considered (cf. Sections III-C and III-D).
- The MV inverter should be able to accept at least 4× the rated current for some milliseconds (inrush currents during switching surges) and 1.5× for some minutes (overload) (cf. Sections III-C and III-D).
- The DC-link capacitance should be sufficiently large, e.g. $CER > 1.0$, in order to maintain reasonable values of DC-link overvoltages in case of lightning and switching surges. Large DC-link capacitances, however, demand for a sufficiently high filter inductance to avoid large inrush currents (cf. Section III-D).
- The LV inverter needs to inject enough fault current in order to trip the downstream protection devices. An overcurrent capability of 3× the rated current for some seconds should be considered for tripping a sensitive breaker while a fuse will require even larger currents (cf. Section III-B).

V. Conclusion

This paper proposes a protection scheme for SSTs that are used to power a LV grid from a MV grid. The work further investigates design criteria and limitations with respect to current and voltage stresses, in particular with respect to robust operation in the MV grid. In this context, different short circuit failure types and overvoltage scenarios are analyzed with the result that line-to-earth short circuits and slow front overvoltage situations are particularly critical. Furthermore, the MV side earthing of the grid is found to have a decisive impact on the stresses in case of short circuit failures.

The required overcurrents and overvoltages capabilities need to be taken into account for the design of a SST and have an impact on the achieved efficiency, power density, volume, and cost. In this context, a high switching frequency may not reduce the volume required for the protective circuits and the MV side filter of the SST. The impact will be particularly important for designs with low power rating, high switching frequency, or high voltage utilization of power devices. Alternatively, a less robust SST may be considered if advanced protection devices, such as solid-state circuit breakers, are used.

The presented analysis shows that a reasonable protection of SSTs is achievable. However, the design of SSTs not only involves the conception of power electronic converters. Also the interactions between the SST and the connected grids need to be taken into account in order to take advantage of dedicated SST features such as flexibility, DC output, and power flow control.

[6]Guidelines come from the analysis of a 10 kV, 1 MVA SST, as shown in Fig. 1. The exact requirements will depends on the voltage and power ratings, SST and grid topologies, etc. Still, the proposed requirements are useful as general guidelines.

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