# A Novel Three-Phase Utility Interface Minimizing Line Current Harmonics of High-Power Telecommunications Rectifier Modules

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***Abstract*— Based on the combination of a three-phase diode bridge and a dc/dc boost converter, a new three-phase three-switch three-level pulsewidth modulated (PWM) rectifier system is developed. It can be characterized by sinusoidal mains current consumption, controlled output voltage, and low-blocking voltage stress on the power transistors. The application could be, e.g., for feeding the dc link of a telecommunications power supply module. The stationary operational behavior, the control of the mains currents, and the control of the output voltage are analyzed. Finally, the stresses on the system components are determined by digital simulation and compared to the stresses in a conventional six-switch two-level PWM rectifier system.**

***Index Terms*— Comparison of converter concepts, control of neutral point potential, hysteresis control of mains phase currents, neutral-point-clamped converter, three-phase three-level PWM rectifier (VIENNA rectifier).**

## I. Introduction

CONVENTIONAL power supplies of the interchanges of telecommunication systems are being replaced more and more by modular rectifier systems, due to the advantages of the latter concerning operational behavior, systems technology, and costs. There, the rectifier modules (having a three-phase supply for a higher number of subscribers and/or higher rated power) are realized as voltage dc-link converters in general. In the simplest case, the mains ac voltage is converted into a dc-link voltage by a three-phase diode bridge with capacitive smoothing. This dc-link voltage is then transformed into the output dc voltage by a high-frequency dc/dc converter connected in series.

The realization of the input stage of a power supply module as an uncontrolled three-phase bridge (in many cases directly connected to the mains) is motivated by the requirement of a high power density, high efficiency, high reliability (robustness), and low cost. However, this concept shows the disadvantage of high effects on the mains, due to high amplitudes of low-frequency mains current harmonics which lead to a distortion of the mains voltage. Therefore, the danger of an influence on, or disturbance of, other loads is present. This is true especially for high installed power and high inner mains impedance. In connection with the limitation of harmonics stress on the public low-voltage mains caused by power electronic converters—as requested by guidelines [1], recommendations, and future standards (IEEE Std. 519-1992, IEC-555-2, and IEC-555-4 [2])—the development of ac/dc converters having low influence on the mains is of special importance. This is especially important for guaranteeing universal applicability of telecommunication rectifier modules.

The scope of this paper is the development and analysis of a new three-phase high-frequency unidirectional pulsewidth modulated (PWM) ac/dc converter for feeding the dc link of a 12-kW telecommunications power supply module. For the determination of the circuit concept, the following basic requirements are given:

- approximately sinusoidal current consumption;
- resistive mains behavior;
- controlled output voltage;
- low-blocking voltage stress on the power transistors;
- high power density;
- high efficiency;
- low complexity of the power and control circuits;
- high reliability.

In Section II, the topology of a new three-phase three-switch three-level ac/dc boost converter is derived based on the basic structure of the power circuit of a three-phase ac/dc converter with controlled output voltage. This basic structure mentioned is based on the series connection of a three-phase diode bridge and a dc/dc boost converter. In Section III, the stationary operational behavior of the converter is analyzed. Based on this, the control range of the phase angle of the mains current is determined, as well as the minimum value of the output voltage being required for a given output power and given mains current phase angle for sinusoidal shape of the mains current. In Section IV, the tolerance band control (in order to have low development and production costs) of the mains current and the control of the capacitive center point of the output voltage (being included into the system function) are discussed. The realization of these considerations is discussed in Section V by using digital simulation. Finally, in Section VI, the voltage and current stresses on the active and passive components are given for

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|---|---|
| ouput power | 12.6 kW; |
| output voltage | 700 V; |
| mains line-to-line voltage | 400 V; |

Manuscript received September 11, 1994; revised February 9, 1997. This work was supported by the Austrian Fonds zur Förderung der wissenschaftlichen Forschung.

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Publisher Item Identifier S 0278-0046(97)05259-3.

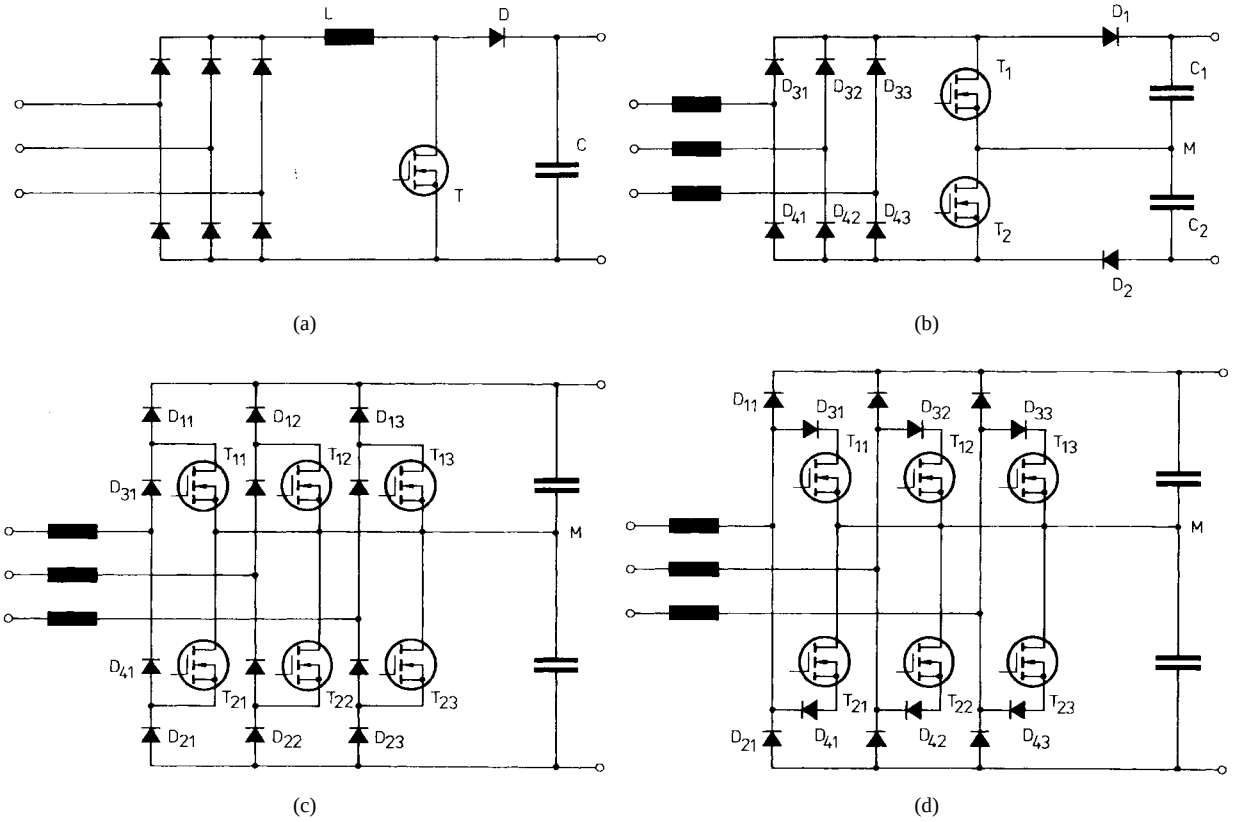



Fig. 1. Development of the basic circuit structures of three-phase three-level PWM rectifiers [(c) and (d)] based on a combination of a three-phase diode bridge and a dc/dc boost converter (a).

(there, one assumes that the system is applied for supplying the dc/dc converter part of a telecom power supply module with rated output power 12 kW (60 V/200 A) and efficiency of $\eta_{\mathrm{dc/dc}} \approx 0.95$). Also, a comparison is made to the component stresses of a conventional six-switch two-level voltage dc-link PWM rectifier system.

## II. Derivation of the Circuit Structure

For the realization of a three-phase unidirectional ac/dc converter with controllable output voltage, a series connection of an uncontrolled diode bridge and a dc/dc boost converter can be used in the simplest case (Fig. 1(a), [4]). However, in the mains current spectrum of this system, low frequency harmonics of high amplitude are present. Due to the operating principle of a three-phase diode bridge, only two phases always conduct current (with the exception of the commutation intervals). Therefore, the phase current shape shows $\pi/3$-wide intervals with zero current.

A reduction of the effects on the mains of this system can be obtained by placing the inductor $L$ on the ac side and by operating the converter in the discontinuous conduction mode (DCM) [6]. Analogous to the DCM of single-phase ac/dc boost converters [7], in this case, a voltage proportional guidance of the peak values of the discontinuous input currents is given directly by the mains phase voltages (for time constant duty cycle of the power transistor $T$). However, as a closer analysis of the system behavior shows, the harmonic content of the mains phase currents remaining after filtering of the discontinuous input quantities is essentially determined by the output voltage level [8]. A largely sinusoidal mains current shape is linked to an output voltage being large with respect to the amplitude of the line-to-line mains voltage. For operating the system with the European low voltage mains (nominal rms line-to-line voltage: 400 V) we, therefore, have to split up the dc-side converter part (due to the blocking voltage stress on the dc-side power semiconductors for an output voltage $>1$ kV) into two simultaneously pulsed partial systems ( Fig. 1(b) or [9, Fig. 10]) having each to sustain half of the dc-link voltage.

The application of the circuit described so far is limited, especially by the discontinuous input current shape leading to high current stress on the power semiconductor devices and by the filtering effort required for limiting the conducted electromagnetic influence (EMI) [9]. These aspects exist in addition to to the high blocking voltage stress on the power semiconductor devices of a converter fed from the high dc-link voltage. Therefore, for the requirement of high output power, one has to ask the question for alternative concepts of three-phase unidirectional PWM boost rectifiers with continuous input current showing (ideally) purely sinusoidal shape and being independent of the output voltage level (being larger than the maximum value of the line-to-line mains voltage).

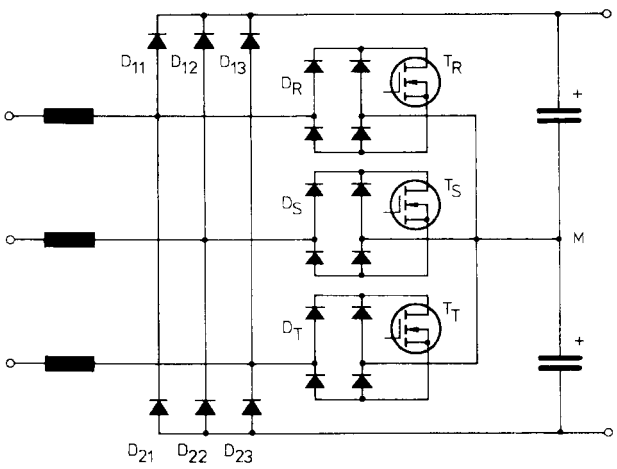
The current consumption of the system shown in Fig. 1(b) is defined, in general, by the difference between mains voltage and rectifier input voltage lying across the inductances connected in series at the input. A continuous, sinusoidal

mains current shape (with the exception of the harmonics with pulse frequency and their multiples), therefore, is obtained only by rectifier input voltages having sinusoidal shape in the average over the pulse periods. Therefore, this requires a separate controllability of the voltage synthesis of each phase or the application of synchronously controlled transistors $T_{1j}$ and $T_{2j}$ and of ouptput diodes $D_{1j}$ and $D_{2j}$ in each bridge leg $j = 1,2,3$, respectively [Fig. 1(c)]. Due to the inclusion of the center point of the output voltage into the system function, all power semiconductors of the resulting circuit (called *forced commutated three-phase boost-type rectifier* in [11]) only have to sustain half of the output voltage. However, the advantage of the low blocking voltage stress is followed by the disadvantage of relatively high conduction losses, because the entire current flow connected with supplying the output power goes through the diode legs due to the rectifier function of the converter.

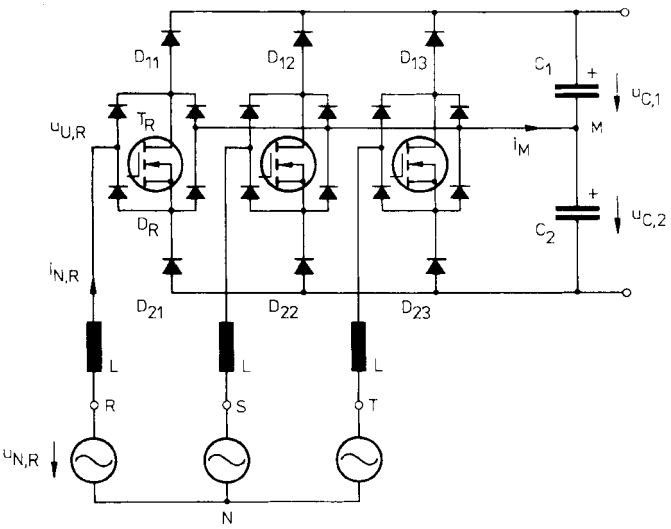
A reduction of the conduction losses can be obtained by shifting the diodes $D_{3j}$ and $D_{4j}$ into the circuit legs controlling the conduction state of the converter [Fig. 1(d)]. A further advantage of this circuit modification consists in the fact that then, in each phase, a bidirectional bipolar switch is realized by the control legs lying in antiparallel ($D_{3j}, T_{1j}$ and $T_{2j}, D_{4j}$). This switch can be replaced, as shown in Fig. 2(a), by the combination of a single-phase diode bridge $D_i$ and a power transistor $T_i$, $i = R,S,T$. Compared to a realization according to Fig. 1(c) or (d), this results in reducing the number of the turn-off power electronic devices by 50% and/or reduced control effort and in a higher utilization of the power transistors (there, the entire and not only half of the total transistor chip area of a phase is always used for conduction and control of the input current). However, now the diodes $D_{1j}$ and $D_{2j}$ have to sustain the full output voltage (and not, as for the circuit according to Fig. 1(c), only half of the output voltage) in the blocking direction. This disadvantage can be avoided, however, in a simple manner by the integration of the bidirectional bipolar switches $T_i, D_i$ into the bridge legs of the diode bridge on the input side [19]. This results in a new converter topology [Fig. 2(b)] which will be called *three-phase three-switch three-level (three-phase/switch/level) PWM (VIENNA) rectifier* in the following. Its detailed analysis is the topic of this paper.

*Remark:* One has to mention that, regarding the circuits shown in Fig. 1(c) and (d), a close topological relationship exists to the basic types of three-phase three-level PWM *inverters* introduced in [12] and [13]. Furthermore, one has to point out a modified circuit realization proposed in [14] according to Fig. 1(c), a PWM inverter circuit being identical with Fig. 2(a) regarding the control leg realization (as analyzed in [15]), and a converter structure which can be derived by further development of the circuit according to Fig. 2(a) as described in [16] using low switching frequency, i.e., three times the mains frequency. Single-phase realizations of the circuits given in Fig. 2 are analyzed in [17] and [18].

For the sake of completeness, we finally want to bring attention to papers describing circuit concepts of three-switch *two-level* PWM rectifiers, e.g., [19], [20] (cf. pp. 87–89), and [21]–[23].




(a)




(b)

Fig. 2. Basic structures of novel three-phase/switch/level unity power factor PWM (VIENNA) rectifier systems resulting by further development of Fig. 1(d); the feeding mains is replaced by voltage sources $u_{N,i}, i = R,S,T$; $N$ denotes the mains star point. The circuit shown in (b) has higher conduction losses as compared to the circuit according to (a). However, the diodes $D_{1j}$ and $D_{2j}$ (as well as all other power semiconductor devices) of (b) only have to sustain half of the output voltage. Due to the (in general) longer reverse recovery time of diodes with higher blocking voltage capability (and/or the higher switching losses connected herewith) one has to prefer circuit (b) for high pulse frequency as compared to (a).

## III. Principle of Operation

### A. Basic Function

For describing the basic function of the rectifier systems shown in Fig. 2, the analysis is limited to the fundamentals of the system quantities on the ac side.

Based on a single-phase equivalent circuit (Fig. 3), there follows (using complex ac current calculus) for the phasor of the rectifier input voltage fundamental [denoted by the index (1)]:

$$\underline{U}_{U,(1)} = \underline{U}_N - j\omega_N L \underline{I}_{N,(1)}. \tag{1}$$

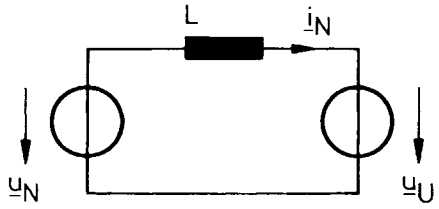



Fig. 3. Single-phase equivalent circuit related to the fundamental for the ac-side system section of a three-phase/switch/level PWM (VIENNA) rectifier.

The current consumption (and, therefore, the basis for the power consumption)

$$\underline{I}_{N,(1)} = \hat{I}_{N,(1)} \exp j(\varphi_N - \varphi) \tag{2}$$

$(\varphi_N = \omega_N t)$ of the system is defined by the voltage lying across the inductances $L$ connected in series on the ac side. There, this voltage is the difference between the (sinusoidal) mains voltage

$$\underline{U}_N = \hat{U}_N \exp j\varphi_N \tag{3}$$

$(\underline{U}_N = \underline{U}_{N,(1)})$ and the rectifier input voltage fundamental $\underline{U}_{U,(1)}$ which can be controlled regarding amplitude and phase via appropriate pulsation of the power transistors $T_i$, $i = R, S, T$ (Sections III-B and IV-A).

The power delivered to the dc side follows (if the system losses are neglected), based on the power balance, as

$$P_O = U_O I_O = \tfrac{3}{2} \hat{U}_N \hat{I}_{N,(1)} \cos\varphi. \tag{4}$$

### *B. Rectifier Input Voltage*

Forming of a rectifier input phase voltage $u_{U,i}$ is influenced according to

$$u_{U,i} = \begin{cases} \operatorname{sign}\{i_{N,i}\} \dfrac{U_O}{2} & \text{if } s_i = 0 \\ 0 & \text{if } s_i = 1 \end{cases} \tag{5}$$

also by the sign (direction) of the associated mains phase current $i_{N,i}$, besides by the switching state of the power transistor $T_i$ defined by a binary switching function $s_i$. (As reference point of the voltage $u_{U,i}$ the center point $M$ of the dc-link voltage is chosen.) Each brigde leg shows a three-level characteristic, i.e., three possible voltage values $+(U_O/2)$, 0, and $-(U_O/2)$. Accordingly, the system is called a *three-level PWM rectifier*.

### *C. Stationary Operating Region*

Due to the influence on the voltage generation caused by the sign of the phase currents [see (5)], the stationary maximum amplitude of the rectifier input voltage fundamental $\hat{U}_{U,(1),\max}$ (how it can be obtained without overmodulation) is defined also by the phase difference between $\underline{U}_{U,(1)}$ and the mains current fundamental $\underline{I}_{N,(1)}$. This definition by the phase difference has to be seen, besides the control limit $\hat{U}_{U,(1),\max} \leq (1/\sqrt{3})U_O$, which is given basically for bridge circuits. Therefore, in general, the definition of $\underline{U}_{U,(1)}$ is equivalent to defining the operating region of the converter [see (1)].

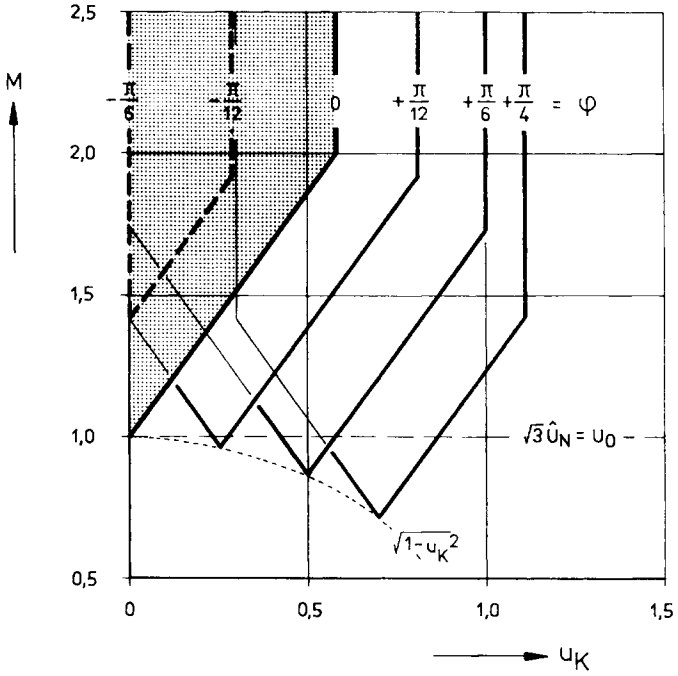



Fig. 4. Dependency of the operating region of a three-phase/switch/ level PWM rectifier system on the phase angle $\varphi$ of the mains current (representation limited to angles within the interval $\varphi \in [-(\pi/6), +(\pi/4)]$ for the sake of clarity). The limits of the operating regions are show by solid lines for $\varphi > 0$., and for $\varphi < 0$, dashed lines are used. The operation region for resistive mains fundamental behavior $(\varphi = 0)$ is marked by the dotted area.

For the case of a resistive mains fundamental behavior [$\varphi = 0$, (2)], being important for practical applications, the operating region of the PWM rectifier system is determined by

$$u_K \leq \begin{cases} \dfrac{1}{\sqrt{3}}(M-1) & \text{if } M \leq 2 \\ \dfrac{1}{\sqrt{3}} & \text{if } M > 2 \end{cases} \tag{6}$$

where

$$u_K = \frac{1}{\hat{U}_N} \hat{I}_{N,(1)} \omega_N L \tag{7}$$

characterizes the load condition of the converter and where

$$M = \frac{U_O}{\sqrt{3}\hat{U}_N} \tag{8}$$

defines the system voltage transformation. Because for high pulse frequency of the system there is always $u_K \ll 1$ (typically $u_K \approx 0.01 \cdots 0.02$), only the limitation for $M \leq 2$ is of importance in (6). For the minimum value of the output voltage there follows, accordingly,

$$U_O \geq \sqrt{3}\hat{U}_N + 3\hat{I}_{N,(1),\max} \omega_N L. \tag{9}$$

*Remark:* For deriving (6), a description of the system operation based on complex three-phase phasors (complex space vectors) is advantageous, due to special clarity and a simpler calculation [24] as compared to a calculation with phase quantities. The analysis (not shown in detail here for

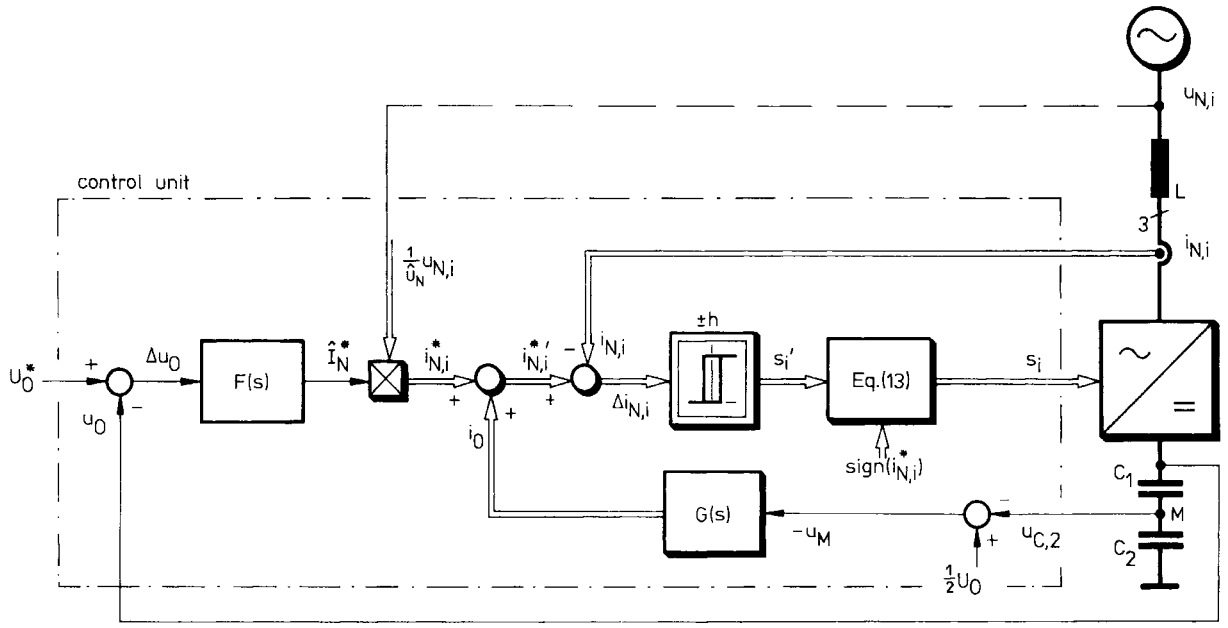



Fig. 5. Multiloop control of a three-phase/switch/level PWM (VIENNA) rectifier system. Outer control loops: $F(s)$: control of the output voltage $u_O$; $G(s)$: balancing of the output partial voltages $u_{C,1}$ and $u_{C,2}$. Inner control loop: tolerance band (or hysteresis) control of the phase currents $i_{N,i}, i = R, S, T$. The switching decisions $s_i'$ of the hysteresis controllers are inverted according to (13) for $\operatorname{sign}(i^*_{N,i}) = -1$; for the sake of clarity, signal paths equivalent for all phases are combined into double lines.

the sake of brevity) also shows a basic restriction

$$-\frac{\pi}{6} \leq \varphi \leq \frac{\pi}{2} \tag{10}$$

of the operation of the rectifier system with inductive $(\varphi > 0)$ or capacitive phase angle of the mains current. According to Fig. 4, $\varphi = -(\pi/6)$ is only obtained there for $u_K \to 0$ or for $\hat{I}_{N,(1)} \to 0$ and, therefore, it constitutes only a theoretical limiting case. The real power transferred to the output circuit

$$P_O = \frac{3}{2}\frac{\hat{U}_N^2}{\omega_N L} u_K \cos\varphi \tag{11}$$

becomes zero at both limits of the operating region. Feeding back of energy from the output circuit into the mains $(\varphi \in (\pi/2, \pi]$ or $\varphi \in (-\pi, -(\pi/2))$, therefore, is not possible, as can also be seen immediately from the circuit structure (Fig. 2).

System operation with a capacitive phase angle, in general, is linked to a higher amplitude of the rectifier input voltage as compared to inductive mains behavior. This can be explained based on a phasor diagram. This also means that a higher value of the dc-link voltage and/or a higher voltage transformation ratio $M$ is involved (Fig. 4).

Due to the dependency of the system control region on the phase difference of the fundamental of the rectifier input voltage and of the mains current, the minimum value $M_{\min}$ to be maintained for $u_K \to 0$ for capacitive *and* inductive mains current phase angle $\varphi$ lies above the value $M_{\min} = 1$, which is given for resistive mains behavior. For inductive mains behavior, the output voltage $U_O$ can theoretically be lowered in a section of the operating region below the voltage value $U_O = \sqrt{3}\hat{U}_N$ (and/or $M = 1$), resulting in the case of no-load and uncontrolled rectification $(s_i = 0)$. $\varphi \geq \pi/6$ requires a minimum load $u_K > 0$ of the system and is, therefore, of little practical importance.

## IV. System Control

Besides a control of the mains current and of the output voltage, we also have to provide a control of the potential of the output voltage center point (and/or an active symmetrization of the output partial voltages) for the proposed system. This would not be required for conventional PWM rectifier systems, but requires only a minor additional circuit effort, as will be shown in the following.

### A. Mains Current Control

The control of the power transistors and/or of the rectifier input voltage synthesis can be performed, in the simplest case, by a tolerance band or hysteresis control of the phase currents by independent phase current controllers.

The amplitude $\hat{I}_N^*$ of the phase current reference values

$$i_{N,i}^{*\prime} = \hat{I}_N^* \frac{u_{N,i}}{\hat{U}_N} \tag{12}$$

(which are derived directly from the phase voltages for resistive mains behavior) is given there by an output voltage controller $F(s)$, which is superimposed on the current control loop (Fig. 5). Because the control of the output voltage has no special features as compared to conventional converter systems, detailed explanations are omitted here for the sake of brevity.

The dependency of the sign of a rectifier input phase voltage $u_{U,i}$ (formed for $s_i = 0$) on the sign of the associated phase current $i_{N,i}$ [see (5)] has to be considered by generating the

control signals $s_i$ of the power transistors by an inversion

$$s_i = \begin{cases} s_i' & \text{if } i_{N,i}^* \geq 0 \\ \text{NOT } s_i' & \text{if } i_{N,i}^* < 0 \end{cases} \tag{13}$$

(as controlled by the sign of the mains current reference value $\text{sign}\{i_{N,i}^*\}$, Fig. 5) of the switching decision

$$s_i' = \frac{1}{2}\left(1 + \text{sign}\left\{\Delta i_{N,i} - h\,\text{sign}\left\{\frac{d\Delta i_{N,i}}{dt}\right\}\right\}\right) \tag{14}$$

($\Delta i_{N,i} = i_{N,i}^* - i_{N,i}$ denotes the control error of the respective phase current $i_{N,i}$) of the associated tolerance band controller.

*Remark:* Equation (14) is valid for the assumption that $d\Delta i_{N,i}/dt$ does not change its sign within the tolerance band $|\Delta i_{N,i}| < h$. For $|\Delta i_{N,i}| > h$ the switching decision is independent of the cicuit/switching history and/or of the direction of the change of $\Delta i_{N,i}$. Then, (14) can be replaced by

$$s_i' = \begin{cases} 0 & \text{if } i_{N,i} > i_{N,i}^* + h \\ 1 & \text{if } i_{N,i} < i_{N,i}^* - h. \end{cases} \tag{15}$$

As already explained in Section III-A, the mains current consumption of the PWM rectifier system is defined by the voltage lying across the series inductances $L$

$$L\frac{di_{N,i}}{dt} = u_{N,i} - (u_{U,i} - u_N) \qquad i = R,S,T. \tag{16}$$

There, via the voltage of the floating mains star point $N$ [see Fig. 2(b)]

$$u_N = \tfrac{1}{3}\sum_{i=R,S,T} u_{U,i} \tag{17}$$

which is influenced by the switching states of all phases, a coupling of the phase current changes is given. If independent phase current controllers are used, this coupling leads to the occurrence of limit cycles [27] and, therefore, to a nonoptimal utilization of the converter pulse frequency. Furthermore, the control error is not restricted to the deadband width $h$; the maximum value of the phase current ripple is defined by twice the value of the deadband width.

An avoidance of the disadvantages mentioned can be achieved by coordinating the switching actions of the phase current controllers [25]–[27]. This shall not be explained here in detail for the sake of brevity.

### B. Balancing of the Output Partial Voltages

As mentioned before, besides control of the output voltage and of the mains phase currents, a symmetrical split

$$u_{C,1} = u_{C,2} = \frac{U_O}{2} \tag{18}$$

of the output voltage has to be guaranteed by the control system of the converter. An unsymmetry of the output capacitor voltages $u_{C,1}$ and $u_{C,2}$ (caused by loading the capacitive center point $M$ by a dc current or low-frequency ac current) may be characterized by the voltage

$$u_M = \tfrac{1}{2}(u_{C,2} - u_{C,1}) \tag{19}$$

referred to the ficticious (ideal) center point of the output voltage. This unsymmetry will cause an increased voltage stress on one output capacitor, an increased blocking voltage stress on the power semiconductor devices situated in the control legs and on the freewheeling diodes of one bridge half, and an uneven current stress on the components over the fundamental period. According to (19), an ideally symmetric split of the output voltage is given for $u_M = 0$.

TABLE I
CENTER POINT CURRENT $i_M$ AND VARIATION OF THE CENTER POINT POTENTIAL $u_M$ IN DEPENDENCY ON THE CONVERTER SWITCHING STATE FOR $\varphi_N \in (-(\pi/6), +(\pi/6))$ OR $i_{N,R} > 0, i_{N,S} < 0, i_{N,T} < 0$ $(i_{N,R} \geq |i_{N,S}|, |i_{N,T}|)$, RESPECTIVELY [SEE (22)]; $(du_M/dt)_{\text{avg}}$ CHARACTERIZES THE POTENTIAL SHIFTS CAUSED BY A SWITCHING STATE BASED ON A RELATIVE ON-TIME BEING EQUAL FOR EACH SWITCHING STATE $(s_R, s_S, s_T)$ AND BEING CONSTANT OVER $\varphi_N$; FURTHER ASSUMPTIONS: PURELY SINUSOIDAL MAINS CURRENT SHAPE AND HIGH, TIME CONSTANT PULSE FREQUENCY

| $s_R$ | $s_S$ | $s_T$ | $i_M$ | $\left(\frac{du_M}{dt}\right)_{\text{avg}}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | $i_T$ | − |
| 0 | 1 | 0 | $i_S$ | − |
| 0 | 1 | 1 | $-i_R$ | −− |
| 1 | 0 | 0 | $+i_R$ | ++ |
| 1 | 0 | 1 | $-i_S$ | + |
| 1 | 1 | 0 | $-i_T$ | + |
| 1 | 1 | 1 | 0 | 0 |

The current

$$i_M = \sum_{i=R,S,T} s_i i_{N,i} \tag{20}$$

loading the capacitive center point is formed by segments of the phase currents in dependency on the switching states $s_i$ of the power transistors $T_i$. For the voltage shift of the center point there follows with $C_1 = C_2 = C$ (see Fig. 2):

$$\frac{du_M}{dt} = \frac{1}{2C} i_M. \tag{21}$$

For a clear description of the behavior in the following, a purely sinusoidal and symmetrical shape of the mains phase currents

$$\begin{aligned} i_{N,R} &= \hat{I}_N^* \cos(\varphi_N) \\ i_{N,S} &= \hat{I}_N^* \cos\left(\varphi_N - \frac{2\pi}{3}\right) \\ i_{N,T} &= \hat{I}_N^* \cos\left(\varphi_N + \frac{2\pi}{3}\right) \end{aligned} \tag{22}$$

and/or $i_{N,i} = i_{N,i}^*$ is assumed. Also, the analysis of the (stationary) operation is limited to an interval of the mains period $\varphi_N \in (-(\pi/6), +(\pi/6))$ and/or $i_{N,R} > 0, i_{N,S} < 0$, and $i_{N,T} < 0$ $(i_{N,R} \geq |i_{N,S}|, |i_{N,T}|)$. Due to the phase-symmetrical circuit structure, this includes the basic relationships within the entire mains period.

The center point currents $i_M$ [see (20)] resulting for the possible combinations of the phase switching functions $s_i$ (the different switching states of the converter, see Fig. 6) are given in Table I.

As described already in Section IV-A, a mutual influence of the phase current controllers is given due to the floating output

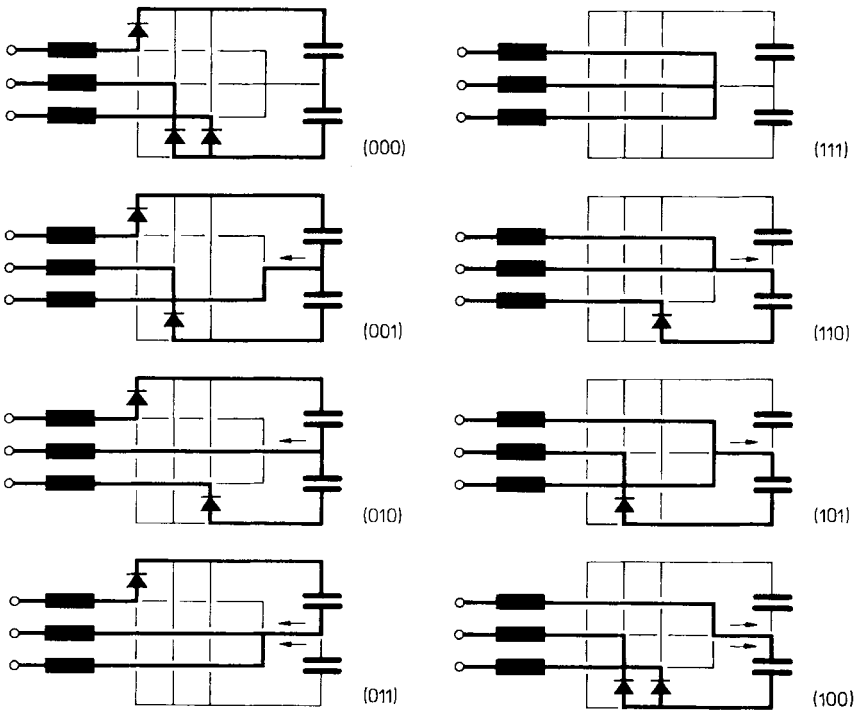



Fig. 6. Basis for the determination of the center point current $i_M$ in dependency on the converter switching state (marked by $(s_R, s_S, s_T)$) for $\varphi_N \in (-(\pi/6), +(\pi/6))$ and/or $i_{N,R} > 0, i_{N,S} < 0$, and $i_{N,T} < 0$ $(i_{N,R} \geq |i_{N,S}|, |i_{N,T}|)$.

voltage center point $M$ for independent hysteresis control of the phase currents; this leads to an arbitrary sequence and to a very variable duration of the single converter switching states $(s_R, s_S, s_T)$. It is clear from the weighting of the switching states regarding the influence of the center point potential (see Table I) that one cannot expect a time constant average value of the center point voltage $U_M$ (gained by averaging $u_M$ over the mains period). This is also true because, as a closer analysis shows, for hysteresis control of the phase currents, a positive feedback effect occurs; an unsymmetry $U_M$ of the output voltage leads to the occurrence of a current mean value (related to the fundamental period)

$$I_M = g_M U_M \qquad g_M > 0 \tag{23}$$

(being in a first approximation proportional to the unsymmetry $U_M$) increasing the unsymmetry. (The differential conductance $g_M > 0$ corresponds to the positive rate of rise of the characteristic $I_M = I_M\{U_M\}$ of the rectifier system in $U_M = 0$ (see Fig. 7(a) the derivation of which is explained in detail in [28].) Therefore, a symmetrical split of the output voltage can only be obtained by controlling the voltage $u_M$ via influencing the frequency and duration of the single switching states.

Because the converter switching state is derived directly from the difference of reference and actual values of the phase currents, the possibiltiy of control interaction is basically limited to a modification of the current reference value synthesis. The only degree of freedom existing here is by addition of a zero component

$$\begin{aligned} i_{N,R}^{*\prime} &= i_{N,R}^{*} + i_0 \\ i_{N,S}^{*\prime} &= i_{N,S}^{*} + i_0 \\ i_{N,T}^{*\prime} &= i_{N,T}^{*} + i_0 \end{aligned} \tag{24}$$

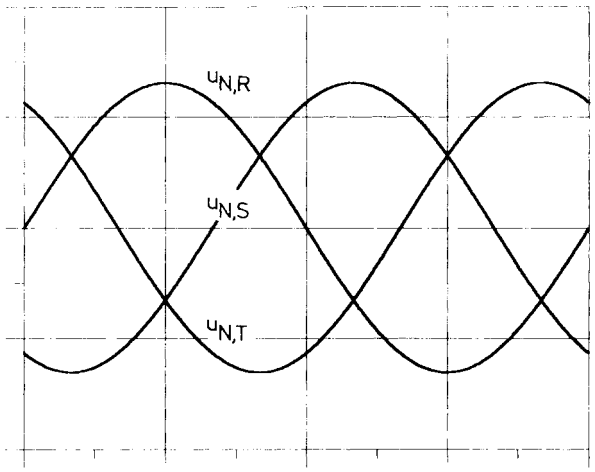
(of an offset $i_0$ equal for all phases) due to the amplitude $\hat{I}_N^*$ being fixed by the power to be delivered and by the sinusoidal shape required for low influence on the mains. The zero component $i_0$ cannot be set by the phase current controllers due to the floating mains star point $(i_{N,R} + i_{N,S} + i_{N,T} \equiv 0)$ and, therefore, does not lead to a direct influence on the mains current shape. However, it influences the frequency and duration of the switching states used for the control of the mains current and, therefore, also of the value of the center point current $i_M$.

According to (13) and (14), a time-constant positive value $i_0 = I_0 > 0$ in the angle interval $\varphi_U \in (-(\pi/6), +(\pi/6))$ considered leads to favoring of the switching states $s_R = 1, s_S = 0$ and $s_T = 0$, leading to a time average $I_M > 0$ (see Table I). For $I_0 < 0$ there follows in an analogous manner $I_M < 0$ [see Fig. 9(II)]. As shown in Fig. 3, with this, the quantity $i_0$ can be used directly for balancing of the output partial voltages.

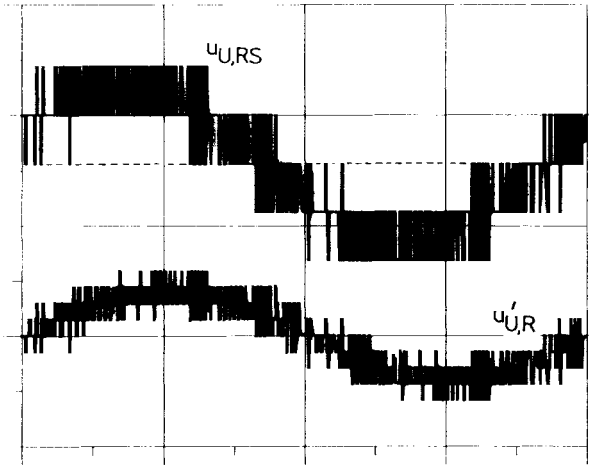
## V. Digital Simulation

The results of a digital simulation of the stationary operating behavior of the system are shown in Figs. 7–9. For the purpose of a clear representation of the conditions, for Figs. 7 and 8 we chose $L = 3$ mH and/or a mean switching frequency of only $f_P \approx 3.8$ kHz. On the contrary, for a practical system realization one would have to choose a switching frequency at least above the audible spectrum, e.g., $f = 38$ kHz and/or $L \approx 0.3$ mH. The simulation results shown in Fig. 9 are based on these parameter values.

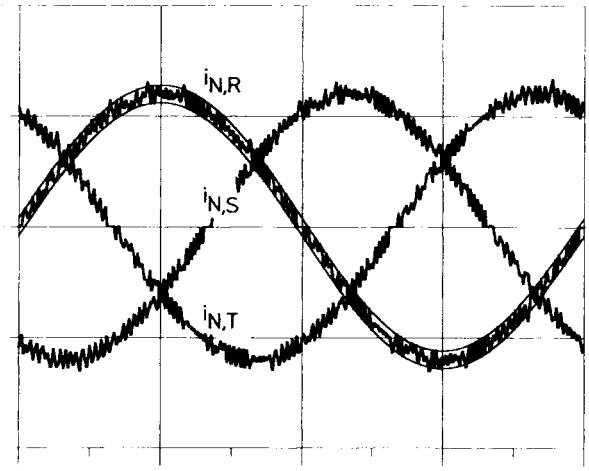
As Fig. 7(b) shows, the three-level characteristic of the bridge legs of the converter results in a very good approximation of the effective rectifier input voltage $u'_{U,i} = u_{U,i} - u_N$




(a)




(b)




(c)

Fig. 7. Digital simulation of a three-phase/switch/level unity power factor PWM rectifier. Representation for one mains period; hysteresis control of the phase currents. (a) Mains phase voltages $u_{N,(RST)}$ (related to the mains star point $N$, see Fig. 2), 250 V/div. (b) Line-to-line rectifier voltage $u_{U,RS} = u_{U,R} - u_{U,S}$ and phase voltage $u'_{U,R} = u_{U,R} - u_N$ determining the phase current $i_{N,R}$ in connection with $u_{N,R}$ [see (16)], 800 V/div. (c) Mains phase currents $i_{N,i}$, for phase $R$ the switching thresholds $i^*_{N,R} + h$ and $i^*_{N,R} - h$ of the hysteresis control are shown, 15 A/div. Parameters: $U_N = 230$ V (rms), $U_O = 700$ V, $\hat{I}^*_N = 18$ A, $h = 1.5$ A, $L = 3.0$ mH.

[see (16)] to the ideal sinusoidal form. Therefore, also for relatively low average switching frequency or low rated power of the inductances $L$, a low rms value of the current ripple is obtained.

By the signal shapes shown in Fig. 8, the considerations concerning the control of the output center point voltage $u_M$ via a shift by $I_0$ of the phase current reference values are proven. For a clear representation of the relationships, very large values $I_0$ are chosen (which are not characteristic for the, in reality, only low influence of the control). In general, the amount of the resulting center point current mean value $I_M$ is determined essentially by the ratio of the amplitude of the mains currents $\hat{I}_N$ and the hysteresis width $2h$ (see Fig. 9(II) and/or [28, Fig. 12]). Due to the then high gain

$$k_M = \frac{\Delta I_M}{\Delta I_0} \tag{25}$$

of the system to be controlled, the balancing of the output partial voltages is made possible by addition of an offset $I_0$ being small as compared to $h$.

As a fast Fourier transform (FFT), which is not discussed here for the sake of brevity, of various mains fundamental periods of the rectifier input current shape shows, and as is immediately clear from a relation of the quantities

$$I_0 \approx 0.01 \cdots 0.05h \tag{26}$$

$(h \approx 0.05 \cdots 0.1\hat{I}_{N,(1),\max})$ being typical for a practical system realization, the amplitudes and the spectral distribution of the current harmonics are only little influenced there. There do not occur low-frequency distortions of the mains current. The amplitudes of the even-order harmonics (which are caused by the unsymmetry due to the shift $i_0$ of the phase current reference values) remain limited to the values of neighboring odd harmonics.

Fig. 9(III) shows the shape of $u_M$ for an open and closed center point voltage control loop (where $G(s)$ is realized as a PI controller). $u_M$ is guided along $u^*_M = 0$ (the reference value), i.e., $u_{C,1} = u_{C,2}$ until the control loop is opened in $t_1$. If the control loop is interrupted ($i_0 = 0$ for $t \in [t_1, t_2]$), the center point potential shows (according to the considerations in Section IV-B) a shape corresponding to the step response of an integrator with positive feedback. According to Fig. 9(I), an increasing rise of the asymmetry is connected with a reduction of the positive feedback and, finally, with a sign inversion of $g_M$. In the case at hand, $g_M$ has negative values in the region $|U_M| = 50 \cdots 100$ V. Accordingly, there is inherent stability in this operating region. This can be seen in Fig. 9(III) by motion of $u_M$ toward the zero crossing of the characterisitc $I_M = I_M\{U_M\}$ defining a value $U_M \approx 80$ V. The control loop is closed again in $t_2$ and, due to proper dimensioning of $G(s)$, the asymmetry of $u_{C,1}$ and $u_{C,2}$ is being corrected without overshoot.

## VI. System Evaluation

For an evaluation of the proposed system, the characteristic current and voltage stresses on the devices are compared (see Table II) to those of a conventional two-level voltage dc-link PWM rectifier system shown in Fig. 10 (see e.g., Section

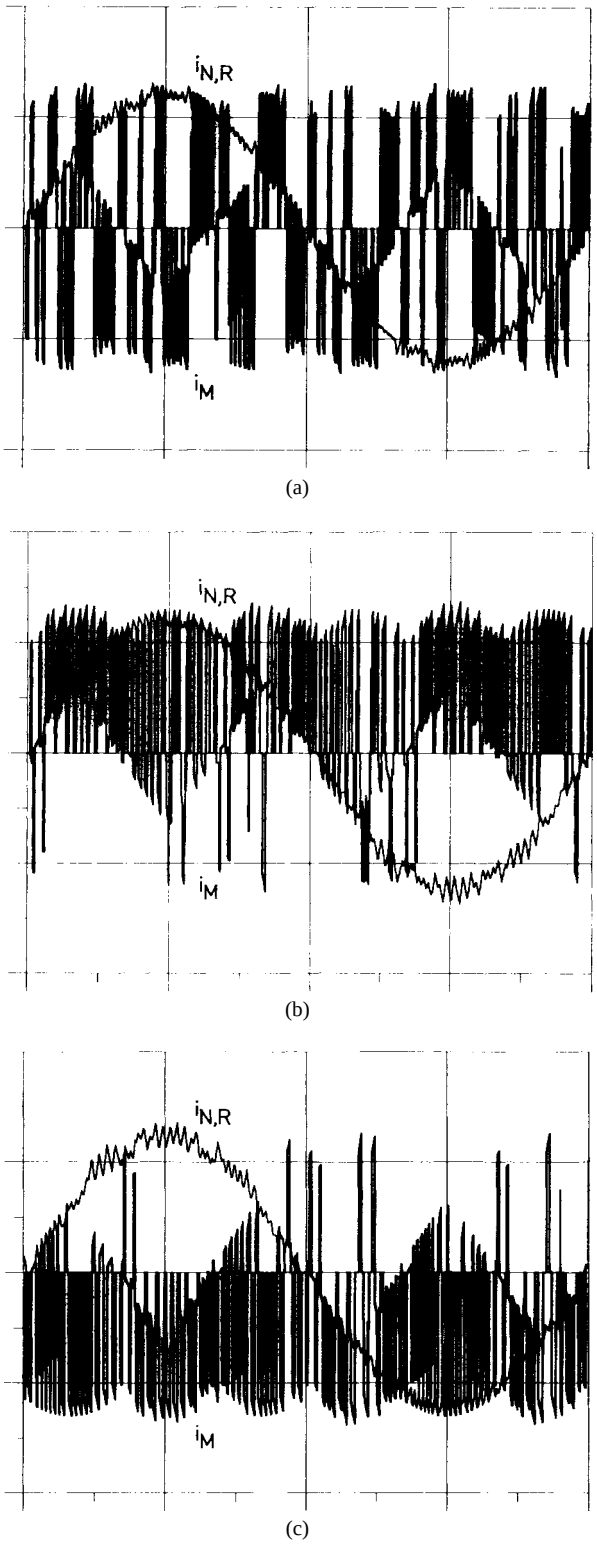



Fig. 8. Digital simulation of the function of balancing the output partial voltages $u_{C,1}$ and $u_{C,2}$ by addition of an offset $I_0$ to the reference values of the phase current hysteresis control (see Fig. 5). Representation of the mains phase current $i_{N,R}$ and of the current $i_M$ loading the center point [see Fig. 2 and (20)]; 15 A/div. (a) $I_0 = 0$ (no influence of the current control), $I_M = 0.16$ A ($I_M$ denotes the mean value of the center point current $i_M$ within one mains period). (b) $I_0 = +0.375$ A $(+\frac{1}{4}h), I_M = +6.1$ A. (c) $I_0 = -0.375$ A $(-\frac{1}{4}h), I_M = -6.0$ A. Parameters the same as for Fig. 7.

17-7 in [29] or [30]). Because this converter circuit is also incorporated into a comparison of concepts of converters with low effects on the mains in [31] and [32], there is also given a relation to other rectifier circuits.

There has to be pointed out, however, that the circuit shown in Fig. 10 allows (contrary to the circuit described in this paper) also an energy feedback from the output circuit into the mains. One also can say that it does not have a basic limitation of the phase angle region of the mains current. Furthermore, one has to mention that the control limit is not influenced by the phase difference of the fundamentals of the rectifier input voltage and of the mains current (see Section III-C). The system operating region for resistive mains load is defined by

$$u_K \leq \sqrt{M^2 - 1}. \tag{27}$$

For given input power (and equal rating of the series inductors $L$), this results in a minimum value of the dc-link voltage which is lower as compared to (9). Therefore, the comparison of the component stresses as given in the following has to be seen as making reference to a (general) evaluation basis and not as a direct comparison of the circuit concepts.

The characteristic component stresses are determined by digital simulation based on nominal values:

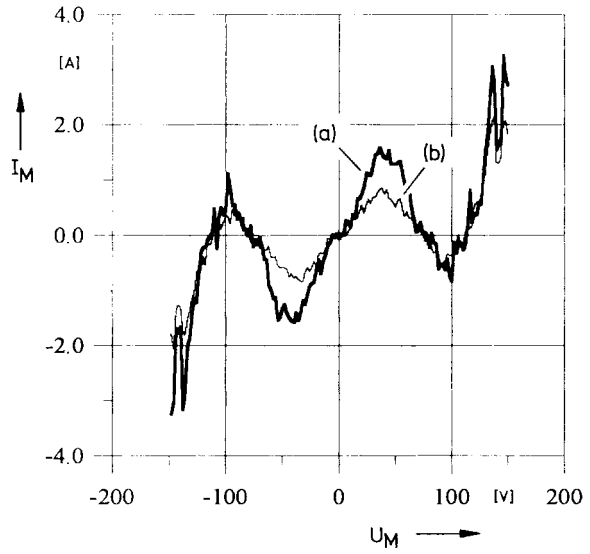
$$\begin{aligned} P_O &= 12.6 \text{ kW} \\ U_N &= 400 \text{ V}/230 \text{ V (rms)} \\ f_N &= 50 \text{ Hz} \\ U_O &= 700 \text{ V} \end{aligned} \tag{28}$$

as given for the development of a 60-V/200-A telecommunications power supply module intended to be used with the European low-voltage system. There, the control of the mains current is realized by hysteresis control, as described in Section IV-A. The phase current reference values are given proportional to the mains phase voltages [see (12)]. The efficiency of the dc/dc output stage of the module (the concept of which is laid out as an ac/dc–dc/dc converter) is estimated by $\eta_{\text{dc/dc}} = 0.95$. For the circuit parameters, we choose (as already mentioned in Section V):

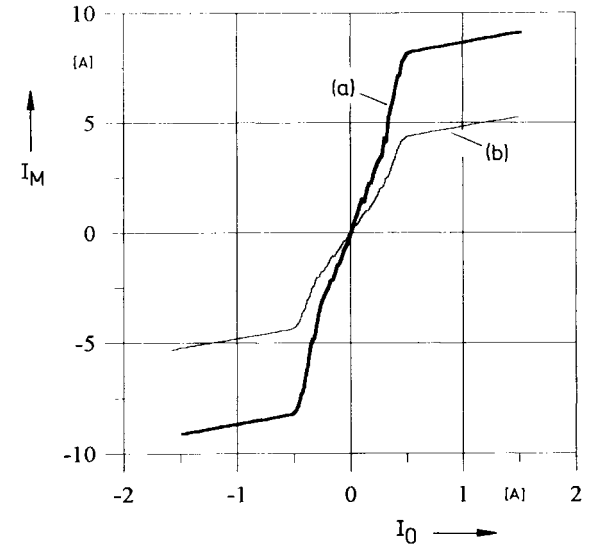
$$\begin{aligned} L &= 0.3 \text{ mH} \\ h &= 1.5 \text{ A}. \end{aligned} \tag{29}$$

As one can see from the comparison of the component stresses of the converter systems (see Table II), a significantly lower average switching frequency of the power transistors occurs for the three-phase/switch/level PWM (VIENNA) rectifier for equal hysteresis width and for approximately equal harmonic rms value $\Delta I_{N,\text{rms}}$ $(\Delta i_{N,i} = i^*_{N,i} - i_{N,i})$ of the mains current. This is obtained by the better approximation of an ideally sinusoidal shape of the rectifier input voltages due to the three-level characteristic. Therefore, for equal average switching frequency, one can reduce the value of $L$ as compared to a realization by a two-level PWM rectifier. Furthermore, this results in a higher power/volume ratio of the converter.

A further advantage of the three-level rectifier system consists in the cutting of the blocking voltage stresses (without considering switching overvoltages) of the power transistors and freewheeling diodes, $U_{T,\text{max},i}$ and $U_{D,\text{max},i}$ into one

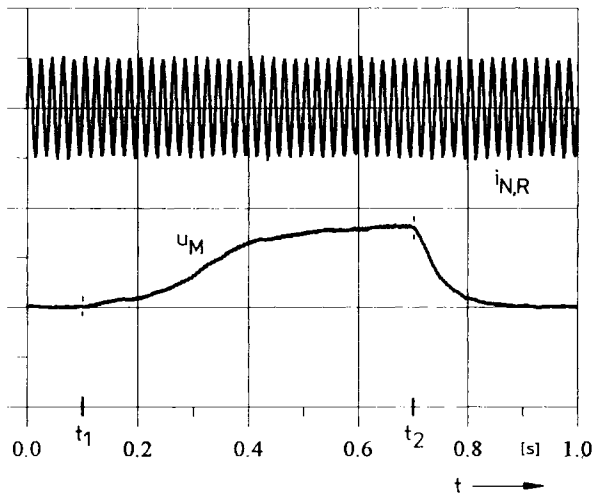



(I)




(II)

Fig. 9. For the control of the potential of the capacitive center point $M$ of the output voltage. (I) Dependency of the mean value $I_M$ (related to a mains period) of the center point current $i_M$ on the (mean) center point potential shift $U_M$; the characterisitc can be replaced in a first approximation by a straight line $I_M \approx g_M U_M$ in the vicinity of $U_M = 0$ ($U_M = 0$ corresponds to the reference value of the controller balancing the output partial voltages). (a) $\hat{I}_N^* = 18$ A, $g_M \approx 0.04\Omega^{-1}$. (b) $\hat{I}_N^* = 9$ A, $g_M \approx 0.02\Omega^{-1}$. (II) Control characteristic $I_M = I_M\{I_0\}$ of the rectifier system; (a) $\hat{I}_N^* = 18$ A, $k_M \approx 16$; (b) $\hat{I}_N^* = 9$ A, $k_M \approx 8$. For operating parameters of the system not specified, see Fig. 7.




(III)

Fig. 9. *(Continued.)* For the control of the potential of the capacitive center point $M$ of the output voltage. (III) Shape of $u_M$ (100 V/div) and $i_{N,R}$ (40 A/div) for open ($t \in [t_1, t_2]$) and closed center point voltage control loop ($\hat{I}_N^* = 18$ A, capacitance of the output capacitors $C_1 = C_2 = 2.0$ mF). For operating parameters of the system not specified, see Fig. 7.

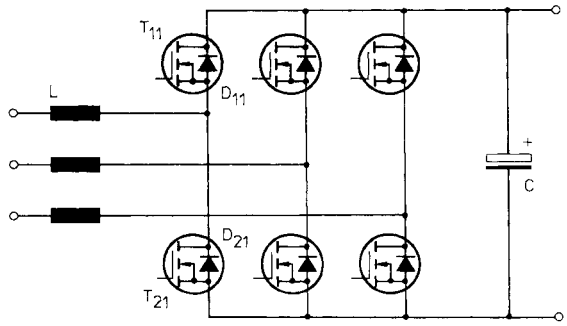



Fig. 10. Structure of the power circuit of a conventional three-phase six-switch *two-level* PWM rectifier system.

half. This allows the application of MOSFET's with lower blocking voltage and of diodes with lower reverse recovery time. With this, lower switching losses and lower transistor conduction losses (due to the lower on-resistance $R_{DS,\mathrm{on}}$ for lower blocking voltage) are obtained. This gives higher efficiency of the energy conversion.

Also, a comparison of the total volt-ampere rating $\Sigma U_{T,\max,i} I_{T,\max,i}, i = R,S,T$ ($I_{T,\max,i} = \hat{I}_{N,\max,i}$) of the transistors of the conventional system shows an advantage of the three-level converter; the two-level rectifier system requires a *four times* higher total volt-ampere rating of the power transistors.

If the two turn-off power semiconductors which are located in each of the three bridge legs of the conventional rectifier system (e.g., $T_{11}$ and $T_{21}$, see Fig. 10) are paralled in each phase and used for realization of the corresponding turn-off power switch of the three-level rectifier, we have an approximately equal current stress $I_{T,\mathrm{rms}}$ for the single transistors in both cases. Also, regarding the rms values $I_{N,\mathrm{rms}}$ of the mains currents, the stresses on the diodes carrying the power flow and the stresses on the output capacitors, there are only minor differences between both systems. This checks the considerations concerning low conduction losses of the proposed system.

## VII. Conclusions

Based on the basic structure of a three-phase ac/dc boost converter, in this paper, the topology of a three-phase/switch/level PWM rectifier is developed. Also, a method for controlling the output voltage and the mains current and for balancing of the partial output voltages is given.

TABLE II
COMPARISON OF THE QUANTITIES CHARACTERIZING THE COMPONENT STRESS OF A THREE-PHASE/SWITCH/LEVEL PWM RECTIFIER SYSTEM [SEE FIG. 2(b)] AND OF A CONVENTIONAL THREE-PHASE SIX-SWITCH TWO-LEVEL PWM RECTIFIER SYSTEM (SEE FIG. 10); THE STRESSES ON THE DIODES GIVEN FOR THE PROPOSED SYSTEM ARE RELATED TO THE FREEWHEELING DIODES $D_{1j}$ AND $D_{2j}$; FOR THE STRESSES ON THE DIODES $D_i$ (WHICH CAN BE REALIZED BY CONVENTIONAL RECTIFIER DIODES) OF THE BIDIRECTIONAL BIPOLAR SWITCHES WE WANT TO REFER TO FIG. 7 IN [33]; OPERATING PARAMETERS: $P_O = 12.6$ kW, $\eta_{\mathrm{ac/dc}} \approx 0.96, U_O = 700$ V, $U_N = 230$ V (rms), $L = 0.3$ mH, $h = 1.5$ A ($\approx 0.05 \hat{I}_{N,(1)}$)

| Characteristic Value | Proposed System | Conventional System |
|---|---|---|
| $I_{N,(1),\mathrm{rms}}$ [A] | 19.0 | 19.0 |
| $I_{N,\mathrm{max,i}}$ [A] | 29.9 | 29.9 |
| $\Delta I_{N,\mathrm{rms}}$ [A] | 0.62 | 0.65 |
| $I_{T,\mathrm{avg}}$ [A] | 5.1 | 1.3 |
| $I_{T,\mathrm{rms}}$ [A] | 8.6 | 4.5 |
| $U_{T,\mathrm{max,i}}$ [V] | 350 | 700 |
| $I_{D,\mathrm{avg}}$ [A] | 6.0 | 7.3 |
| $I_{D,\mathrm{rms}}$ [A] | 11.5 | 12.4 |
| $U_{D,\mathrm{max,i}}$ [V] | 350 | 700 |
| $I_{C,\mathrm{rms}}$ [A] | 9.3 | 9.5 |
| $f_{P,\mathrm{avg}}$ [kHz] | 33.3 | 57.3 |

In the following, the advantages and disadvantages being relevant for a qualitative evaluation of the converter concept (as can be used, e.g., for a concept study) are summarized briefly.

Advantages are the following:

- simple structure of power and control circuit, only one power transistor per phase (low control/driving effort);
- possibility of realization of the control circuit by analog techniques—high dynamics, avoidance of the development effort associated with the application of microprocessor control;
- low harmonics rms value of the mains current due to inclusion of the center point of the output voltage into the synthesis of the rectifier input phase voltages (three-level characteristic); for hysteresis control of the input currents: distribution of the power harmonics over a wide frequency range due to time-varying switching frequency [34]—as compared to constant switching frequency a lower filtering effort for compliance to the regulations concerning conducted EMI [35] is required;
- low blocking voltage stress on the power semiconductors (possibility of application of low-voltage MOSFET's and ultrafast recovery diodes even for high dc-link voltage, e.g., for an output voltage of $U_O = 700$ V valves with a blocking voltage capability $\mathrm{V_{DSS}} = \mathrm{V_{RRM}} = 500 \cdots 600$ V can be applied—low transistor conduction losses and low switching losses (the blocking behavior of the diodes has an essential influence on the resulting switching losses [36]); *remark:* the diodes $D_i$ of the bidirectional bipolar switching elements [see Fig. 2(b)] are not commutated with switching frequency and, therefore, can be realized by conventional rectifier diodes;
- low nominal power of the inductances connected in series on the mains side (high dynamics of the dc-link voltage control and/or reduction of the dc-link capacitance required for buffering of load steps)—high power/volume and/or power/weight ratio of the converter;
- as compared to bridge circuits: 1) significantly higher utilization of the power transistors (conduction of each transistor during positive *and* negative half period of the related phase current); 2) for realization of the power transistors by power MOSFET's no current flow occurs through the parasitic internal diodes of the devices and/or a possible conduction of these diodes doesn't have to be suppressed by diodes lying in series with the power transistors (see [37, Fig. 1]); 3) higher reliability of operation—in the case of a control malfunction of a power transistor, no short circuit of the output voltage occurs; and 4) lower common-mode EMI (lower EMI filter requirement);
- possibiliy of distributing the load to the positive and negative output partial voltages; there, $u_{C,1}$ and $u_{C,2}$ can be loaded very much unsymmetrically because, for appropriate system control, one obtains a high current handling capability of the output voltage center point $M$ [38];
- possibility of operating the system with inductive mains phase current angle allows a partial compensation of the capacitive reactive power caused by an EMI filter; furthermore, this gives a degree of freedom for an optimization of the mains filter (see [39, Figs. 7, 8]).

Disadvantages are the following:

- limitation of the system operating region concerning the phase angle of the mains current and voltage transformation ratio $M$ (see Section III-C), especially limitation to unidirectional energy conversion;
- relatively high circuit effort for the realization of the converter by discrete devices; this can be avoided by application of a power module which integrates a bridge leg of the system (e.g., the module IXYS VUM25-E has been designed for $U_N = 230$ V and $U_O = 700$ V and permits the realization of a rectifier system with $P_O = 15$ kW, $f_P = 50$ kHz und $\eta_{\mathrm{ac/dc}} = 0.96$ [33]);
- for hysteresis control of the input currents by independent phase controllers: current control error possible in the order of magnitude of twice the hysteresis width; occurrance of limit cycles [27]—nonoptimal utilization of the converter pulse frequency.

In order to minimize the effort regarding the circuit technology and/or of development, system and fabrication costs in the present case a simple control method (i.e., hysteresis control of the mains currents, which can be realized by analog means) has been selected. Naturally, this does not lead to a minimization of the harmonics rms value of the mains current or of the switching frequency. The possibility of a relevant optimization (described in the literature for three-level PWM *inverters* [40]–[42]) is only given when the converter control

unit is realized by digital means, e.g., when a signal processor system is used. This is presently the topic of further research.

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