99% Efficient Three-Phase Buck-Type SiC MOSFET PFC Rectifier Minimizing Life Cycle Cost in DC Data Centers

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99% Efficient Three-Phase Buck-Type SiC MOSFET PFC Rectifier Minimizing Life Cycle Cost in DC Data Centers

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Abstract—Due to the increasing power consumption of data centers, efficient dc power distribution systems have become an important topic in research and industry over the last years. Furthermore the power consumed by data centers is an economic factor, which implies that all parts of the distribution system should be designed to minimize the life cycle cost, i.e. the sum of first cost and the cost of dissipation. This paper analyzes a three-phase buck-type PFC rectifier with integrated active 3rd harmonic current injection for dc distribution systems. Switching frequency, chip area and magnetic components are selected based on a life cycle cost optimization, showing that a peak efficiency of 99% is technically and economically feasible with state-of-the-art SiC MOSFETs and magnetic components. Measurements taken on an 8 kW, 4 kW dm⁻³ hardware prototype demonstrate the validity and feasibility of the design.

I. INTRODUCTION

Information and communication technology equipment has become a significant consumer of electric power in recent years. In 2007, for example, the related annual consumption in Germany alone was 55 TWh which equaled approximately 10% of the countries total consumption, where the annual power consumption of data centers located in Germany is approximately constant at ≈ 10 TWh since 2008 [1].

Therefore, the cost for electric energy is becoming a significant economic factor. Given some basic economic parameters the capital-equivalent worth of a continuously dissipated watt of ac power can be estimated. In 2008 the authors of [2] estimate an average value of $14 per watt for the US market and 15 years of service life, which implies that up to $14 could be invested now in order to reduce the equipment’s power consumption by one watt over the next 15 years. Even though the prices for electric power show a considerable geographical variation (approximately a factor of 5 in the US), the authors conclude that the cost of dissipation significantly overshadows the first cost for telecom power supplies.

In conventional data centers using ac distribution systems, as shown in Fig. 1a), up to 50% of the total energy consumed is used for air conditioning, distribution and conversion losses [3]. Compared to this, distribution systems based on a dc bus with a nominal voltage of 380 V offer significantly higher efficiency, improved reliability and reduced capital cost and floor space, cf. Fig. 1b) [4]. Furthermore they allow a direct connection of lead acid batteries, consisting of 168 cells connected in series, with a typical floating cell voltage of ≈ 2.26 V, which results in a nominal bus voltage of 380 V. Accordingly, standards and components for dc distribution systems have been developed in recent years [5, 6].

Normally a boost-type power factor correction (PFC) stage is used to convert the 400 Vac mains into a dc voltage which is higher than the full-wave rectified ac input voltage, typically in the range of 700 V to 800 V. A subsequent buck converter is then required to connect the PFC output to the dc distribution bus. This configuration is also used for fast chargers of Electric Vehicle batteries which are powered from the three-phase ac mains [7]. As an alternative, a single-stage conversion between the three-phase mains and a dc bus with lower voltage can be achieved with buck-type PFC converters, like the SWISS Rectifier, the six-switch buck rectifier or Integrated Active Filter rectifier [8, 9].

A. Buck-Type PFC Rectifiers

In Fig. 2a) the basic schematic of the six-switch rectifier, consisting of an ac input filter, six fully controllable (i.e. reverse blocking) switches and a dc output filter is shown. An additional diode D̄ho can be used to lower the conduction losses in the free wheeling state. Note that similar PWM rectifiers, implemented with thyristors, have been used as early as 1979 [10]. Several modifications of the basic circuit topology, reducing the number of active switches, reducing conduction losses and for buck-boost operation have been described [11–13].

An alternative buck-type PFC converter, called SWISS rectifier, is shown in Fig. 2b). It consists of an ac input filter, an Input Voltage Selector (IVS) built of a line-commutated full-wave diode rectifier D̄k, D̄b, D̄c ∈ {a, b, c} and three four-quadrant switches S̄k and two buck converters which

Fig. 1. Data center power distribution concepts: a) Conventional 400 Vac distribution, using an ac Uninterruptible Power Supply (UPS). Similar concepts can be used with 480 Vac. b) Facility level dc distribution system based on a 380 Vdc bus which allows a direct connection of backup batteries [3].
provide a constant dc output voltage. Note that the IVS switches and diodes are commutated at mains frequency only which implies that almost no switching losses occur in the IVS. This allows the usage of rectifier diodes D_{ink}, D_{dk} which are optimized for a low forward voltage drop. Two additional capacitors C_{ij}' can be used to shorten the commutation paths of the dc-dc converters.

The circuit topology of the Integrated Active Filter (IAF) buck-type PFC rectifier, shown in Fig. 2c), was first introduced in [14] for three-phase solar inverters. A similar circuit was also proposed for drive systems with small dc-link capacitors [15]. Three major blocks can be identified in the IAF schematic: an Input Voltage Selector which is identical to the SWISS Rectifier, a current injection circuit and a dc-dc buck converter S_x, D_x, L_o which provides the constant dc output voltage u_{om}. Typically a small capacitor C_{ij}' is required to ensure a valid conduction path during the commutation of S_{xy}, S_{yz} and S_{x}.

For this paper, the Integrated Active Filter buck-type PFC rectifier was selected as starting point for further analysis in Section II as only two line-commutated diodes D_{ink}, D_{dk} and one power transistor S_k are in its main conduction path [8]. Using the capital equivalent worth of a watt and component cost models a non-isolated 8kW PFC rectifier for 380 Vdc distribution systems is designed in Section III. This allows selecting cost optimal components such as semiconductors, inductors and transformers achieving an economically optimal converter which minimizes life cycle cost, i.e. the sum of first cost of the converter hardware and the cost of dissipation during the service life. Measurements taken on a hardware prototype are presented in Section IV.

### II. CIRCUIT TOPOLOGY

Simulation results for a 8kW IAF buck-type PFC system (cf. Fig. 2c) are shown in Fig. 3, for the system specifications given in Table I. In the IAF, the current injection circuit and the buck converter can be analyzed, optimized and operated almost independently of each other. As the dc output is provided by the buck converter (S_x, D_x, L_o), the output current i_o and voltage u_{om} can be controlled independently of the injection circuit. This can be seen from the simulation results in Fig. 3: During ωt < 180° the current injection circuit is turned off, i.e. i_{inj} = 0. As the buck converter creates a constant output current i_o, it consumes constant power from the ac input. Hence non-sinusoidal ac input currents i_{a,b,c} result and only two ac input phases i_{a,b,c} conduct current at a time.

For ωt > 180° the injection circuit is used to change the current i_{inj} which is proportional to the voltage u_{inj}:

\[
i_{inj}(\omega t) = -\bar{I}_i \frac{u_{inj}(\omega t)}{U_1}
\]

where \bar{I}_i is the peak value of the rectifier’s ac input current and U_1 is the ac phase-to-neutral voltage amplitude. This results in sinusoidal ac input currents as shown in Fig. 3.

![Fig. 2. Three-phase buck-type PFC rectifier topologies: a) Conventional six-switch rectifier consisting of an input filter, six reverse blocking switches and a dc link inductor L. An additional free wheeling diode D_{ink} can be used to lower the conduction losses. b) SWISS rectifier consisting of an input filter, an Input Voltage Selector (IVS) commutated at mains frequency and two buck converters. c) Integrated Active Filter rectifier (IAF), using the same input stage as the SWISS rectifier, combined with a single buck converter providing the output current i_o and a dedicated current injection converter which serves as active harmonic filter for achieving sinusoidal input currents.

![Table I: Converter Specifications](Table I: Converter Specifications)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (Line-to-Neutral)</td>
<td>U_1 = 230 V rms</td>
</tr>
<tr>
<td>Input Frequency</td>
<td>ω_1 = 2π 50 Hz</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>f_s = 27 kHz</td>
</tr>
<tr>
<td>Nominal Output Voltage</td>
<td>U_{om} = 400 V</td>
</tr>
<tr>
<td>Nominal Output Power</td>
<td>P_o = 8 kW</td>
</tr>
</tbody>
</table>
A more detailed description of the modulation and control strategy can be found in [8].

A. Input Voltage Selector

As described above, the IAF rectifier uses an Input Voltage Selector, which connects each ac input phase a, b, c to either node x, y or z. This implies that the voltages \( u_{aN}, u_{yN} \) and \( u_{zN} \) are piecewise sinusoidal, which allows to move the ac filter capacitors \( C_{a,b,c} \) from nodes a, b, c to nodes x, y, z as shown in Fig. 4. This shortens the commutation paths of the buck converter and the injection switches. Additionally the ripple of the diode bridge currents \( i_x \) and \( i_z \) reduces which reduces the conduction losses in full-wave diode bridge \( D_{sk} \) [16].

B. Buck Converter

It can be seen in Fig. 2c) that the buck converter’s input is connected to \( u_{aN} \) which is a six-pulse shaped voltage provided by the IVS’ full bridge rectifier, cf. Fig. 3. Neglecting any voltage drops across the semiconductors and inductors, the dc output voltage \( u_{pn} \) can be expressed as:

\[
  u_{pn} = \frac{3}{2} \hat{U}_1 M \quad M \in [0,1]
\]  

where \( \hat{U}_1 \) is the ac phase-to-neutral voltage amplitude and \( M \) is the converter’s modulation index. Note that this relationship is valid for all three buck-type topologies shown in Fig. 2 [8].

A small distortion of the output current occurs at every 60° sector of the ac input voltage, i.e. at the intersection of two phase voltages \( u_{a,b,c} \). This is most likely due to the switching frequency ripple of the filter capacitor voltages \( u_{aN}, u_{yN}, u_{zN} \) as similar disturbances exist in the SWISS rectifier [16].

If a conventional single-phase buck converter is used as shown in Fig. 2c) a discontinuous input current \( \dot{i}_x' \) results which causes a switching frequency voltage ripple across the input filter capacitors \( C_{a,b,c} \). As these capacitors are connected to the three-phase ac input of the converter they generate reactive power and hence reduce the rectifiers power factor. Therefore, the reactive power is typically limited to 5% to 10% of the converter’s active power rating.

C. Interleaved Buck Converter

In order to reduce the input current ripple and hence the electromagnetic noise emission of the rectifier, an interleaved buck converter can be used, as shown in Fig. 4. By modulating the switches \( S_{a1} \) and \( S_{a2} \) with 180° phase shifted PWM signals the peak-to-peak ripple in \( \dot{i}_x' \) is reduced by approximately a factor of two and the ripple frequency is twice the switching frequency due to the cancellation of harmonics.

The dc output filter for the interleaved buck converter can be implemented by a combination of a close-coupled inter-cell transformer (ICT) and single inductor \( L_o \).
As described in [2] the capital equivalent worth of one watt of continuous dissipation can be used to select components in order to minimize the total life cycle cost. Combined with component cost models, the switching frequency, semiconductors and magnetic components are selected to achieve minimal life cycle cost for a given service life time assuming continuous operation at rated power [20]. A hard switching converter design was chosen for the analysis because of the simpler modulation and control, the lower noise emission, the lower peak and rms currents in the switches and magnetics and the comparatively low switching losses of modern SiC semiconductor devices.

A calculation example for the input voltage selector diodes D_{S1}, D_{S2} is shown in Fig. 5, where a capital equivalent worth of \( \gamma = \text{EUR 0.12 per kW h} \) (approximately USD 0.13 at time of publication) is assumed. Neglecting switching losses in the IVS, the device losses can be directly determined from the rms and average currents found by numerical simulation, resulting in \( I_{\text{rms}} = 8.1 \text{ A} \) and \( I_{\text{avg}} = 4.6 \text{ A} \) for an 8 kW system. Assuming a service life time of 10 years or more, a SiC MOSFET with a high initial cost of approximately EUR 30 and low on-state resistance achieves the same or lower life cycle cost than conventional Si diodes with an initial cost of EUR 2.6. The same holds for a parallel connection of two SiC MOSFETs with a first cost of approximately EUR 8. Note that all devices are operated far below their thermal limits, 1.7 W of conduction losses result for the SiC MOSFETs, \( \approx 4 \text{ W} \) for the Si diodes and Si MOSFETs while all devices are rated for more than 100 W of continuous power dissipation. Therefore the full wave rectifier in the IVS is implemented with SiC MOSFETs operated as synchronous rectifiers as shown in Fig. 4.

### A. Minimizing Life Cycle Cost

The life cycle cost shown in Fig. 5 is based on a selection of standard semiconductor devices. Using more than one device in parallel reduces the total on-state resistance \( R_{\text{ds.on}} \) of MOSFETs or the bulk resistances \( r_b \) of diodes which lowers the conduction losses. This reduces the cost of dissipation during system operation, but increases the first cost as more devices are used. This implies that the resulting life cycle cost is a function of the number of devices used in parallel. For a MOSFET continuously conducting the current \( I_{\text{rms}} \) for the run time \( t_r \) without switching losses the corresponding LCC \( \Lambda \) can be expressed as:

\[
\Lambda_M(n) = \gamma R_{\text{ds.on}}^2 \frac{I_{\text{rms}}^2}{n} t_r + \sigma_M n \ ,
\]

where \( \sigma_M \) is the cost of a single MOSFET device with an on-state resistance \( R_{\text{ds.on}} \) and \( n \) is the number of devices connected in parallel. A plot of the resulting values for \( t_r = 10 \text{ years} \) and a SiC MOSFET with \( R_{\text{ds.on}} = 96 \text{ m\Omega} \) and a cost of EUR 7.14 is considered as unit device together with a capital equivalent worth of \( \gamma = \text{EUR 0.12 per kW h} \) and a run time of \( t_r = 10 \text{ years} \).

\[
\begin{align*}
  n_{\text{opt}} &= \sqrt[1]{\gamma \ t_r R_{\text{ds.on}} I_{\text{rms}}} \ ,
  \\
  \Gamma_M &= \sqrt[1]{\gamma \ t_r R \sigma_M I_{\text{rms}}} \ ,
  \\
  \Lambda_M &= \Gamma_M + \sigma_M n_{\text{opt}} = 2 \sqrt[1]{\gamma \ t_r R \sigma_M I_{\text{rms}}} \ .
\end{align*}
\]

This implies that \( n \) is not a free parameter of a converter design if LCC is considered. For a given run time \( t_r \) an optimal \( n \) exists which corresponds to an optimal \( R_{\text{ds.on}} \).

Note that a certain minimum \( n_{\text{min}} \) exists due to the thermal limits of the device and the cooling system as indicated in Fig. 6. However, even for short run times of \( t_r \approx 1 \text{ year} \) the optimum \( n \) is typically larger than \( n_{\text{min}} \). Furthermore \( n \) does not necessarily have to be an integer number as semiconductor devices are usually available in a range of different chip sizes and hence \( R_{\text{ds.on}} \) values in the same package. As the obtained LCC function \( \Lambda(n) \) is flat around the optimum (cf. Fig. 6) one or more devices suitable for an implementation can typically be found.
This optimization can be extended from MOSFETs to diodes modeled by a constant forward voltage drop $U_f$ connected in series with a bulk resistance $r_b$. In this case the optimal number of diodes connected in parallel does not depend on $U_f$, however the losses and hence the cost of dissipation $\Gamma$ increases. An example calculation for different run times is shown in Fig. 7 where a 96 mΩ Si MOSFET and Si diode with $U_f \approx 0.74$ A and $r_b = 4$ mΩ are considered as unit elements. For both, MOSFETs and diodes the optimal $n$ increases proportional to $\sqrt{t_r}$, however for Si diodes the resulting losses show little variation due to $U_f$. As the first cost of the considered diode is $\approx 6$ times lower than the MOSFET’s the Si diodes achieve lower LCC for small $t_r$ while the SiC MOSFET achieves lower LCC for $t_r \geq 12.5$ years.

**B. Global Optimization Algorithm**

The algorithm outlined above can also be extended to include switching losses of the semiconductors and to magnetic components. The basic optimization procedure for a full rectifier system then works by sweeping over all relevant switching frequencies $f_{sw}$ and considered run times $t_r$. For each tuple $(f_{sw}, t_r)$ and all components $k$ of the system an optimal relative size $n_{k,opt}$ can be determined which achieves minimal life cycle cost $\Lambda_{k,opt}$ for component $k$. This implies that all components (e.g. switches, inductors, etc.) can be designed independently of each other which simplifies the optimization procedure. Once all components have been selected, their life cycle costs can be summed up which yields the system’s LCC for the considered $(f_{sw}, t_r)$:

$$\Lambda_{sys}(f_{sw}, t_r) = \sum_k \Lambda_{k,opt}(f_{sw}, t_r) \quad (7)$$

Once all designs have been calculated the switching frequency achieving lowest overall LCC is selected for each $t_r$, considered in the analysis:

$$\Lambda_{sys,opt}(t_r) = \min_{f_{sw}} \Lambda_{sys}(f_{sw}, t_r) \quad (8)$$

**C. Semiconductors**

As shown in Fig. 5 SiC MOSFETs achieve similar life cycle cost as Si devices for a run time of approximately 10 years if only conduction losses are considered. This implies that SiC MOSFETs clearly outperform Si devices for the hard switching elements $S_{12}^y$, $S_{13}$ and $S_{12}^y$. Therefore, SiC MOSFETs were considered for the IVS components and active switches in the buck converter and the current injection circuit. SiC Schottky diodes are considered for the buck converter free wheeling diodes $D_{12}^y$.

**D. Magnetic Components**

The dimensioning of magnetic components is performed with a similar algorithm: for a given switching frequency the current and voltage stresses created by the converter can be determined. For a given core material, shape and size the optimal number of turns, which minimizes the sum of core and winding losses, can then be found by numerical optimization methods. Using the losses and cost models for core and winding materials the inductor’s life cycle cost can
be calculated, which allows the selection of an optimal core size achieving minimal LCC for the given design point.

Note that different core and winding materials can only be compared at the full system level as the resulting losses depend strongly on design parameters such as the switching frequency. Ferrites, for example, typically feature lower core losses but also lower saturation flux densities than tape wound cores which makes ferrite more suited for higher switching frequencies. In this paper amorphous and nanocrystalline tape wound cores with helical windings made from rectangular wire as well as ferrite cores with solid round wire have been considered.

E. Auxiliary Components

The losses, volume and cost of other components, such as gate drive circuits, DSP/FPGA, capacitors, PCBs, heat sinks, fans, EMI filter, etc. have to be considered as well. While their contribution to the overall converter volume, and life cycle cost can be significant, they are almost independent of the design point in the considered application. Therefore auxiliary components have been considered in the design but were not part of the optimization.

F. Optimization Results

Fig. 8 shows the achievable minimal life cycle cost \( \Lambda_{\text{sys, opt}}(t_r) \) and the resulting first cost \( \Sigma_{\text{sys, opt}}(t_r) \) as a function of run time as calculated by the optimization outlined above. It can be seen that the first cost of the optimal systems is less than 30% of the total life cycle cost for a run time of 10 years or more. Furthermore, the life cycle cost is comparable for all three core materials considered in the optimization. Designs using amorphous cores are expected to have slightly higher LCC than systems with nanocrystalline or ferrite cores, which is due to the higher core losses of amorphous materials.

However, the volumes and switching frequencies of the designed converters differ significantly as shown in Fig. 9, the resulting efficiency as function of \( t_r \) is shown in Fig. 10. For short run times (\( \leq 2 \) years) converters with high switching frequencies and high power densities achieve minimal LCC as opposed to long run times (\( \geq 10 \) years) where designs with approximately half the switching frequency, twice the volume and half the losses result. Furthermore, these results show that very high efficiencies of up to 99% are economically feasible with available state-of-the-art SiC switches and core materials. Note that three-phase rectifiers based on Si and SiC MOSFETs with slightly lower efficiencies have been reported in the literature [21, 22], however without considering cost.

G. Selected Design

Based on the numerical optimization results the design point with \( t_r = 10 \) years, \( f_{sw} = 27 \) kHz, a power density of 4.0 kW dm\(^{-3}\) and an efficiency of 99% was selected to implement a hardware prototype. FINEMET nanocrystalline cores with helical windings (cf. Fig. 11) are used as they achieve considerably higher power density compared to designs based on ferrite. Detailed design results are shown in Fig. 12: for systems with a run time of 10 years or more, it can be seen that the semiconductors and heat sinks contribute about half of the first cost, life cycle cost and losses, but only about 10% to 20% of the total volume. Furthermore, the auxiliary components, such as PCBs, gate drivers, FPGA/DSP etc. have a significant contribution to both first cost and life cycle cost which implies that they cannot be neglected in the design process.

IV. HARDWARE PROTOTYPE

Using the optimization results presented in the previous chapter an 8 kW, prototype rectifier with a switching frequency of \( f_{sw} = 27 \) kHz, according to the specifications given in Table I, was implemented. A picture of the hardware is shown in Fig. 13.

A more detailed distribution of the calculated component losses for the implemented prototype at nominal operating conditions and the corresponding component volumes are shown in Fig. 14. About 50% of the total losses occur...
in the semiconductors of which approximately one third are switching losses. Core and winding losses in the main magnetic components $L_3$, ICT and $L_{int}$ account for $\approx 22\%$ of the total losses. The remaining $28\%$ occur in the EMI filter, the PCB tracks, and other elements such as fans, gate drivers, FPGA, current sensors etc. Measurement results of the prototype converter are presented in the following.

A. AC Input Currents

In Fig. 15 measurement results of the prototype rectifier operated at full load and nominal input voltage are shown. Sinusoidal input currents with slight distortions at the mains voltage sector boundaries result as expected from simulation.

B. Efficiency

A comparison of the rectifier’s calculated and measured efficiency as a function of dc output power is shown in Fig. 16. The solid lines show the calculated efficiency for 400 V and 380 V output voltage, while the round and triangular markers show measurements taken with a Yokogawa WT 3000 power analyzer. Additionally three efficiency measurements were taken based on a direct measurement of the converter’s losses using a calorimeter which closely match the values obtained by the electrical measurement.

V. Conclusion

This paper describes a life cycle cost driven optimization process were not only the first cost of a converter, but also the capital equivalent worth of the energy dissipated during the system’s service life is considered. This allows the selection of optimal components, such as switches, inductors, transformers, etc. which achieve minimal cost for a given application, run time and switching frequency. By sweeping over a range of suitable switching frequencies a cost optimal converter system can then be found.
As an example an 8kW buck-type three-phase interleaved Integrated Active Filter rectifier for 380 V dc distribution systems in data center and telecommunication applications is designed. Using state-of-the-art SiC MOSFETs and nanocrystalline cores a design with a power density of 4kW dm⁻³ and an efficiency of 99% results. Measurement results taken on a hardware prototype verify the validity of the employed models.

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