Center-Point Voltage Balancing of Hysteresis Current Controlled Three-Level PWM Rectifiers

Luca Dalessandro, Member, IEEE, Simon D. Round, Senior Member, IEEE, and Johann W. Kolar, Senior Member, IEEE

Abstract—The output center-point voltage of a hysteresis current-controlled three-level, unidirectional PWM rectifier is not naturally stable. This paper shows that the balancing of the center-point voltage can be realized by adding an offset to the input current-reference and that this offset results in a change of the relative on-times of the redundant switching states. The space-vector representation of the input rectifier voltage and current is used to help explain the effect of the current-offset injection on the output center-point voltage. The influence of the offset-current injection on the mains currents as well as the control and center-point characteristics are analyzed and verified by measurements. Finally, the design of the center-point controller is presented and its dynamic performance experimentally demonstrated.

Index Terms—Center point voltage control, hysteresis current control, three-phase three-level rectifiers.

I. INTRODUCTION

The three-phase, current-controlled, voltage-source, PWM rectifier has found extensive application as the front-end stage in ac drives [1], [2], in distributed power systems [3], as the input power-supply for welding processes [4], and within more-electric aircraft [5]. This is due to several advantages such as:

1) regulation of input power factor to unity;
2) low harmonic distortion of line current;
3) adjustment and stabilization of dc-link voltage.

Three-phase PWM rectifiers can be implemented using a six-switch active rectifier topology, or with star or delta connections of single-phase PFCs [6], [7]. Three-level rectifier topologies (see one example in Fig. 1) have further advantages compared to the conventional two-level topologies in terms of lower blocking voltage across the power switches and reduced input current ripple. However, the balancing of the output capacitors voltages has to be ensured in order to prevent over-voltage stress across the semiconductors and the output capacitors and to avoid low-frequency harmonics in the input rectifier voltage [8]–[11].

The problem of controlling the center-point voltage variations has been widely recognized for three-phase, three-level inverters [8], [9], [11]–[16]. The possibility of influencing the center-point voltage of a three-level rectifier is based on the existence of identical switching states concerning the voltage space vector generated at the input of the rectifier system [17]. These redundant switching states are characterized by the opposite loading of the center point (opposite signs of the center point current). This makes possible the control of the center point voltage, ideally, independent of the input current control that determines the rectifier input voltage space vector generated over a pulse period. In general, one has to select a switching state that acts to reduce the voltage asymmetry if a voltage space vector being non-unique with respect to the converter switching state occurs. This switching state has to be included into the switching sequence while still considering the use of a minimum number of switch commutations. For the time-average over a mains period, this leads to an increase of the relative on-time of the switching states which results in a reduction of the unsymmetrical voltage distribution. The relative on-times of the redundant switching states, which would increase the asymmetry, are reduced by the same amount. For ideal symmetry of the output partial voltages, the redundant switching states would have equal average on-times.

The well-known indirect modulation methods, where typically separated current error compensators and voltage modulators are used, for three-level PWM inverters [19], [20] are applicable to three-level PWM rectifier systems [Fig. 2(a)]. The coordination of the switching of the phase legs is implemented with a space vector control unit that is part of the current controller. However, for lower power level applications, such as...
5 kW telecommunication power supplies, a small volume, low weight and high power density are desired, and therefore high switching frequencies are necessary. The indirect modulation methods have the disadvantages of a relatively high complexity of the control unit requiring a digital realization (not normally suited for high switching frequencies) and restricted dynamics due to the application of a PWM unit as compared to direct (hysteresis) current control [Fig. 2(b)]. Hysteresis current controllers are usually implemented in analog circuitry and are, therefore, easily understood by the traditional analog power supply design engineer. The design of the current controller is simple, requires no in-depth analysis and has robust operation, which is of particular advantage in mission-critical applications, such as aerospace. Hysteresis current controllers, in addition, have a high dynamic capability, thus providing a fast response to step changes in the load current and/or reference current [21],[22]. The switches operate with a non-constant frequency and the switching harmonics are distributed over a wider frequency range with a lower average amplitude, although techniques can be applied that result in a near constant switching frequency [23]. However, when a hysteresis current controller is applied to a three-level PWM rectifier, the center point voltage is not naturally stable. Therefore, to minimize the system cost, we have to pose the question: is it possible to include the control of the center point voltage in a simple analog hysteresis current control concept? It is shown in this paper that by adding an offset (an equal value for all phases) of the phase current reference values. Due to the floating mains neutral point, the mains current shape is not directly influenced. However, the offset signal influences the distribution of the frequency of the switching states used for guidance of the mains current and therefore of the value of the center point current. In Section V the design of the center point voltage control circuit of a rectifier unit is described and the output voltage center point controller response for stationary operation and for a load step are experimentally demonstrated.

II. HYSTERESIS CURRENT CONTROL

A brief review of the hysteresis current control of the input current of three-level rectifiers is undertaken in order to show the resulting loading of the output voltage center point in Section III.

The input current $i$ of a boost-type PWM rectifier is impressed according to

$$L \frac{di}{dt} = v - v_r$$

by the difference of the rectifier input voltage space vector $v_r$ and the mains voltage space vector

$$v = \tilde{V}e^{j\varphi} \quad \varphi = \omega t \quad \text{and} \quad \omega = 2\pi f$$

across the inductances $L$ connected in series on the mains side with a fundamental frequency $f$. The definition of the complex space vector, using the rectifier input voltage as an example, is

$$v_r = \frac{2}{3}(v_{RM} + v_{SM} + v_{TM}) \quad \overrightarrow{a} = e^{j\frac{2\pi}{3}}.$$  

A sinusoidal shape of the mains voltage (corresponding to the mains voltage shape) and a resistive mains behavior of the rectifier system is required. The phase current reference

$$i^* = \tilde{f} \frac{v}{\tilde{V}}$$

is obtained, ideally, for

$$v_{r1} = v - j\omega L \tilde{i}^*.$$  

Due to the discontinuous control property of the rectifier, the fundamental voltage space vector $v_{r(1)} = v_{r1}$ is generated only as a time average over several switchings of the system bridge legs. For the current control error

$$\Delta i = i - \tilde{i}^*$$

Fig. 2. Schematic representation of a) indirect current controller having separated phase current error compensator and voltage modulator parts and b) direct (hysteresis) current controller.
it there follows from (1)

\[ L \frac{d\Delta_i}{dt} = \xi^b_i - \xi^c_i, \]

that the variation of the control error is defined directly by the difference between the actual generated voltage and the time-continuous varying reference value.

To sinusoidally guide the phase currents by independent hysteresis controllers, the control signals of switches in the bridge legs (see Fig. 3) are derived directly from the control errors of the related phase currents from

\[ s^i_k = \begin{cases} 0, & \text{if } i^k > \xi^k_i + h \\ 1, & \text{if } i^k < \xi^k_i - h \end{cases}, \]

where the index \( i = R, S, T \) and \( \pm h \) defines the hysteresis band.

The input rectifier phase voltage \( v_{iM} \) is influenced both by the switching state of the power transistor \( s_k \) and also by the sign of the corresponding mains current \( i_k \)

\[ v_{iM} = \begin{cases} \text{sgn}(i_k) \frac{1}{2}, & \text{if } s_k = 0 \\ 0, & \text{if } s_k = 1 \end{cases}. \]

The dependency of the phase switching decisions on the phase current direction is included by an inversion

\[ s_k = \begin{cases} s^k_p, & \text{if } i^k_p \geq 0 \\ \text{NOT}s^k_p, & \text{if } i^k_p < 0 \end{cases}. \]

Basically, each phase has three possible phase voltage values, \( +\left( V_1/2 \right), 0 \) and \( -\left( V_1/2 \right) \) (three-phase, three-level PWM rectifier). In total, there result \( 3^3 = 27 \) possible states of the converter system. However, due to the dependency of the voltage generation on the sign of the mains phase currents [cf. (9)], each phase only switches between two voltage levels \( +\left( V_1/2 \right) \) and \( 0 \) for \( i^k > 0 \); \( -\left( V_1/2 \right) \) and \( 0 \) for \( i^k < 0 \). Therefore, only \( 2^3 = 8 \) phase voltage combinations remain for each combination of current directions (e.g., \( i_R > 0, i_S < 0, i_T < 0 \)).

Since the rectifier system has no connection between the dc side and the mains star point, the formation of the mains phase currents is not defined by the phase voltages but by the line-to-line voltages and/or by the voltage space vectors \( \xi_p \) corresponding to the eight phase voltage combinations \( (v_{RM}, v_{SM}, v_{TM}) \) and/or switching state combinations. Only seven voltage space vectors (cf. Fig. 4) are related to the eight phase voltage combinations (and/or switching state combinations) and therefore a redundancy of switching states exists (equal to a degree of freedom of the voltage control) regarding the formation of the voltage space vectors. This degree of freedom can be applied for controlling the center point voltage.

The voltage space vectors available in the mains phase interval \( \varphi \in (-\pi/6), (+\pi/2) \) for a three-level PWM rectifier are shown in Fig. 4(a). Each switching space vector is de-
The current $i_M$ loads the capacitive center point and is formed by sections of the phase currents with dependency on the switching states $s_i$ of the power transistors:

$$i_M = s_Ri_R + s_Si_S + s_Ti_T. \quad (14)$$

The voltage shift of the center point is hence given by

$$\frac{d\Delta v_M}{dt} = \frac{1}{2C}i_M \quad (15)$$

for a constant output voltage $V_0$ and equal capacitor values $C_+ = C_- = C$. It should be noted that since the output partial voltages affect the center-point voltage shift in the same direction:

$$\frac{dv_{C+}}{dt} = -\frac{dv_{C-}}{dt}$$

the variation of the center-point voltage is determined only by $i_M$. Moreover, because of the constant output voltage, regulated by the output voltage controller $F(s)$, the parallel connection of both capacitors, $2C$, is acting.

The center point current (14) resulting for the possible combinations of values of the phase switching functions for $\varphi \in (-\pi/6, +\pi/6)$ can be taken directly from Fig. 5. In Fig. 5, the contribution to $i_M$ of three different types of rectifier input space vectors is represented and the space vectors for sector 1 are chosen (cf. Fig. 4). The short space vectors of $(0-, +)$, corresponding to the redundant switching states, provide the largest contribution to $i_M$ in opposite directions. This is indicated in Table I by a double contribution $(++$ or $-\cdot)$, respectively. The medium vectors contribute also to $i_M$, like $(+0-)$ in Fig. 5, and are indicated in Table I by a single sign, $+, or -$ in Fig. 5, do not contribute to $i_M$. For equal frequency (equal relative on-time and equal distribution within the angle interval $\varphi$) there results no mean potential shift $d\Delta i_M/dt_{\text{avg}}$ of the capacitor center point due to the sum of the contributions of the different switching states. However, for hysteresis control of the phase currents the switching states resulting in a lower current variation $d\Delta i_i/dt$, i.e. the space vectors lying in the vicinity of the trajectory of the reference input space vector $\gamma^*$, have a greater mean existence interval and/or higher relative on-time $\delta$. Therefore, for the considered segment of the mains period there results a negative mean value $i_{M,\text{avg}}$ and/or an increase of $v_{C+}$ relative to $v_{C-}$ (where $i_{M,\text{avg}}$ denotes averaging over a $\pi/3$ wide interval).

An analog analysis of the center point current for the angle interval $\varphi \in (+\pi/6, +\pi/2)$ leads to the values compiled in Table II. A positive mean value $i_{M,\text{avg}}$ results, which is opposite to the previous interval. The analysis of further angle intervals leads to alternating positive and negative contributions of $i_{M,\text{avg}}$. Accordingly, the fundamental frequency of the center point current $i_M$ is defined by $3f$, where $f$ is the mains frequency, as is also known from three-level PWM inverters [11].

Based on the previous considerations and on ideal and equal system behavior within the different angle intervals, one would not expect a voltage shift in the average over a mains period. However, due to the mutual influence of the three independent

---

**Noted by the triple $(t_R, t_S, t_T)$ formed by the phase switching functions $t_i$, where $t_i = sgn(v_{iM}) = \{+0, -\}$ if the respective phase input rectifier terminal is clamped to the positive rail, to the center-point or to the negative rail, respectively.

The space vectors are usually classified into zero voltage vectors, small vectors which are the vertices of the outer hexagon, medium vectors which are the midpoints of the sides of the outer hexagon and large vectors comprising of the vertices of the outer hexagon.

If the input current is based on a purely symmetrical sinusoidal shape of

$$i_R = I_R \cos(\varphi)$$
$$i_S = I_R \cos \left(\varphi - \frac{2\pi}{3}\right)$$
$$i_T = I_R \cos \left(\varphi + \frac{2\pi}{3}\right) \quad (11)$$

there always results at the limits of the $\pi/3$ wide intervals (e.g. $\varphi \in (-\pi/6, +\pi/6)$, $(+\pi/6, -\pi/2)$) a reversal of the sign of a phase current. From the inversion of the corresponding phase voltage, the hexagon, formed by the rectifier input voltage space vectors (cf. Fig. 4) is rotated by $\pi/3$ in the direction of the movement of the current space vector.

The basis for controlling the center-point voltage is given by the knowledge of the center point currents. The short space vectors of $(0-, +)$ lie always symmetrically around the angular segment corresponding to the momentary combination of the sign and/or directions of the phase currents.

The block diagram of the control rectifier system is shown in Fig. 3. According to (4) the mains phase current reference values $i_i^*$ are proportional to the corresponding mains phase voltages $v_i$. The amplitudes $I_i$ of the phase reference currents are defined by an output voltage control loop, with a dependency on the output voltage error $\Delta V_0 = V_0 - V_0$. The functions for the output voltage control and the center-point voltage balance are given by $F(s)$ and $G(s)$, respectively.

**III. Loading of the Output Voltage Center Point**

The control unit of the converter has to guarantee the symmetry of the partial output voltages, $v_{C+}$ and $v_{C-}$ (Fig. 1). The basis for controlling the center-point voltage is given by the knowledge of the center point currents $i_M$ resulting from different switching states. Therefore, in the following we will investigate the average shift of the center point voltage occurring within the $\pi/3$ wide interval $\varphi \in (-\pi/6, +\pi/6)$ of the mains period. First, the case of balanced output voltages is considered and then the case of unbalanced partial output voltages.

**A. Balanced Output Partial Voltages**

The center-point voltage unbalance $\Delta v_M$ is defined as

$$\Delta v_M = \frac{1}{2}(v_{C-} - v_{C+}). \quad (12)$$

Accordingly, since $v_{C+} + v_{C-} = V_0$, then the output partial voltages are

$$v_{C-} = \frac{1}{2}V_0 + \Delta v_M \quad v_{C+} = \frac{1}{2}V_0 - \Delta v_M. \quad (13)$$

The current $i_M$ forces the center point.
TABLE I
CENTER POINT CURRENT $i_M$ AND AVERAGE SHIFT OF THE CENTER POINT POTENTIAL $\Delta v_M$ FOR $\varphi \in (-\pi/6, +\pi/6)$ AND SWITCHING STATE $(t_R, t_S, t_T)$ FOR EQUAL RELATIVE ON-TIME AND DISTRIBUTION OF THE SWITCHING STATES (CF. $(d\Delta v_M/dt)_{avg}$) AND FOR THE RELATIVE ON-TIME $\delta$.
A NEGATIVE MEAN VALUE OF THE CENTER POINT CURRENT RESULTS

<table>
<thead>
<tr>
<th>$t_R$</th>
<th>$t_S$</th>
<th>$t_T$</th>
<th>$i_M (d\Delta v_M/dt)_{avg}$</th>
<th>$\delta (d\Delta v_M/dt)_{avg}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>+</td>
<td>-</td>
<td>-</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>+</td>
<td>-</td>
<td>0</td>
<td>$i_T$</td>
<td>$-\Delta v_M$</td>
</tr>
<tr>
<td>+</td>
<td>0</td>
<td>-</td>
<td>$i_T$</td>
<td>$-\Delta v_M$</td>
</tr>
<tr>
<td>+</td>
<td>0</td>
<td>0</td>
<td>$-i_R$</td>
<td>$+\Delta v_M$</td>
</tr>
<tr>
<td>0</td>
<td>-</td>
<td>-</td>
<td>$+i_R$</td>
<td>$+\Delta v_M$</td>
</tr>
<tr>
<td>0</td>
<td>-</td>
<td>0</td>
<td>$-i_T$</td>
<td>$+\Delta v_M$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>-</td>
<td>$-i_T$</td>
<td>$+\Delta v_M$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

TABLE II
AS IN TABLE I BUT FOR THE INTERVAL $\varphi \in (+\pi/6, +\pi/2)$

<table>
<thead>
<tr>
<th>$t_R$</th>
<th>$t_S$</th>
<th>$t_T$</th>
<th>$i_M (d\Delta v_M/dt)_{avg}$</th>
<th>$\delta (d\Delta v_M/dt)_{avg}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>+</td>
<td>+</td>
<td>-</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>+</td>
<td>0</td>
<td>+</td>
<td>$i_T$</td>
<td>$-\Delta v_M$</td>
</tr>
<tr>
<td>+</td>
<td>0</td>
<td>0</td>
<td>$-i_R$</td>
<td>$+\Delta v_M$</td>
</tr>
<tr>
<td>0</td>
<td>+</td>
<td>-</td>
<td>$+i_R$</td>
<td>$+\Delta v_M$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>+</td>
<td>$-i_T$</td>
<td>$+\Delta v_M$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

hysteresis phase current controllers, there results a stochastic [24, 25] or chaotic [26] sequence and/or large variation in the on-times and distributions of the different switching states. Thus, the center point current $i_M$ shows in general a small dc-component $I_M$ (mean value over a mains period) or a low frequency harmonic, lying below the mains frequency. This leads to an asymmetry of the partial output voltages and/or to a shift $\Delta v_M$ of the output voltage center point.

In order to maintain long-term stability for a higher modulation index and/or in case of unbalanced, non-linear loads or no load operation, one has to investigate whether the voltage shift $\Delta v_M$ causes an increase or decrease of the mean center-point current value $I_M$ and if the center-point loading effect of the current $i_M$ leads to an instability of the center-point voltage.

B. Unbalanced Output Partial Voltages

In case of asymmetry of the output partial voltages, the input rectifier voltage space vector $\mathbf{V}_r^g$ is given by the sum of the vector $\mathbf{V}_r$, as defined for balanced conditions and a distortion space vector $\Delta \mathbf{V}$ that is dependent on converter switching states:

$$ \mathbf{V}_r' = \mathbf{V}_r + \Delta \mathbf{V} $$

where the distortion vector is given by

$$ \Delta \mathbf{V} = \frac{2}{3} \Delta v_M (s_R + q s_S + q_s^2 s_{ST}) $$

The distortion space vectors for the interval $\varphi \in (-\pi/6, +\pi/6)$ are shown in Table III.

If the capacitive center-point $M$ is not loaded (long space vectors and $i_M = 0$) a voltage shift $\Delta v_M$ does not influence the corresponding voltage space vectors. In this case, the input rectifier voltage is only determined by the total amount of the output voltage. The distortion space vectors $\Delta \mathbf{V}$ of the switching states associated with the short and medium space vectors show a constant absolute value and are defined directly by the asymmetry. The resultant voltage space vectors for $\Delta v_M < 0$ and $\varphi \in (-\pi/6, +\pi/6)$ are shown in Fig. 4(b).

For hysteresis current control, the frequency of the switching states is essentially influenced by the absolute values of the corresponding space vectors $d\Delta i_M/dt$ defining the time behavior of the control error. For example, in $\varphi \in (-\pi/6,+\pi/6)$ the switching states (+00), (+−−), (+−0) and (0−−) are preferred. According to Fig. 4(b), an asymmetry $\Delta v_M$ leads, especially, to a change of the absolute value of the vectors of the switching states (0−−) and (00) by the same amount in the opposite directions and to a rotation of the vectors of the switching states (+00) and (+−0). Therefore, for $\Delta v_M < 0$ the switching state (00) is preferred as compared to (0−−) (cf. Fig. 4(b) and Fig. 6(a), which is generated from simulation). As can be seen from Table I with this the equilibrium of the switching states, which have essential influence on generating the center point current, is disturbed. There occurs a reduction of the negative average value $\bar{i}_{M,avg}$ which further increases the asymmetry.

As a detailed analysis shows, the considerations given so far for $\varphi \in (-\pi/6, +\pi/6)$ correctly represent the conditions over the entire fundamental period. For each $\pi/3$-wide interval of the mains period (to be differentiated concerning the sign combinations of the phase currents) there results a change of the respective average value $\bar{i}_{M,avg}$ which acts in the direction of an increase of an (already) existing asymmetry.
Since the rectifier’s output center point is not connected to the mains neutral point, the sum of the mains phase currents is forced to zero at all times and therefore the offset $i_o$ cannot be produced by the phase current controllers and does not influence the mains current shape.

The space vector representation of the control errors of the phase currents $\Delta i_i = i_i - i_i^s$, whose complex components are given by

$$
\Delta i_\alpha = \frac{1}{\sqrt{3}}(\Delta i_S - \Delta i_T) \\
\Delta i_\beta = \frac{1}{\sqrt{3}}(\Delta i_S + \Delta i_T)
$$

(19)

clearly shows that $i_o$ has influence on the form of the tolerance area (Fig. 7) defined by the intersection of the tolerance bands of each of the phase current controllers. Therefore, the offset has influence on the frequency of the switching states used for guidance of the mains current and consequently the value of the center point current.

For $i_o = 0$, the tolerance area shows the characteristic form of an equilateral hexagon, limited by segments of the positive and negative switching thresholds of equal length (Fig. 7). Accordingly, for both switching thresholds there exists equal switching frequency,

$$
f_+ = f_- 
$$

where $f_+$ and $f_-$ indicate the number of intersections of the current ripple with the positive and negative thresholds, respectively.

If now the switching thresholds are shifted due to an offset $i_o$ of the phase current reference values, the tolerance area is distorted and the conditions in (8) are now given by

$$
s'_i = \begin{cases} 
0, & \text{if } i_i > i_i^s + h + i_o \\
1, & \text{if } i_i < i_i^s - h + i_o
\end{cases}
$$

(20)

In addition, the border is formed by segments of the positive and negative switching thresholds that are of unequal length.

For $i_o > 0$, an increase of the contribution of the negative switching thresholds is given in Fig. 7. Accordingly, for guidance of $\Delta i$ within the tolerance area the switching frequency $f_-$ is increased and $f_+$ decreased, respectively. Therefore, the on-switching states, $(s'_R, s'_S, s'_T)$ = (1xx), (x1x), (xx1) are used more often, leading to a positive center-point voltage shift ($d\Delta v_M/dt > 0$). This effect is shown in Fig. 8, where the shape of the center point current for a discrete value of the offset $i_o$ is represented for a mains period, along with the phase current $R$. The resulting experimentally measured trajectories of the space vector $\Delta i$ (19) are given in Fig. 9 for $i_o = 0, 0,5 h$ and $-0,5 h$. Fig. 6(b) shows the change in the average relative on-times $\delta_{(0-)}$ and $\delta_{(0+)}$ of the redundant switching states (0 $-$) and (0 $+$) ($\varphi \in (-\pi/6, +\pi/6)$) for increasing values of the offset current. It can be seen that the switching state (0 $-$) becomes dominant for a positive $i_o$.

For $i_o < 0$, an analog consideration leads to $f_+ > f_-$ and finally to $d\Delta v_M/dt < 0$. Therefore, the offset signal $i_o$ offers the possibility of an active symmetrization of the partial output voltages and/or of a control of the voltage of the output voltage center point.

**IV. CONTROL CONCEPT**

As previously discussed, the three-level PWM rectifier system has two identical (redundant) switching states regarding the generation within each $\pi/3$-wide interval of the mains period. The redundant switching states in an interval have opposite signs of the center point current and a significant influence on the generation of the center point current. Therefore, a shift and/or control of the center point potential can be achieved without influencing of the output voltage control and/or the mains current control. In general, to balance the output partial voltages the relative on-time of the redundant switching state that reduces the unbalance must be increased.

**A. Impact of a Phase Current Reference Offset on Center-Point Voltage and Mains Current**

Since the switching decisions $s'_i$ are derived directly from the difference between reference and actual value of each phase current, according to the function of the hysteresis control, the possibility of a control input influencing the applied time of the different switching states is basically limited to a modification of the reference value shape. Due to the amplitude $\tilde{f}$ being fixed by the power to be supplied and by the required sinusoidal shape, the only degree of freedom consists of the addition of a zero-component $i_o$ (an equal offset for all phases). The modified current references are now

$$
\begin{align*}
\tilde{i}_R' &= \tilde{i}_R + i_o \\
\tilde{i}_S' &= \tilde{i}_S + i_o \\
\tilde{i}_T' &= \tilde{i}_T + i_o.
\end{align*}
$$

(18)

Fig. 6. Simulated average relative on-time $h_{(+)0}$ and $h_{(0-)}$ of the redundant switching states (+00) and (0$-$) in Sector 1 as function of (a) of the center point voltage shift $\Delta v_M$ normalized over the total output voltage $V_o$ and (b) of the current offset $i_o$ normalized over the hysteresis band amplitude $h$. 

Since the rectifier’s output center point is not connected to the mains neutral point, the sum of the mains phase currents is forced to zero at all times and therefore the offset $i_o$ cannot be produced by the phase current controllers and does not influence the mains current shape.
We have to point out that the method described here shows an analogy to a control concept for controlling of $\Delta v_M$ proposed in [11] in connection with controlling three-level inverters by pulse width modulation. In [11], it is shown very clearly how the direct influence on the average value of the center point current by a zero-component $i_0$ of the phase modulation functions is possible for PWM. This zero-component corresponds to the offset $i_0$ of the phase current reference values. Due to the attempt of the phase current controllers to impress $i_0$ despite the missing neutral line, a mean value of the zero-voltage lying between the mains star point and the center point $M$ results. This shows that both concepts are mutually corresponding.

**B. Dependence of the Center-Point Current on the Current-Reference Offset**

The average value $I_M$ resulting for a defined shift $i_0$ of the reference values and/or the gain:

$$ k_M = \frac{\Delta I_M}{\Delta i_0} $$  \hspace{1cm} (21)

of the output signal $I_0$ from the center-point voltage controller has been experimentally measured and the resulting control characteristic $I_M(i_0)$ is shown in Fig. 10. In this case the partial capacitor voltages are externally forced to be equal and accordingly $\Delta v_M = 0$ and there is a constant output voltage $V_0$ and a constant amplitude of the phase current reference values $\hat{I}^\ast$. The characteristic can be approximated by a straight line around the origin:

$$ I_M = I_{M,\Delta v_M=0} + k_M I_0 $$  \hspace{1cm} (22)

where, $I_{M,\Delta v_M=0}$ describes the average value of the center point current related to a mains period, occurring without control input ($i_0 = 0$) and for symmetric partition $\Delta v_M = 0$ of the output partial voltages.

The center point current $I_M$ shows in a first approximation a linear dependency on the amplitude of the phase current reference values $\hat{I}^\ast$, as apparent from (14) and the normalized plot in Fig. 10. It should be noted that a reduction of the mains voltage amplitude $\hat{V}$ leads to an increase of the absolute value of $I_M$, since the relative on-time of the redundant switching states $1/(0-\pm)$ and $(+00)$ for $\varphi \in (-\pi/6, +\pi/6)$ increases, resulting for a defined value $I_0$.

The saturation in the control characteristic of Fig. 10 for $I_0 = \pm(1/3)h$ becomes clear by inspection of Fig. 7. For $I_0 = +1(1/3)h$ the positive switching thresholds are touched by the tolerance area at only one point. Therefore, the tolerance area assumes the form of a triangle and is limited exclusively by negative switching thresholds (cf. Fig. 9). Thereby, the limit of an approximately linear influence of $I_0$ on the relative on-times $\delta_{+}$ and $\delta_{-}$ of the redundant switching states is reached. A further increase of $I_0$ has no importance in practice and results only in a small increase of the average value $I_M$.

It is of interest to analyze if the offset $I_0$ produces low frequency harmonics, especially those of even order, due to the asymmetry of the positive and negative half cycles caused by

Fig. 7. Space vector representation of the current ripple $\Delta I$ for offset $i_0 = 0$ (dashed line) and $i_0 > 0$. The positive and negative hysteresis thresholds, $+h_s$ and $-h_n$ (index $i = R, S, T$) respectively, vary according to the value of $i_0$. For $i_0 = (1/3)h$ the positive switching thresholds are touched by the tolerance area only at one point.

Fig. 8. Simulated time behavior of the phase current $i_\alpha$ (black line) and of the center-point current $i_{3M}$ (gray line) for different values of $i_0$. a) $i_0 = 0$, b) $i_0 = +0.3h$ and c) $i_0 = -0.3h$, where $h$ is the hysteresis band amplitude.
The center point voltage control represents a fixed command control $\Delta V^*_{M} = 0$. Therefore, the control loop has to be designed with respect to its disturbance response. A disturbance of the symmetrical voltage partition can result, from a change of the system load. Hence, the output voltage controller $F(s)$ (Fig. 3) changes the amplitude of the mains phase current reference values within a mains period. Due to the direct coupling between center point current and mains current (14) this results in the occurrence of a transient mean value of $i_{M}$. Furthermore, a direct loading of the center-point can result due to an asymmetric partitioning of the load, supplied by the rectifier, from the two partial output voltages. The disturbance influence is considered in Fig. 12 by the current $I_{Z}$.

### A. Center-Point Characteristic

Fig. 13 shows that the deviation of the partial output voltages from the symmetrical case results in a mean value $I_{M}$, which produces further asymmetry and is proportional, in a first approximation, to $\Delta V_{M}$. For a control oriented model this behavior can be described by a positive feedback:

$$g_M = \frac{\Delta I_M}{\Delta V_M}, \quad g_M > 0$$

(24)

corresponding to the positive rate of rise of the characteristic $I_{M}(\Delta V_{M})$ at the origin. Therefore, the system $S(s)$ to be controlled by the center point voltage control (see Fig. 12) shows a pole in the right-hand s-half-plane:

$$S(s) = \frac{1}{s - \frac{g_M}{2k}}.$$  

(25)

It should be noted that the mains voltage has influence on the value of the gain $g_M$. A reduction of the mains voltage and/or relative reduction of the mains voltage peak value (defining the trajectory of the space vector $y_{M}$) results in an increase of the gain $g_M$. This is true since, in general, a larger relative on-time
of the P-component of the
component, for the mains-current amplitude
needs to be considered as well as
the quantities
Thus the model shown in
and
damping
due to the operating principle of the rectifier. In
with a frequency
over one mains period.
the increase in the variation of
controller, the limitation of the correcting value introduced for
controller, the cross-over frequency
Fig. 13. Experimentally measured and normalized center-point characteristic.
The center-point voltage shift \( \Delta V_M \) is referred to the output voltage \( V_o \) while
the center-point current \( I_M \) to the mains-current amplitude \( I \). Experimental operating point is \( V_{rms} = 30 \ \text{V}, V_o = 115 \ \text{V}, I^* = 5 \ \text{A}, h = 0.5 \ \text{A} \).
order to avoid a mutual influence of the phase current control
and of the center point voltage control, the cross-over frequency
should occur sufficiently below 3\( f \). Thus the model shown in
Fig. 12, based on averaging over a fundamental period, can be
directly applied for dimensioning of the controller.
If \( G(s) \) is realized, with respect to the stationary operation
\( \Delta V_M = 0 \), as a PI-controller such that
it follows that the disturbance response is
\[
\frac{\Delta V_M(s)}{I_Z(s)} = k \frac{s}{1 + 2k \frac{s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2}
\]
with
\[
k = \frac{1}{k_P k_M} \omega_0 = \sqrt{\frac{k_P k_M}{2C}} \ \text{and} \ d = \frac{k_P k_M - g_M}{2\sqrt{2C k_P k_M}}.
\]
Therefore, for a step function disturbance \( I_Z(s) = I_Z/s \) the
center point voltage has a shape corresponding to an impulse
response of a second-order transfer function with gain \( k \),
characteristic frequency \( \omega_0 \) and damping \( d \). Based on the impulse
response of such a function, the controller parameters \( k_P \) and
\( k_I \) can be easily calculated and used to obtain a desired
transient response and/or damping and characteristic frequency.
For determining the gain \( k_P \) of the P-component of the
controller, the limitation of the correcting value introduced for
values \( i_o > h/3 \) (Fig. 13) needs to be considered as well as
the increase in the variation of \( \Delta V_M \) with a frequency 3\( f \),
for increasing \( k_P \).
For low load conditions a reduction in the damping of the
control loop and a decrease of the characteristic frequency \( \omega_0 \)
(28) results, due to a decrease of the gains $k_M$ and $g_M$, which are proportional to the mains current amplitude in a first approximation.

Concerning the assumption of a constant output voltage, it should be noted, that there is a certain decoupling between the controller of the output partial voltages (center-point control) and the total output voltage controller. The dynamics of the two controllers are different since for the center-point voltage control the dynamically active capacitance of the output circuit is defined by the parallel circuit of the partial capacitors ($2C$), while for the output voltage control it is by the series connection ($(1/2)C$). Furthermore, the center point current oscillates with three times the mains frequency. This requires a relatively low cross-over frequency of the center point voltage controller. Contrary to this, there is an ideally constant power flow for output voltage control, therefore, the controller dimensioning can be performed without taking consideration of the low-frequency variation of the controlled quantity.

C. Stationary and Dynamic Operation

Verification of the performance of the center-point voltage controller has been undertaken using a three-level Vienna rectifier [18] with the rectifier and system parameters given in Table IV. The experimental rectifier is designed to operate over a wide line-to-line voltage range of 200 to 480 V. The maximum rated current is 15 $A_{rms}$ giving a maximum input rated power of 5 kW at 200 V and 10 kW at 400 V. A purely digital, software hysteresis current controller is implemented in a TMS320F2808 DSP with a sampling frequency of 75 kHz. With the set hysteresis band an average switching frequency of approximately 10 kHz is realized. Fig. 14 shows the variation of $\Delta V_M$ duration the operation and non-operation of the center point voltage control loop. It can be seen that the center point voltage difference is initially controlled to be zero ($\Delta V_M^k = 0$) until $t = t_0$. As can be expected due to the I-component of the controller $G(s)$ (26), no stationary error results. At $t = t_0$, the center point voltage controller is turned off and the voltage shows a shape corresponding to the step response of an integrator with positive feedback. The step disturbance is given there by the absence of the controller output $k_MI_0\Delta V_M=0$, compensating the average value of the center point current resulting from the statistic sequence of the switching states of the system. An almost identical shape of the step response of the linear model (25) of the real system only exists in the vicinity of $\Delta V_M = 0$. According to Fig. 13, an increasing asymmetry is associated with a reduction of the positive feedback. The control loop is again operated at $t = t_1$ and results in the asymmetry of the partial voltages being controlled back to zero within 30 ms. As shown in Fig. 14, the sinusoidal guidance of the phase currents is slightly influenced by the asymmetric partitioning of the output voltage, although there is an instantaneous shift in the phase current at $t = t_1$ due to applied offset current $i_0$. Within 1 mains cycle the additional distortion disappears and the phase current has a mostly sinusoidal shape. It can also be seen that a relatively large shift of the center point ($\Delta V_M \approx 0.125 V_o$) leads to no significant distortion of the mains current shape.

In order to view the dynamic behavior of the center point voltage control, the center point $M$ is loaded by a step function of an external current disturbance $I_Z$. This corresponds, in a first approximation, to a disturbance that could be expected from a load, such as a dc-dc converter, that is connected to one half of the output voltage bus. The measured waveform of the center point voltage for a load step from 1.8 A (720 W) to 6.0 A (2.4 kW) is shown in Fig. 15. It can be seen that this results in an insignificant deviation of 4 V in the center-point voltage shift $\Delta V_M$.

The dynamic quality of the control is influenced by the output power and/or by the mains current amplitude, which influences directly the parameters $g_M$ and $k_M$. With decreasing output

<table>
<thead>
<tr>
<th>parameter</th>
<th>symbol</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>mains voltage</td>
<td>$V_{rms}$</td>
<td>115 V</td>
</tr>
<tr>
<td>output voltage</td>
<td>$V_o$</td>
<td>400 V</td>
</tr>
<tr>
<td>output power</td>
<td>$P_o$</td>
<td>2.65 kW</td>
</tr>
<tr>
<td>peak reference current</td>
<td>$I^*$</td>
<td>11.5 A</td>
</tr>
<tr>
<td>hysteresis band</td>
<td>$\pm h$</td>
<td>$\pm 1.5$ A</td>
</tr>
<tr>
<td>input inductance</td>
<td>$L$</td>
<td>1 mH</td>
</tr>
<tr>
<td>output capacitance</td>
<td>$C$</td>
<td>940 $\mu$F</td>
</tr>
</tbody>
</table>

Fig. 14. Measured input voltage $v$ (Ch. 1, 200 V/div), phase current $i$ (Ch. 2, 10 A/div) and center-point voltage shift $\Delta V_M$ (Ch. A, 25 V/div) for open ($t = t_0$) and closed ($t = t_1$) center-point voltage control loop. The total output voltage is $390 V_{dc}$. Time scale: 20 ms/div.

Fig. 15. Measured line current $i$ (Ch. 2, 10 A/div), load current $i_L$ (Ch. 1, 2 A/div) and center-point voltage $\Delta V_M$ (Ch. A, 25 V/div) for a load-step. The total output voltage is $410 V_{dc}$. Time scale: 10 ms/div.
power, the oscillation tendency of the system increases and the settling time rises accordingly. A control quality that is constant for a wide load range can be obtained only by adaption, i.e., by varying the controller gains proportional to $1/P$. An alternative is given by elimination of the load dependency of $k_M$ by a current proportional variation of the hysteresis width.

VI. CONCLUSION

A center-point voltage controller for a three-level PWM rectifier was implemented by augmenting the current reference value by a common offset, which has a control effect on the center-point current. The mains current guidance is realized by three independent hysteresis controllers.

A space vector representation of the input rectifier voltage and current is used to show that the proposed control method alters the on-times of the redundant switching states. The impact of the offset $i_0$ injection and of the center-point voltage shift $\Delta u_M$ on the selection and the frequency of the switching states is analyzed and experimentally verified with a three-level Vienna rectifier. The center-point characteristic $i_M(\Delta u_M)$ is derived and the intrinsic instability of the center-point for hysteresis current controlled PWM rectifiers shown.

A design method of the center-point controller is presented based on the analysis of the center-point voltage shift $\Delta u_M$ due to the effect of both the current $i_M$ and the offset $i_0$. The controller performance has been experimentally verified and it proved to possess good dynamic performance and to have minimum impact on the mains current shape.

The essential advantages of the control concept for the voltage control of the output voltage center point of a unidirectional three-phase three-level PWM rectifier system are the straightforward realization with practical circuits and the possibility of direct inclusion into the analog hysteresis current controller. Therefore, the method can be applied to lower power rectifier systems and for systems with switching frequencies greater than 100 kHz such as used in aerospace applications.

REFERENCES


Luca Dalessandro (S’02–M’07) was born in Bari, Italy, on April 29, 1978. He received the M.Sc. degree (with first class honors) from the Politecnico di Bari, Italy, in 2001 and the Ph.D. degree from the Swiss Federal Institute of Technology, ETH Zurich, Switzerland, in 2007, both in electrical engineering. From 2001 to 2002, he was Researcher at the Max-Planck Institute for Mathematics in the Sciences (MPI-MIS), Leipzig, Germany. From 2002 to 2006, he was a Research and Teaching Assistant at the Power Electronics Systems Laboratory (PES) of the ETH Zurich. In the summer of 2006, under a post-doctoral fellowship grant provided by the Industry, he joined the National Science Foundation Engineering Research Center (NSF-ERC) for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, VA. In the fall of 2006, he was appointed Adjunct Professor at the Bradley Department of Electrical and Computer Engineering, Virginia Tech. Since fall 2007, he has
been a Research Associate at the Power Systems and High-Voltage Technology Institute (EEH) of ETH Zurich. In 2008, he joined the R&D Department, Turbo-machines Group, of ALSTOM Power Systems. He has been an Invited Lecturer and Visitor at several recognized institutions and companies, including the Massachusetts Institute of Technology (MIT), MA, and the National Japanese Institute for Advanced Industrial Science and Technology (AIST), Japan. His research interests include all disciplines of electrical power engineering.

Dr. Dalessandro is the recipient of several awards and fellowship and is listed in Who’s Who in Science and Engineering. He serves the Swiss Embassy in Italy as an External Advisor for international scientific events. He is a Registered Professional Engineer in Italy.

Simon D. Round (SM’01) received the B.E. (Hons) and Ph.D. degrees from the University of Canterbury, Christchurch, New Zealand, in 1989 and 1993, respectively.

From 1992 to 1995, he held positions of Research Associate in the Department of Electrical Engineering, University of Minnesota, and Research Fellow at the Norwegian Institute of Technology, Trondheim, Norway. From 1995 to 2003, he was a Lecturer/Senior Lecturer in the Department of Electrical and Electronic Engineering, University of Canterbury, where he performed research on power quality compensators, electric vehicle electronics, and cryogenic power electronics. He has also worked as a power electronic consultant for Vectek Electronics, where he developed a state-of-the-art digital controller for high-power inverter systems. From 2004 to 2008, he was a Senior Researcher with the Power Electronic Systems Laboratory at ETH Zurich, Switzerland, where he researched in the areas of ultra-compact power converters, applications silicon carbide power devices, and three-phase ac–ac converters. In October 2008, he joined ABB Switzerland as the Control Platform Manager for the Power Electronics and Medium-Voltage Drives Business Unit. He has over 80 publications in journals and international conferences. His current research interests are in ultra-compact power converters, digital control, medium voltage and high temperature applications of silicon carbide power devices, and the application of sparse matrix converters.

Dr. Round was the recipient of the University of Canterbury Teaching Award in 2001. He has been actively involved in the IEEE New Zealand South Section, where he was Vice-Chair and Chairman from 2001 to 2004.

Johann W. Kolar received the Ph.D. degree (summa cum laude/promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria.

Since 1984, he has been working as an independent international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel PWM converter topologies, and modulation and control concepts, e.g., the VIENNA Rectifier and the Three-Phase AC–AC Sparse Matrix Converter. Dr. Kolar has published over 250 scientific papers in international journals and conference proceedings and has filed more than 70 patents. He was appointed Professor and Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich in February, 2001. The focus of his current research is on ac-ac and ac-dc converter topologies with low effects on the mains, e.g. for power supply of telecommunication systems, more-electric-aircraft, and distributed power systems in connection with fuel cells. Further main areas of research are the realization of ultra-compact intelligent converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and EMI filtering, multi-domain/multi-scale modelling and simulation, pulsed power, bearingless motors, and power MEMS.

Dr. Kolar received the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005. He also received an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003. In 2006, the European Power Supplies Manufacturers Association (EPSMA) awarded the Power Electronics Systems Laboratory of ETH Zurich as the leading academic research institution in Europe. He is a member of the IEEJ and of technical program committees of numerous international conferences in the field (e.g., Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). From 1997 through 2000 he has been serving as an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and since 2001 as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS. Since 2002, he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.