A Novel Three-Phase Single-Switch Discontinuous-Mode AC-DC Buck-Boost Converter with High-Quality Input Current Waveforms and Isolated Output

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***Abstract*—In this paper, a new three-phase single-switch ac–dc flyback converter system is presented. The system operates in the discontinuous mode. The simple structure of its power and control circuit, low mains current distortion, and resistive fundamental behavior, as well as the high-frequency isolation of the controlled output voltage, have to be pointed out. Besides the analysis of the stationary operating behavior, the dependencies of the peak values, average values, and rms values of the device currents, and of the maximum blocking voltages across the power electronic devices on the circuit parameters, are given as analytic approximations. The theoretical analysis is verified by digital simulation.**

I. Introduction

THE topic of this paper is the development and analysis of a circuit concept for the realization of the input unit of a unidirectional three-phase ac–dc converter. The converter will be applied as a power supply for an electronic control unit, and will be fed from a 115 V, 400 Hz, three-phase ac system. Due to safety and systems aspects, it has to be realized as a two-stage converter [1]. The controlled output voltage of the rectifier input stage is converted by a dc–dc converter into the load voltage levels.

The basic development requirements which are relevant for the determination of the concept of the mains converter are defined as follows:

- high reliability (low complexity of the power and control units)
- high power density
- full-load efficiency > 0.85
- wide input voltage range
- isolation of the ac and the dc sides
- total harmonic distortion factor < 0.05 (with the assumption of a purely sinusoidal and symmetric mains voltage system)
- fundamental displacement factor of the mains current > 0.95
- current limited start-up, active limitation of the input currents for transient mains overvoltages, limitation of the output current (overload protection)
- possibility of parallel operation of several converters.

For universal applicability of the ac–dc converter, the dc link voltage is defined as $U_O = 280$ V. This is approximately equal to the (ideal) mean output voltage for three-phase diode rectification of the 115 V mains. Due to the high voltage level, this can also be used for buffering of mains voltage outages with relatively low capacitances (minimization of the size). The maximum output power of the mains converter is given by 690 W.

In Section II, a new topology of a three-phase single-switch pulse rectifier system is developed via a three-phase extension of a dc–dc flyback converter. Section III treats the analysis of the operating principle of the system which forms the basis for the derivation of the equations for the stationary operation (Section IV). With the assumption of high pulse frequency, in Section V analytic approximations of the current stresses (peak values, average values, rms values) on the system components are calculated, and the blocking voltage stresses on the power electronic devices are given. The accuracy (or the limit of applicability) of the analytical approximations is derived via a comparison of the results of the calculations to the results of a digital simulation. Based on Section V, in Section VI the approach for dimensioning the converter is discussed. Furthermore, in this section, the values for the component stresses resulting for the initially given operating parameters are summarized. These component stresses form the basis for the selection of the power electronic devices and can be used in an assessment of the converter within a concept evaluation.

Section VII describes a simple extension of the converter structure which leads to an increase of the system efficiency and to a reduction of the blocking voltage stress of the power electronic devices. Finally, the advantages and disadvantages of the converter are compared and commented on in Section VIII.

II. Converter Topologies

Due to requirements for low effects on the mains and for high power density, the mains converter has to be realized

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as a pulse converter system. For high system pulse frequency, the filtering effort is considerably reduced as compared to line-commutated systems [2], [3]. Furthermore, the isolation can be included directly into the converter function and be achieved by a small-size high-frequency transformer.

For the realization of a three-phase pulse rectifier system, one can apply (besides three-phase converter structures) also three single-phase ac–dc converters which are connected in three-phase configuration [4]–[6].

The combination of three single-phase units makes possible the design of a fault-tolerant system due to the parallel operation (on the output side) of the three partial systems which are fed by the different mains phases. The dimensioning of the three converter modules there has to be performed according to half of the output power of the overall system. This results in a high reliability via the redundancy of one module. Furthermore, the modular design simplifies the system development and test. However, these advantages are paid for by a high device count for power and control circuits, and by a reduction of the power density. A further disadvantage is the basically low utilization of the phase modules, which is due to the instantaneous phase power pulsating with twice the mains frequency. In the case at hand, we prefer a direct three-phase realization.

Based on [7] in [8]–[11] three-phase unidirectional pulse rectifier systems with high-frequency isolation are introduced. They show a very simple structure of the power and control circuits and satisfy the initially mentioned requirement regarding low system complexity. The converter topologies can be thought to be formed via a three-phase extension of basic dc–dc coverter structures [8]. They are characterized by discontinuous input phase currents (three-phase single-switch discontinuous inductor current mode boost-type rectifier) or by discontinuous input phase voltages (three-phase single-switch discontinuous capacitor voltage mode buck-type rectifier). The mains voltage proportional control of the peak values of the converter input currents/voltages is achieved in analogy to the discontinuous operation of single-phase ac–dc pulse rectifiers (having constant power transistor on-time) directly by the mains voltages/currents (*automatic* current shaping [12]). For series connection of a mains filter which suppresses input current harmonics with switching frequency, a considerable reduction of the effects on the mains is achieved, as compared to line-commutated rectification.

As a more detailed analysis of the system behavior shows, the harmonics content of the mains currents remaining after filtering the discontinuous input quantities is essentially determined by the voltage or current transformation ratio of the converter [8], [11], [13]. For example, in three-phase single-switch discontinuous inductor current mode boost rectifier systems, high amplitudes of low-frequency harmonics are present in the mains current spectrum [13] for output voltages being low as compared to the amplitude of the line-to-line mains voltage. This leads to a small distortion factor of the mains currents only for high output voltages or for low input voltages, respectively.

Due to the required wide input voltage region, one has to ask the question regarding the topologies of three-phase single-switch discontinuous-mode pulse rectifier systems with input voltage independent (ideal) sinusoidal input currents.

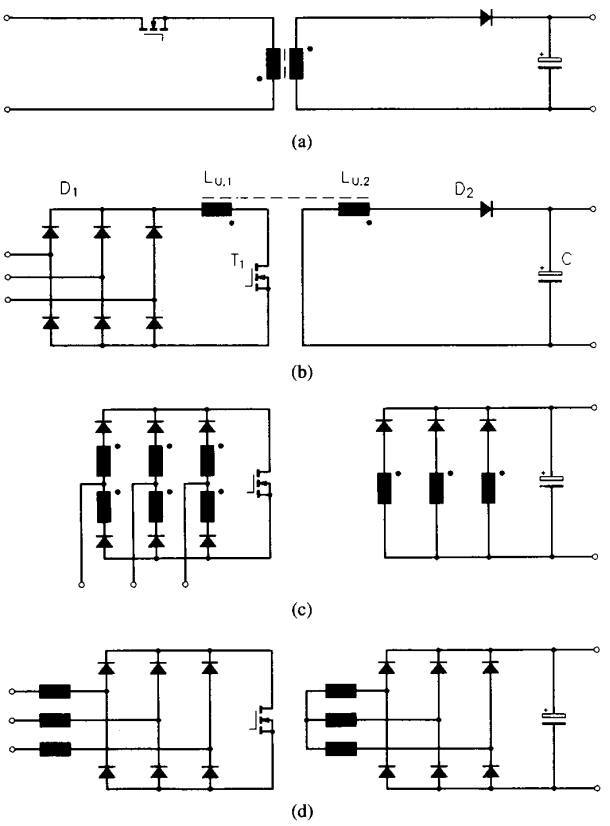

Fig. 1. Development of three-phase single-switch ac–dc flyback converter topologies (b), (c), (d) based on the basic structure of a dc–dc flyback converter (a). (c) shows the three-phase single-switch discontinuous inductor current mode flyback rectifier (regarding the coupling of the partial windings, cf. Fig. 2).

Discontinuous-mode single-phase ac–dc flyback coverters show a purely sinusoidal shape of the filtered input currents for constant pulse frequency and constant on-time [14]. In connection with the simple structure of the power circuit and the full controllability of the power flow (as given for this converter type), this motivates the development of three-phase pulse rectifier systems based on the basic structure of a dc–dc flyback converter as described in the following.

Fig. 1(a) shows the power circuit of a dc–dc flyback converter which can be extended to a three-phase converter by connecting a three-phase diode bridge D_1 [cf. Fig. 1(b)] in series. However, low-frequency harmonics of high amplitude are present in the mains current of this system. This is the case because (due to the operating principle of the three-phase diode bridge) for transistor T_1 conducting, only two phases conduct current. Therefore, the phase current shape shows $\pi/3$-wide intervals with zero current.

If one splits up $L_{U,1}$ to the valve branches [cf. Fig. 1(c)], the mains voltage system and the valve voltage system are decoupled and a simultaneous current flow in all phases is made possible. Due to splitting up the primary windings, the

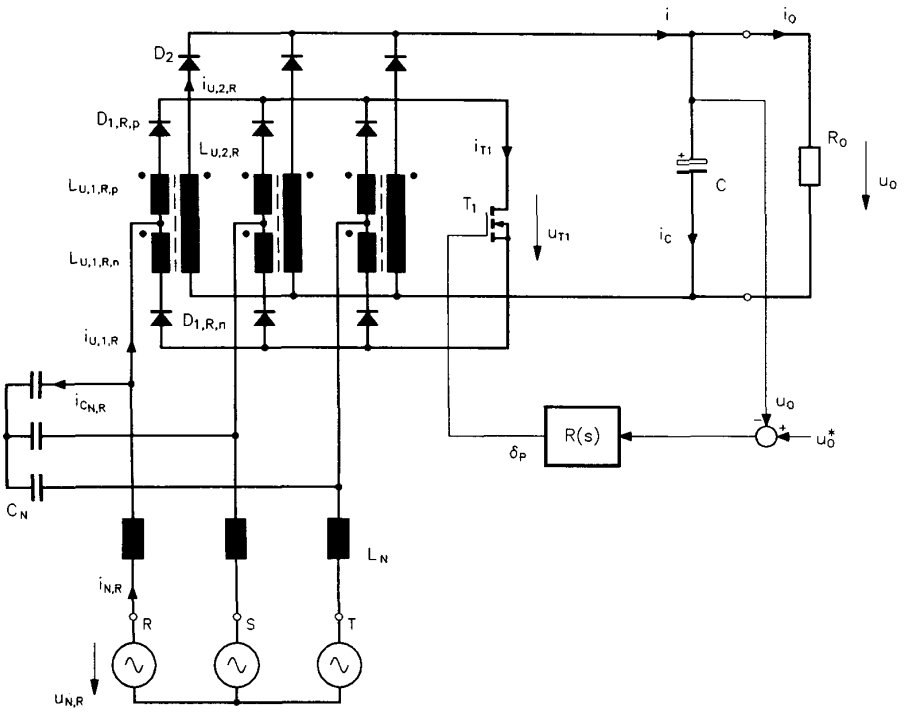

Fig. 2. Basic structure of the power and control circuits of a three-phase single-switch DICM flyback rectifier; the feeding mains is replaced by a Y-connection of ideal voltage sources $u_{N,(RST)}$; filtering of the high-frequency spectral components of the discontinuous converter input currents $i_{U,1,(RST)}$ by a mains filter L_N, C_N. R_O: load resistance (e.g., voltage dependent input impedance of a dc–dc converter connected to the output of the pulse rectifier). In the stationary case, the control of the power transistor T_1 is performed by a constant pulse frequency f_p and by a constant relative turn-on time δ_p being set by an output voltage control circuit.

direction of the secondary current is *not* dependent on the direction of the primary phase currents. The basic secondary circuit structure of the dc–dc converter can therefore be maintained, and the secondary circuits of the phases can be connected in parallel directly.

An ac-side arrangement (and split-up) of $L_{U,1}$ results in the converter structure shown in Fig. 1(d) [15] which makes possible [contrary to (c)] a combination of the phase energy storage devices to a three-phase system. For rectification on the ac currents being present on the secondary, one has to connect the output diodes D_2 in a three-phase bridge configuration, however. Therefore, the function of the converter as a flyback converter is linked to a minimum output voltage value defined by mains voltage and turns ratio.

For the case at hand, a closer analysis can therefore be limited to the circuit shown in Fig. 1(c), which will be called in the following three-phase single-switch discontinuous inductor current mode (DICM) flyback rectifier.

Remark: If one moves the power transistor T_1 instead of $L_{U,1}$ to the input of the three-phase bridge D_1, there follows a three-phase flyback converter structure which requires three turn-off power semiconductor devices. With regard to the desired minimum complexity, this variant (as analyzed in [16]) and other variants of higher complexity (as given in the literature, e.g., in [17], [18]) will not be considered here.

III. Principle of Operation

In analogy to the three-phase single-switch discontinuous-mode pulse rectifier systems, as given in the literature, the control of the system shown in Fig. 2 may be performed in the stationary case with a pulse frequency f_P and an on-time of the power transistor T_1 being constant within the mains period. A synchronization of f_P and mains frequency f_N is not necessary for $f_P \gg f_N$. Due to the low-pass characteristic of the mains filter L_N, C_N, the mains voltage can be assumed to lie directly at the filter output.

For illustrating the operating principle, Fig. 3 shows the conducting states of the converter occurring during the pulse period $t_\mu \in [0, T_P]$. (t_μ denotes a local time running within the considered pulse period.) Concerning the mains phase voltages being approximately constant within the pulse period, we assume $u_{N,R} > 0, u_{N,T} \leq u_{N,S} \leq 0$ (being valid in an interval of $\pi/6$ of the mains fundamental period [cf. Fig. 5(a)]). Due to the phase-symmetric structure of the converter and due to the assumption of a purely sinusoidal voltage system, the analysis of this angle interval determines the system behavior within the entire fundamental period. Fig. 4 shows the local shape of the phase currents being related to Fig. 3.

Before turning on T_1, we have, according to the operation of the system in discontinuous mode, $i_{U,1,(RST)} = i_{U,2,(RST)} = 0$. T_1 is turned on at $t_\mu = 0$. The dc side short-circuit of the bridge circuit consisting of $L_{U,1,(RST),p} =$

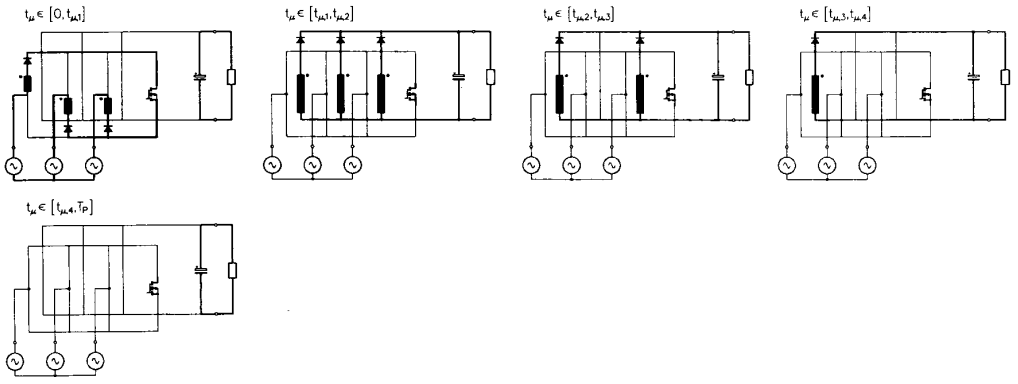

Fig. 3. Sequence of the conduction states of a three-phase single-switch DICM flyback rectifier within a pulse period $t_\mu \epsilon [0, T_P]$ for $u_{N,R} > 0, u_{N,T} \leq u_{N,S} \leq 0$. t_μ denotes a local time within the pulse period. $t_\mu = 0$: turn-on instant of the power transistor T_1. $t_\mu = t_{\mu,1}$: turn-off instant of T_1. The position of the pulse interval within the fundamental period is given by the global time t or by the phase angle $\varphi_N = \omega_N t$ (ω_N = angular mains frequency).

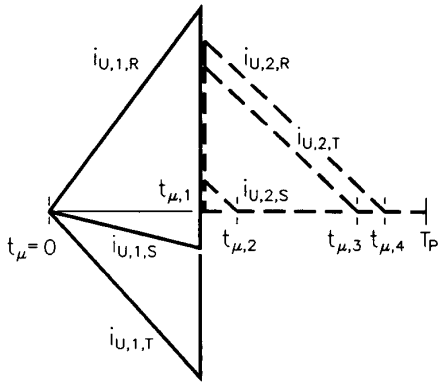

Fig. 4. Time characteristic of the converter input currents $i_{U,1,(RST)}$ and of the output currents $i_{U,2,(RST)}$ (dashed) within a pulse period for $t_\mu \epsilon [0, T_P]$ for $u_{N,R} > 0, u_{N,t} \leq u_{N,S} \leq 0$ (cf. Fig. 3). $t_{\mu,4} - t_{\mu,1}$: demagnetization interval. Parameter: $N_2/N_1 = 1.2$.

$L_{U,1,(RST),n}$ (primary inductances of the phase transformers) and $D_{1,(RST),p}$, $D_{1(RST),n}$ (diodes on the primary side) results in a rate of rise of the input currents being defined by the instantaneous values of the mains phase voltages. For constant turn-on time, therefore, in the turn-off instant $t_\mu = t_{\mu,1}$ of T_1 phase current values are obtained which vary sinusoidally over the mains period and which are proprotional to the respective phase voltage. The demagnetization of the transformers is performed via the secondary diodes $D_{2,(RST)}$. For discontinuous mode, we have to guarantee $t_{\mu,4} \leq T_P$ according to Fig. 4. A stress on T_1 caused by reverse recovery currents of the diodes $D_{2,(RST)}$ is therefore avoided.

Because the demagnetization interval does not influence the mains current shape, after filtering there remain purely sinusoidal mains currents which are in phase with the mains voltages. This is due to the sinusoidal envelope of the converter input currents $i_{U,1,(RST)}$ [cf. Fig. 5(b)] for ideal filtering of the harmonics with pulse frequency (cf. Section IV-B). The system therefore shows (contrary to, e.g., three-phase DICM boost-type rectifiers) low effects on the mains independently of the voltage transfer ratio, as well as a high power factor and resistive mains behavior. Futhermore, independently of the output voltage level, full controllability of the power flow is given. This makes a limitation of the start-up current or an overcurrent protection easily realizable.

The advantages of the proposed concept mentioned so far have to be compared to the basic disadvantages being caused by the high current stresses on the devices due to the flyback converter principle and by a high filtering effort. In order to establish an evaluation basis concerning the applicability of the proposed converter system (going beyond the special application described here) and concerning a comparison to alternative concepts, we therefore want to determine (after formulation of the basic equations for the stationary case) the device stresses being relevant for dimensioning.

IV. System Analysis

A. Assumptions

For the analysis of the stationary operating behavior, the following assumptions are made in order to concentrate on the essential:

- purely sinusoidal, symmetric mains voltage system $u_{N,(RST)}$;
- purely sinusoidal mains currents (fundamental), switching frequency components of $i_{U,1(RST)}$ are suppressed—ideal mains filter;
- the voltage ripple of the filter capacitors C_N may be neglected;
- fundamental components of the voltages across L_N may be neglected as compared to the amplitude $\hat{U}_N$ of the mains phase voltages; accordingly, the filter capacitor voltages are assumed impressed and set equal to the mains phase voltages;
- ideal magnetic coupling of the two primary windings and of the secondary winding for each phase;
- constant output voltage u_O;
- constant load (output) current i_O;

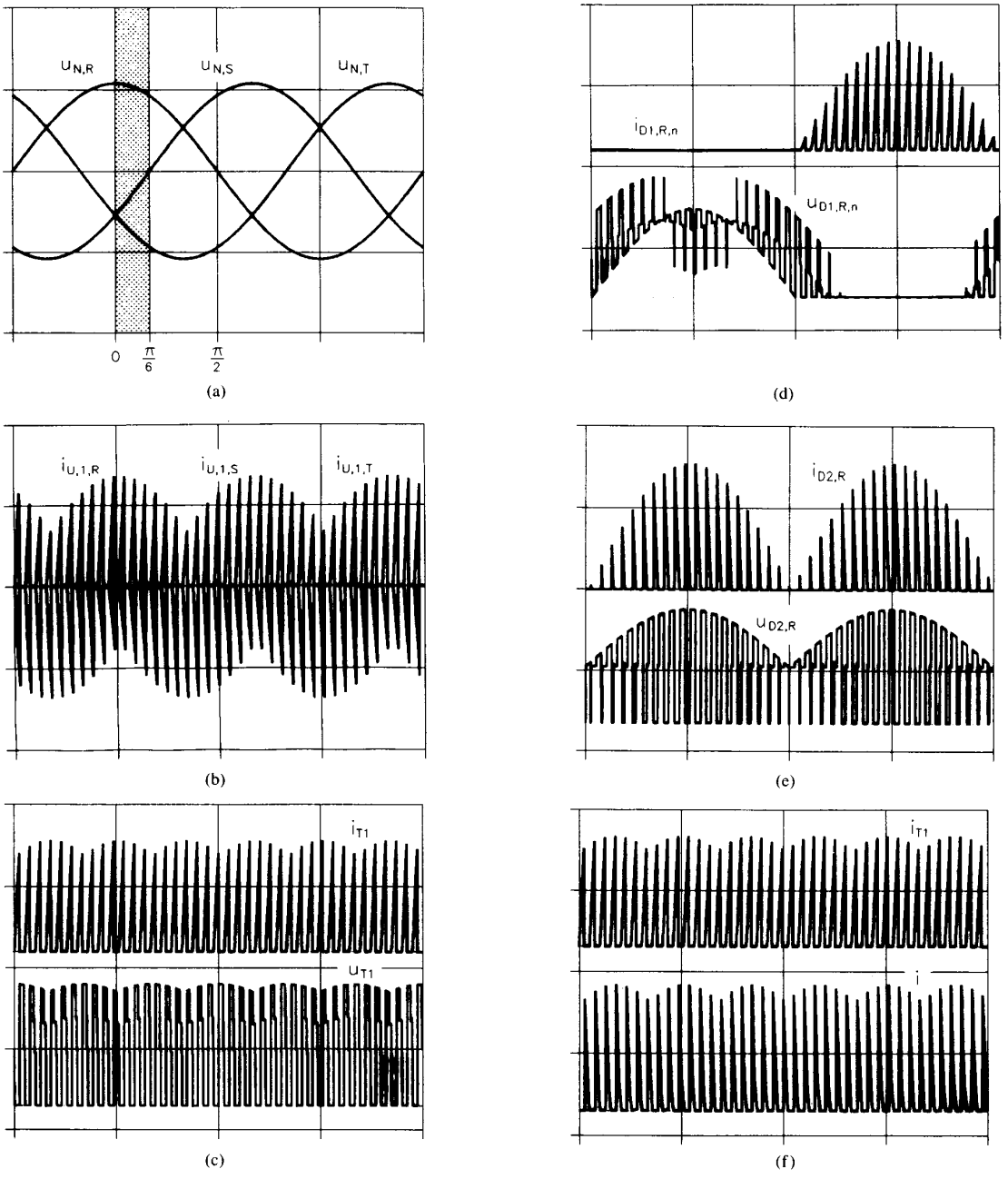

Fig. 5. Digital simulation of a three-phase single-switch DICM flyback rectifier operating with constant switching frequency f_P without mains filter L_N, C_N connected in series based on the assumptions made in Section IV-A. Turn-on time $t_{\mu,1}$ of T_1 constant within the fundamental period; representation of one fundamental period T_N. The angle interval $\varphi_N \epsilon [0. \frac{\pi}{6}]$ considered for the analysis of the system behavior (cf. Section III) is marked in (a) by the dotted area. (a) Mains phase voltages $u_{N,(RST)}$ (150 V/div); (b) converter input currents $i_{U,1,(RST)}$ (10 A/div); (c) transistor current i_{T1} (10 A/div) and transistor blocking voltage u_{T1} (400 V/div); (d) primary diode current $i_{D1,R,n}$ (10 A/div) and diode blocking voltage $u_{D1,R,n}$ (300 V/div); (e) secondary diode current $i_{D2,R}$ (5 A/div) and diode blocking voltage $u_{D2,R}$ (400 V/div); (f) current i feeding the output capacitor and transistor current i_{T1}, (10 A/div). Parameters: $P_O = 800$ W, $U_{N,rms} = 115$ V, $f_N = 400$ Hz, $U_O = 280$ V, $N_1/N_2 = 0.57$, $L_{U,1} = 0.36$ mH, $L_{U,2} = 1.12$ mH, $f_p = 1/T_P = 15.6$ kHz, $t_{\mu,1} = 30.8\,\mu$s.

- $f_P > 200 f_N$ or $T_P \ll T_N$, respectively (mains phase voltages approximately constant within a pulse period);
- ideal system components (especially, neglection of the system losses, switching times, etc.).

Of special importance is the assumption of a pulse frequency being sufficiently higher than the mains frequency. As described in Section V-A, this assumption makes possible a very exact approximation of the current stresses on the system components being relevant for dimensioning. Therefore, one can omit a very time-consuming determination of the device stresses by digital simulation. Furthermore, the knowledge of analytical relationships has (as compared to a system

analysis by digital simulation whose validity is limited to discrete parameter sets) the advantage of a deeper insight into the system behavior, and therefore allows an immediate conclusion regarding the influence of parameter variations on the device stresses.

B. Basic Equations

The analysis of the basic equations of the stationary operating mode is performed for constant f_P and constant local on-time $t_{\mu,1}$ of T_1. Furthermore, only the discontinuous mode is assumed as well as a symmetric split-up of the primary windings of the transformers according to

$$L_{U,1,(RST),_p} = L_{U,1,(RST),_n} = L_{U,1}. \tag{1}$$

For the relation of primary and secondary inductances, we have

$$\frac{L_{U,1}}{L_{U,2}} = \frac{N_1^2}{N_2^2} \tag{2}$$

according to the assumption of ideal coupling. Based on a symmetrical, purely sinusoidal mains voltage system

$$\begin{aligned} u_{N,R} &= \hat{U}_N \cos(\varphi_N) \\ u_{N,S} &= \hat{U}_N \cos\left(\varphi_N - \frac{2\pi}{3}\right) \\ u_{N,T} &= \hat{U}_N \cos\left(\varphi_N + \frac{2\pi}{3}\right) \end{aligned} \tag{3}$$

there follows for the instantaneous input phase currents at turn-off instant of T_1 $t_\mu = t_{\mu,1}$ (cf. Fig. 4)

$$\begin{aligned} i_{U,1,t\mu 1,R} &= \hat{U}_N \frac{t_{\mu,1}}{L_{U,1}} \cos(\varphi_N) \\ i_{U,1,t\mu 1,S} &= \hat{U}_N \frac{t_{\mu,1}}{L_{U,1}} \cos\left(\varphi_N - \frac{2\pi}{3}\right) \\ i_{U,1,t\mu 1,T} &= \hat{U}_N \frac{t_{\mu,1}}{L_{U,1}} \cos\left(\varphi_N + \frac{2\pi}{3}\right). \end{aligned} \tag{4}$$

There, the position of the considered pulse interval within the fundamental period T_N is defined by the angle

$$\varphi_N = \omega_N t. \tag{5}$$

The mains currents remaining after (ideal) filtering of the spectral components with pulse frequency (cf. L_N, C_N in Fig. 2) of the discontinuous input currents $i_{U,1,(RST)}$ now follow directly via averaging related to the pulse period as

$$\begin{aligned} i_{N,R} &= \frac{1}{2}\hat{U}_N \frac{T_P}{L_{U,1}} \delta_P^2 \cos(\varphi_N) \\ i_{N,S} &= \frac{1}{2}\hat{U}_N \frac{T_P}{L_{U,1}} \delta_P^2 \cos\left(\varphi_N - \frac{2\pi}{3}\right) \\ i_{N,T} &= \frac{1}{2}\hat{U}_N \frac{T_P}{L_{U,1}} \delta_P^2 \cos\left(\varphi_N + \frac{2\pi}{3}\right) \end{aligned} \tag{6}$$

where

$$\delta_P = \frac{1}{T_P} t_{\mu,1} \tag{7}$$

denotes the relative turn-on time or the duty cycle of the power transistor T_1. As already described in Section III, *no* low-frequency effects of the system on the mains occur. The amplitude of the (ideally) purely sinusoidal mains currents being in phase with the mains phase voltages is given with (6) as

$$\hat{I}_N = \frac{1}{2}\hat{U}_N \frac{T_P}{L_{U,1}} \delta_P^2. \tag{8}$$

Regarding the loading of the mains, the converter therefore can be assumed to be replaced by equivalent resistances

$$R_N = 2\frac{L_{U,1}}{T_P} \delta_P^{-2} \tag{9}$$

(for Y-connection) which can be set by the relative turn-on time δ_P of T_1.

Remark: This defining equation of an input-equivalent resistance is also given in an identical form for DICM dc-dc (cf. eq. (13) in [19]) and for single-phase ac–dc flyback converters (cf. eq. (13.28) in [12]) and is valid approximately also for three-phase single-switch DICM boost-type input rectifiers (cf. eq. (16) in [8] or eq. (38) in [13]).

Considering the equality of input and output power (because the system has been assumed loss-free), we have the converter output power

$$P_O = \frac{3}{4}\hat{U}_N^2 \frac{T_P}{L_{U,1}} \delta_P^2. \tag{10}$$

For ideal magnetic coupling and for discontinuous operation, the entire magnetic energy being stored at instant $t_\mu = t_{\mu,1}$ in the primary inductances is transferred into the secondary within each pulse period. The power flow as averaged over one pulse period is therefore not influenced by the value of the output voltage u_O, and has the time-constant value

$$p_{O,avg} = P_O \tag{11}$$

for the stationary case. The system shows a constant-power behavior on the output side being also characteristic for single-phase ac–dc flyback converters operating in discontinuous mode [20]. One has to point out, however, that in the case at hand (contrary to single-phase systems) also for highly dynamic output voltage control no low-frequency distortion of the input current shape occurs. This is due to the time-constant (average) power flow for constant turn-on time.

As shown in the following section, besides the output current

$$I_O = \frac{P_O}{U_O} \tag{12}$$

and the duty ratio δ_P of T_1, the global maximum value of the transistor current

$$I_{T1,max} = \hat{U}_N \frac{T_P}{L_{U,1}} \delta_P \tag{13}$$

and the global maximum value of the output diode current

$$I_{D2,max} = I_{T1,max} \frac{N_1}{N_2} \tag{14}$$

are of paramount importance regarding the current stress on the system components.

Remark: In this paper, a global maximum value denotes the maximum of a signal characteristic within the fundamental period. This maximum value has to be distinguished from a local maximum value being present within a pulse interval; e.g., the current values $i_{U,1,t\mu 1,(RST)}$ given in (4) represent local maximum values of the input current shape.

For the relation of the amplitude of the mains current fundamental and the maximum transistor current, there follows with (8) and (13)

$$\frac{I_{T1,max}}{\hat{I}_N} = 2\delta_P^{-1}. \tag{15}$$

Therefore, the results, e.g., for $\delta_P = 0.5$, a current stress on T_1 being four times the peak value of the mains current fundamental. This clearly points out the high current stress on the devices characterizing the discontinuous mode of a flyback converter.

For the (global) maximum duration of the current flow within a pulse interval, there follows

$$T = t_{\mu,4,max} = t_{\mu,1} + \Delta t_{\mu,41,max} = t_{\mu,1}\left(1 + \frac{\hat{U}_N}{U_O}\frac{N_2}{N_1}\right) \tag{16}$$

where

$$\Delta t_{\mu,41,max} = \frac{\hat{U}_N}{U_O}\frac{N_2}{N_1}t_{\mu,1} \tag{17}$$

denotes the maximum duration of the demagnetization phase. For discontinuous mode, we therefore have to guarantee

$$T_P \geq T. \tag{18}$$

V. Component Ratings

For dimensioning and determination of the application region of the system, the current and voltage stresses on the power electronic devices, as well as on the passive components, are of special interest. The current and voltage characteristics to be analyzed for the calculation of the component stresses are shown in Fig. 5(c)–(f), with the exception of the mains filter and the output capacitor currents.

The calculation of the dependencies of device stresses being relevant for dimensioning (current and blocking voltage peak values, current average, and rms values) on the system parameters (input voltage, output voltage, output power, turns ratio, pulse frequency, etc.) as simple analytic approximations is the topic of the following subsections.

A. Analysis Method

The basis of the calculation method is a quasi-continuous analytical approximation of the discontinuous behavior [21], [22], being defined by averaging the quantities over a pulse period. The knowledge of the characteristic of a time function $i_i(t_\mu)$ within one pulse period $t_\mu \in [0, T_P]$ is replaced there by the (discrete) quantities, which can be denoted as local mean value

$$i_{i,avg} = \frac{1}{T_P}\int_0^{T_P} i_i(t_\mu)dt_\mu \tag{19}$$

and local rms value

$$i_{i,rms}^2 = \frac{1}{T_P}\int_0^{T_P} i_i^2(t_\mu)dt_\mu. \tag{20}$$

(*Remark:* The local rms value corresponds to a discrete time function having equal loss.) If these local mean values now are related to the postion φ_N of the pulse interval within the fundamental period T_N (or to the global time $t = \omega_N^{-1}\varphi_N$), then there is defined a *continuous* (global) time characteristic of the local mean value and of the local rms value. By a second averaging related to the fundamental period.

$$I_{i,avg} = \frac{1}{2\pi}\int_0^{2\pi} i_{i,avg}(\varphi_N)d\varphi_N \tag{21}$$

$$I_{i,rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} i_{i,rms}^2(\varphi_N)d\varphi_N \tag{22}$$

there follow accordingly and directly the quantities global mean value and global rms value which characterize the component stresses.

In connection with a minimization of component size and weight of the magnetic devices, one has to aim in a practical realization, by all means, for $f_P \gg f_N$. As a digital simulation based on the assumptions made in Section IV-A shows, the deviations of the analytical expressions from exact results remain below 2% for $f_P > 200 f_N$. Because in the discontinuous mode a transistor stress by reverse recovery currents of the output diodes D_2 is avoided, $f_P \approx 500 f_N$ seems to be obtainable in the case at hand. Therefore, the analytical approximations (21) and (22) show high accuracy. The computation results given in the following can therefore be applied directly as the basis for dimensioning.

B. Characteristic Current Values of the Devices

Mains Filter Capacitance C_N:

$$I_{CN,rms}^2 = \frac{1}{6}\left(1 - \frac{3}{4}\delta_P\right)\delta_P I_{T1,max}^2 \tag{23}$$

$$I_{CN,max} = I_{T1,max} - \hat{I}_N \tag{24}$$

Transformer $L_{U,1,p}, L_{U,1,n}, L_{U,2}$:

Primary:

$$I_{U,1,p,max} = I_{U,1,n,max} = I_{D1,max} \tag{25}$$

$$I_{U,1,p,rms} = I_{U,1,n,rms} = I_{D1,rms}. \tag{26}$$

Secondary:

$$I_{U,2,max} = I_{D2,max} \tag{27}$$

$$I_{U,2,rms} = I_{D2,rms}. \tag{28}$$

Diodes D_1:

$$I_{D1,max} = I_{T1,max} \tag{29}$$

$$I_{D1,avg} = \frac{1}{3}I_{T1,avg} \tag{30}$$

$$I_{D1,rms}^2 = \frac{1}{12}\delta_P I_{T1,max}^2. \tag{31}$$

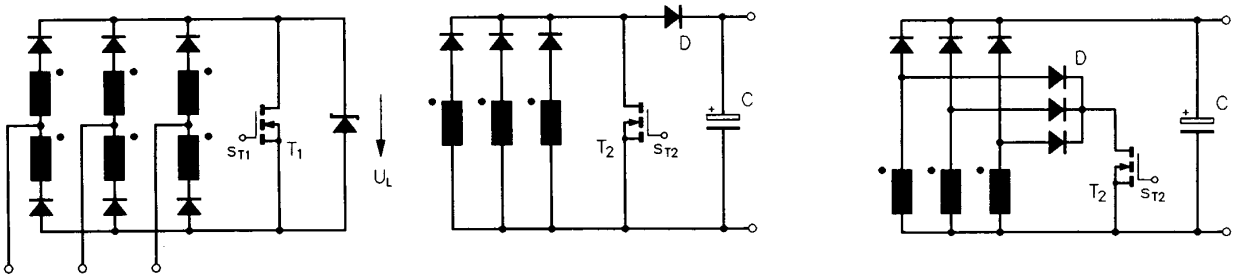

Fig. 6. Reduction of the losses in the blocking voltage limitation circuit U_L connected in parallel to T_1 (the losses occur due to nonideal magnetic coupling of primary and secondary): (a) T_2 turned on in interval $t_\mu \epsilon [t_\mu \leq t_{\mu,1}, t_{\mu,c} > t_{\mu,b}]$ [cf. Fig. 7, (c)], diode D prevents the shorting of the output voltage; (b) as (a), but avoidance of an increase of the conduction losses caused by diode D (representation limited to the secondary systems part).

Power Transistor T_1

$$I_{T1,max} = \hat{U}_N \frac{T_P}{L_{U,1}} \delta_P \tag{32}$$

$$I_{T1,avg} = \frac{3}{2\pi} \delta_P I_{T1,max} \tag{33}$$

$$I^2_{T1,rms} = \frac{1}{6}\left(1 + \frac{3\sqrt{3}}{2\pi}\right) \delta_P I^2_{T1,max}. \tag{34}$$

Diodes D_2:

$$I_{D2,max} = I_{T1,max} \frac{N_1}{N_2} \tag{35}$$

$$I_{D2,avg} = \frac{1}{3} I_O \tag{36}$$

$$I^2_{D2,rms} = \frac{16}{27\pi} I_O I_{D2,max}. \tag{37}$$

Total Current of the Secondary Diode Branches:

$$I_{max} = 2 I_{D2,max}. \tag{38}$$

Output Capacitance C:

$$I^2_{C,rms} = \frac{8}{3\pi}\left(\sqrt{3} - \frac{1}{3}\right) I_O I_{D2,max} - I^2_O \tag{39}$$

$$I_{C,rms} = I_{max} - I_O. \tag{40}$$

C. Blocking Voltage Stress

Power Transistor T_1:

$$U_{T1,max,i} = \sqrt{3}\hat{U}_N + 2\frac{N_1}{N_2} U_O. \tag{41}$$

The voltage value given here is related to ideal magnetic coupling ($k = 1$) of the primary and secondary, according to the assumptions made in Section IV-A.

For nonideal magnetic coupling

$$k = \sqrt{1 - \sigma}$$

of the primary and the secondary (the coupling of the two primary windings $L_{U,1,(RST),p}$ and $L_{U,1,(RST),n}$ is still assumed to be ideal), there occurs, contrary to ideal coupling, no immediate current commutation from $L_{U,1,(RST),p}$ or $L_{U,1,(RST),n}$ to $L_{U,2,(RST)}$ when turning off T_1. For limiting the blocking voltage, one has to provide a circuit U_L in parallel to T_1. Its function is illustrated by an avalanche-diode in Fig. 6. Then a maximum blocking voltage stress on T_1 is fixed by

$$U_{T1,max} = U_L \tag{42}$$

replacing (41). The length of the current commutation interval and, therefore, the power dissipated in U_L are substantially influenced by the maximum blocking voltage stress. For maximizing the system efficiency, one has to aim for values of U_L as high as possible, where the maximum transistor voltage has to be observed.

Diodes D_1: The maximum blocking voltage stress can only be given as a worst-case estimate

$$U_{D1,max} \leq \max\left(\begin{cases} \frac{3}{4}\hat{U}_N + \frac{1}{2}U_L \\ \sqrt{3}\hat{U}_N + \frac{1}{3}U_L - \frac{2}{3}k\frac{N_1}{N_2}U_O \\ \sqrt{3}\hat{U}_N + k\frac{N_1}{N_2}U_O. \end{cases}\right) \tag{43}$$

This is due to the relatively complex blocking voltage characteristic for nonideal coupling and limitation of the voltage across T_1 (cf. Fig. 5(d), valid only for *ideal* coupling).

Diodes D_2: For neglection of a small reduction of the blocking voltage stress for nonideal coupling, there follows

$$U_{D2,max} = U_O + \frac{N_2}{N_1}\hat{U}_N. \tag{44}$$

VI. Converter Design

In the following, the procedure for dimensioning of the converter is outlined, and an overview of the component stresses is given using a numerical example.

A. Procedure

Setting the turns ratio and the inductance of the primary of the transformer has to be done under consideration of the following: 1) blocking voltage stresses on the semiconductors occurring for maximum input voltage $\hat{U}_{N,max}$, and 2) maintaining the discontinuous mode for minimum input voltage $\hat{U}_{N,min}$ and maximum output power $P_{O,max}$.

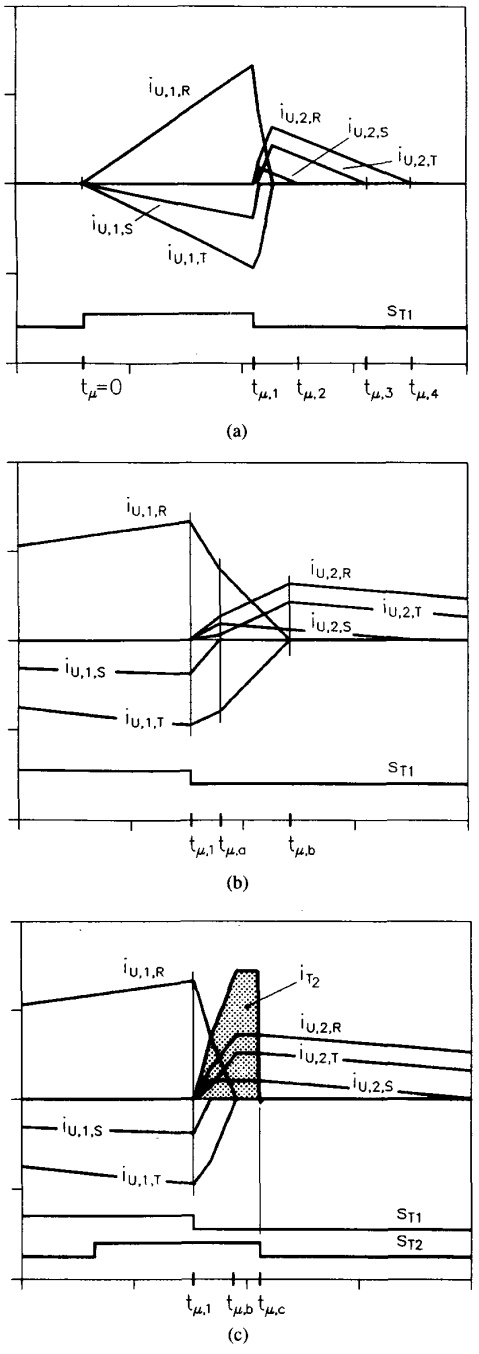

Fig. 7. Digital simulation of the shapes of the input and output currents of the converter ($i_{U,1,(RST)}$ and $i_{U,2,(RST)}$) within a pulse period [cf. (a)]. Nonideal magnetic coupling of $L_{U,1}$ and $L_{U,2}$. s_{T1}: switching function or control signal of T_1, respectively. $t_{\mu,1}$: turn-off instant of T_1. Parameters: as Fig. 5, but $\sigma = 0.0975$ ($k = 0.95$); $u_{N,R} > 0, u_{N,T} \leq u_{N,S} \leq 0$. (b) Current commutation from $L_{U,1,R,p}, L_{U,1,S,n}, L_{U,1,T,n}$ to $L_{U,2,(RST)}$ for $U_L = 800$ V. (c) as (b), but with power transistor T_2 on the secondary. s_{T2}: switching function of T_2, i_{T2} marked by the dotted area. Current commutation interval $t_\mu \epsilon [t_{\mu,1}, t_{\mu,b}]$ significantly reduced as compared to (b), reduction of the limitation losses.

Regarding the blocking voltage stress, one has to keep in mind especially the power transistor T_1. As outlined in connection with (42), one has to set the maximum blocking voltage $U_{T1,max,i}$ (occurring for ideal coupling) sufficiently below the maximum blocking voltage for nonideal coupling (as defined by U_L). Therefore, there follows by transformation of (41) for the turns ratio

$$\frac{N_1}{N_2} \leq (U_{T1,max,i} - \sqrt{3}\hat{U}_{N,max})\frac{1}{2U_O}. \tag{45}$$

One has to point out that a reduction of $U_{T1,max,i}$ leads to an increase of the blocking voltage stress on the diodes D_2 according to

$$U_{D2,max} \geq U_O\left(1 + \frac{2\hat{U}_{N,max}}{U_{T1,max,i} - \sqrt{3}\hat{U}_{N,max}}\right) \tag{46}$$

[cf. (44)]. Using (16) and (18), there follows, for guaranteeing the discontinuous mode for minimum input voltage,

$$\delta_{P,max} \leq \left(1 + \frac{\hat{U}_{N,min}}{U_O}\frac{N_2}{N_1}\right)^{-1}. \tag{47}$$

Then, the inductance of the primary windings of the transformer results in [cf. (10)]

$$L_{U,1} = \frac{3}{4}\hat{U}^2_{N,min}\frac{T_P}{P_{O,max}}\delta^2_{P,max}. \tag{48}$$

The inductance of the secondary windings is given by the relation

$$L_{U,2} = L_{U,1}\frac{N_2^2}{N_1^2} \tag{49}$$

[cf.(2)].

After determination of the basic system parameters, one can now (as shown in the following by using a numerical example) calculate the remaining dimensioning parameters by applying the relations compiled in Sections V-B and C.

B. Design Example

We assume (cf. Section I):

$$\begin{aligned} U_{N,rms} &= 50\,\text{V} \cdots 165\text{V} \\ f_N &= 400\,\text{Hz} \\ U_O &= 280\,\text{V} \\ P_{O,max} &= 690\,\text{W} (P_{O,avg} = 640\,\text{W}) \\ f_P &= 100\,\text{kHz}\ (T_P = 10\mu\text{s}). \end{aligned}$$

The system efficiency to be expected is estimated as $\eta \approx 0.85$ in order to provide a sufficient safety margin. Therefore, $P_O = 810\,\text{W}$ is the basis for dimensioning. For calculation of the maximum duty cycle, the inclusion of a control margin can be therefore omitted.

For the threshold level of the blocking voltage limitation circuit (which defines the maximum blocking voltage of T_1), we choose

$$U_L = 800\,\mathrm{V}$$

and

$$U_{T1,max,i} = 600\,\mathrm{V}.$$

This is done considering the actually occurring blocking voltage stress which should be well below the maximum allowable blocking voltage.

$$U_{T1,max} \leq 1000\,\mathrm{V}$$

(for guaranteeing high operation reliability) for the MOSFET's which are used in parallel for the realization of T_1.

An alternate realization of the switch can be realized paralleling a power MOSFET and an IGBT. This allows a minimization of the conduction and switching losses with a low circuit and control effort [23]. In this case, also, the given assessements concerning the blocking voltage stress are still valid.

The leakage of the transformer is estimated as

$$\sigma = 0.025.$$

According to Sections VI-A and V-C, there follows, then,

$$\begin{aligned} N_1/N_2 &= 0.35 \\ U_{D2,max} &= 945\,\mathrm{V} \\ U_{D1,max} &= 606\,\mathrm{V} \\ \hat{U}_{N,min} &= 71\,\mathrm{V} : \delta_{P,max} = 0.58 \\ \hat{U}_{N,max} &= 233\,\mathrm{V} : \delta_{P,min} = 0.176 \\ L_{U,1} &= 15.5\,\mu\mathrm{H} \\ L_{U,2} &= 126.5\,\mu\mathrm{H} \end{aligned} \quad .$$

As already mentioned in Section IV-B, the component current stress is essentially determined by the maximum values of the transistor current and the output diode current, and by the duty ratio δ_P. For the determination of the maximum stress on the ac-side components, one therefore has to consider the case of minimum input voltage (or maximum δ_P, respectively).

Remark: Because the output power is determined directly by the maximum value of the transistor current according to

$$P_O = \frac{3}{4}\frac{L_{U,1}}{4\,T_P} I_{T1,max}^2 \tag{50}$$

[cf. (10) and (13)], for constant output power $I_{T1,max}$ and, therefore, the secondary currents are not influenced by the input voltage value. The current characteristic values of the dc-side devices are therefore only dependent on the output power and not on the input voltage.

By evaluating the relations given in Sections IV-B and V-B, we get the following current ratings.

Amplitude of the Mains Current Fundamental:

$$\hat{I}_{N,max} = 7.6\,\mathrm{A}.$$

Mains Filter Capacitor C_N:

$$\begin{aligned} I_{CN,rms} &= 6.2\,\mathrm{A} \\ I_{CN,max} &= 19.0\,\mathrm{A}. \end{aligned}$$

Transformer Inductances $L_{U,1,p}, L_{U,1,n}, L_{U,2}$:

Primary:

$$\begin{aligned} I_{U,1,p,max} &= I_{U,1,n,max} = 26.6\,\mathrm{A} \\ I_{U,1,p,rms} &= I_{U,1,n,rms} = 5.9\,\mathrm{A}. \end{aligned}$$

Secondary:

$$\begin{aligned} I_{U,2,max} &= 9.3\,\mathrm{A} \\ I_{U,2,rms} &= 2.3\,\mathrm{A}. \end{aligned}$$

Diodes D_1:

$$\begin{aligned} I_{D1,max} &= 26.6\,\mathrm{A} \\ I_{D1,avg} &= 2.5\,\mathrm{A} \\ I_{D1,rms} &= 5.9\,\mathrm{A}. \end{aligned}$$

Power Transistor T_1:

$$\begin{aligned} I_{T1,max} &= 26.6\,\mathrm{A} \\ I_{T1,avg} &= 7.4\,\mathrm{A} \\ I_{T1,rms} &= 11.2\,\mathrm{A}. \end{aligned}$$

Diodes D_2:

$$\begin{aligned} I_{D2,max} &= 9.3\,\mathrm{A} \\ I_{D2,avg} &= 0.96\,\mathrm{A} \\ I_{D2,rms} &= 2.3\,\mathrm{A}. \end{aligned}$$

Total Current Through Diodes D_2:

$$I_{max} = 18.6\,\mathrm{A}.$$

Output Capacitor C:

$$\begin{aligned} I_{C,rms} &= 4.9\,\mathrm{A} \\ I_{C,max} &= 15.7\,\mathrm{A}. \end{aligned}$$

Output Current I_O:

$$I_O = 2.9\,\mathrm{A}.$$

VII. Effiency Improvement

As mentioned in Section V-C, and as easily verifiable by digital simultion, the obtainable efficiency is influenced substantially by the difference $U_L - U_{T1,max,i}$, as well as by the loss contributions of the semiconductors and the passive components. A high efficiency is inevitably linked to a high blocking voltage stress on T_1 (defined by U_L) and to low tranformer leakage (connected with a high manufacturing effort).

A fictitious increase of U_L (while avoiding an increase of the blocking voltage stress on T_1) can now be achieved by applying a second power transistor T_2 (on the secondary) and of an output diode D (cf. Fig. 6, left side). T_2 is turned on in the interval between turn-on instant and turn-off instant of T_1 [cf. Fig. 7(c)]. During the conduction period of T_1, a current flow via T_2 is suppressed by the fact that the output diodes [cf. Fig. 6(a)] are in the blocking state, or by the diodes D being connected in series to T_2 [cf. Fig. 6(b)]. By shorting the secondary winding, the transformatory coupling of a voltage into the primary (which would slow down the current commutation) is suppressed. Due to this, the current commutation interval is shortened, and the losses in U_L are reduced accordingly.

After turning off T_2, the magnetization energy (stored in $L_{U,2,(RST)}$) is fed into the output via diode D which prevents shorting of the output voltage when T_2 is turned on. Due to its very short on-time, one has to dimension T_2 regarding the pulse current stress, and a transistor with low average current carrying capability can be applied. The control of T_2, which is directly linked to the turn-off of T_1, furthermore allows a simple realization of the control stage. Therefore, with a small increase of system complexity, a significant converter efficiency improvement (or a reduction of the blocking voltage stress in T_1, respectively) is made possible.

VIII. Conclusions

Based on the topology of a dc–dc flyback converter, a new three-phase single-switch DICM rectifier system has been developed in this paper.

The system is characterized by the following advantages and disadvantages.

+ Ideally, there is complete avoidance of low-frequency effects on the mains (purely sinusoidal mains currents being in phase with the mains voltages).
+ Simple structure of the power circuit and of the control circuit (constant pulse frequency and—for the stationary case—constant turn-on time of the power transistor allow the application of standard SMPS control IC's), possibility of sensing the output voltage to be controlled by a third transformer winding which also can be used for the internal supply of the system.
+ High-frequency potential separation between ac and dc sides (possibility of matching the input and output voltage levels and reduction of the component stress by proper choice of the turns ratio).
+ Simple control behavior—corresponds to a DCIM dc–dc flyback system [24], [25] due to the time-constant average power flow [cf. (11)].
+ full controllability of the power flow [inrush-current limitation (start-up or transient over-voltages of the mains), output current limitation (load faults)].
+ Low circuit effort when various potential separated output voltages are to be realized.
+ Possibility of direct parallel operation of several converters.
− High peak current stress on the components (high conduction losses, especially if a power MOSFET is used for realizing T_1, high requirements regarding the ESR (equivalent series resistance) of the filtering and smoothing capacitors, etc..
− High blocking voltage stress on the power semiconductors.
− Low utilization of the magnetic cores; transfer of power pulsating with twice the mains frequency; relatively low utilization of the primary winding by splitting it up into two partial windings where each conducts only one current half-wave per mains period; unidirectional (unsymmetric) magnetization of the transformers.
− High filtering effort for avoiding conducted EMI (electromagnetic interference)—reduction of the power density of the system.

The advantages and drawbacks mentioned above correspond, to a large extent, to those of a DICM dc–dc flyback converter; an application of the system is especially of interest for low output power ($<1\,\mathrm{kW}$) and low rated mains voltage. Finally, it shall be pointed out that one can basically avoid low-frequency effects on the mains only for the discontinuous mode of the system (when three-phase energy is transformed into dc energy, and only a single controlled power electronic device is used). The high current stress being paid for the simple system structure therefore (contrary to dc–dc converters) cannot be reduced by choosing the continuous mode.

Appendix
List of Symbols

C	Output capacitor.
C_N	Mains filter capacitor.
D	Blocking diode on the secondary side.
D_1	Diodes on the primary side.
D_2	Diodes on the secondary side.
f_N	Mains frequency.
f_P	Pulse frequency.
i	Total current of the three secondary branches.
i_C	Output capacitor current.

i_{CN}	Current through the capacitors of the mains filter.
i_{D1}	Current through D_1 (primary side).
i_{D2}	Current through D_2 (secondary side).
$i_{N,R}, i_{N,S}, i_{N,T}$	Mains phase currents.
i_{T1}	Current through transistor T_1.
$i_{U,1,R}, i_{U,1,S}, i_{U,1,T}$	Input phase currents.
$i_{U,1,R,p}, i_{U,1,S,p}, i_{U,1,T,p}$	Primary currents of the transformers (positive branches).
$i_{U,1,R,n}, i_{U,1,S,n}, i_{U,1,T,n}$	Primary currents of the transformers (negative branches).
$i_{U,2,R}, i_{U,2,S}, i_{U,2,T}$	Transformer secondary currents.
k	Coupling factor between primary and secondary windings.
L_N	Mains filter inductances.
$L_{U,1}$	Inductance of a primary winding (positive or negative branch).
$L_{U,2}$	Inductance of a secondary winding.
N_1	Number of turns of a primary winding.
N_2	Number of turns of a secondary winding.
p_O	Output power.
R_N	Power-equivalent input resistance of the converter (Y-connection).
t	(Global) time (within a fundamental period).
T	Global maximum value of the sum of turn-on time of T_1 and duration of the demagnetization phase.
T_1	Main power transistor.
T_2	Auxiliary power transistor for reduction of the losses in U_L.
T_N	Mains fundamental period.
T_P	Pulse period.
t_μ	Microscopic (local) time counted within a pulse interval.
U_L	Threshold voltage of the voltage limitation circuit of T_1.
$u_{N,R}, u_{N,S}, u_{N,T}$	Mains phase voltages.
u_O	DC output voltage.
$u_{T1,max}$	Maximum blocking voltage stress on T_1 for nonideal magnetic coupling.
$u_{T1,max,i}$	Maximum blocking voltage stress on T_1 for ideal magnetic coupling.
δ_P	Relative turn-on time of T_1, duty cycle.
φ_N	Phase assigned to time $t(\varphi_N = \omega_N t)$ within the fundamental period.
ω_N	Mains angular frequency.
σ	Transformer leakage coefficient (according to coupling k).

Lower case letters characterize (local or global) time-dependent quantities.
Upper case letters characterize time-indpendent global mean or rms values.

Indices:

avg	linear mean value
i	common counting subscript, ideal magnetic coupling
max	global maximum value
min	global minimum value
n	components between the phase inputs and the negative bus bar of the primary bridge
p	components between the phase inputs and the positive bus bar of the primary bridge
(RST)	phase R or phase S or phase T
rms	quadratic mean value
$t\mu i$	time assignment of local current value
μ	local time (within a pulse period)
1	primary side
2	secondary side

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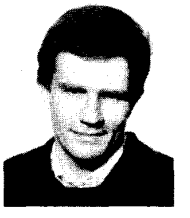

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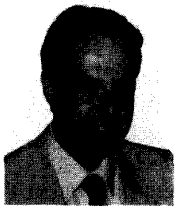

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